CITIROC 1A

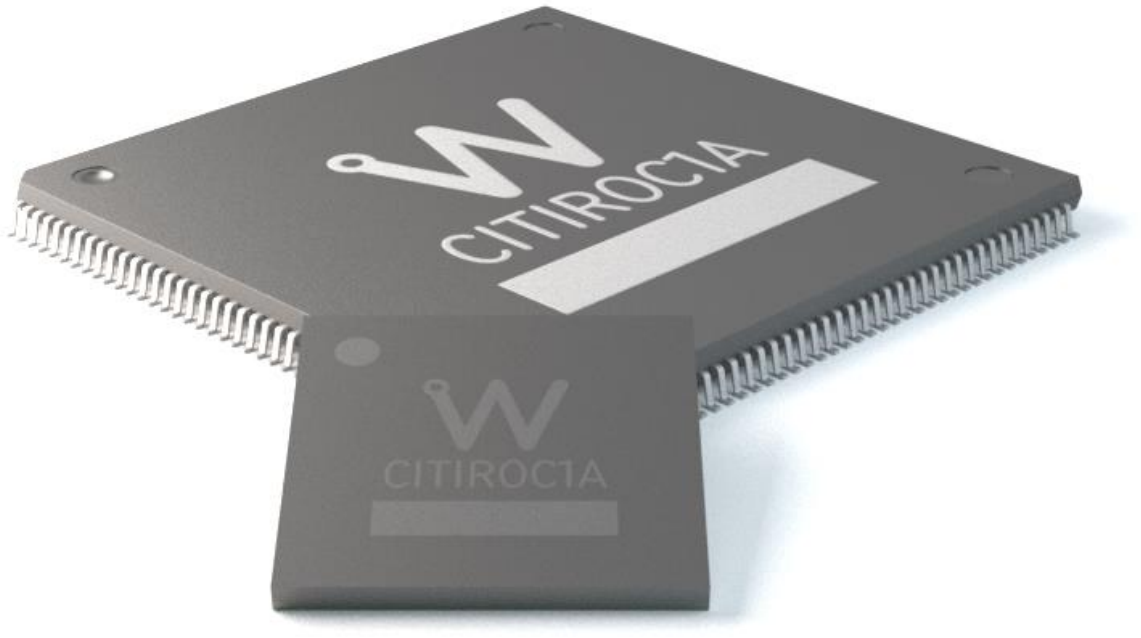
SOFTWARE & TEST BOARD USER GUIDE

Version: 19 February 2020

Abstract

CITIROC 1A is a 32-channel front end ASIC dedicated to read-out SiPM detectors.

This guide explains how to install and use the test board for CITIROC 1A and how to operate with the associated software.



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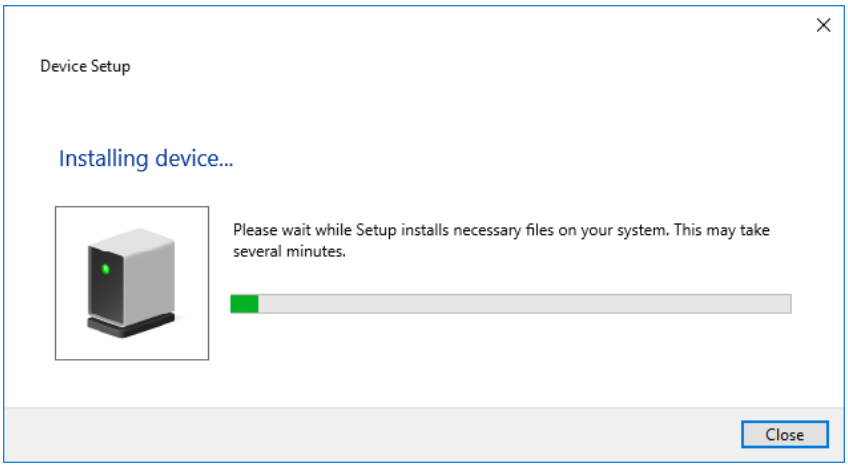
1 Installation & Test of the Test Board

1.1 Pre requisites

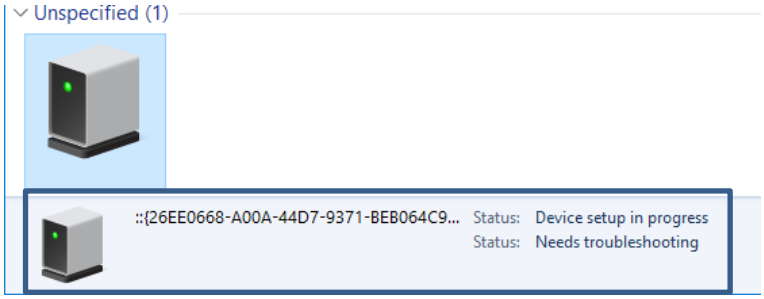
The use of this PCB requires:

- A computer (windows OS) with USB connection
- A USB-A to mini-USB cable
- Optional : A positive output power supply (delivering 500mA)

The first time a Weeroc testboard is plugged, the following message should prompt.



In order to verify that the drivers are correctly installed, go in the control panel under the "Devices and Printers" window. the PCB_Citiroc 1A device should have gone from



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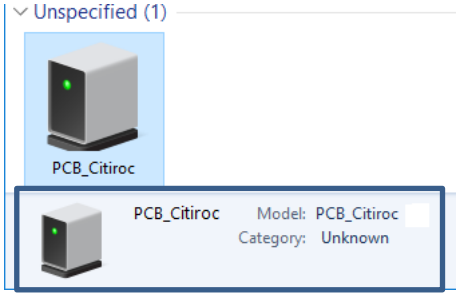

1.2 Installation guide

Before running the software for the first time, please verify that the PCB is correctly identified in the "Devices and Printers" window under the control panel. The release of the CITIROC 1A user interface can be found in the Weeroc download center on the website http://www.weeroc.com .

2 Evaluation board description

The evaluation board has mainly been developed to allow characterization and debug of the ASIC CITIROC 1A. Some features were added on the board or in the firmware/software to allow versatility and its use with real detectors or within an experiment. The schematics of the evaluation board, the firmware and software sources are provided on the WEEROC Website, users can modify anything they need to fit their own requirements.

- This board provides easy access to each CITIROC 1A pin, as all analogues pins are connected to through-hole test points (where pin number is written on the silkscreen layer) and as all digitals I/Os are connected to probes between the ASIC and the FPGA.
- A "VCC_SELECTION" jumper ① allow to choose whether the board is powered through the USB connection or using an external power supply plugged to the top right connector of the board (~6V, ②).
- Many test points are also connected to the FPGA, outputting digital internal nodes.
- OR32 trigger signal and Hit_Mux output are available on LEMO connectors
- 3 analogue buffers provide ASIC's analogue outputs on 50 ohm load on LEMO connectors. Two are direct charge outputs (OUT_LG and OUT_HG) and one is the analogue probe (OUT_PROBE).
- 2 external ADCs are on-board, allowing ASIC data acquisitions.
- SiPM & HV connectors enables the use of this board with SiPMs or matrixes.
- When not using a SiPM and thus the high voltage connector it needs to be shorten to bring gound to the floating high voltage part of the board.

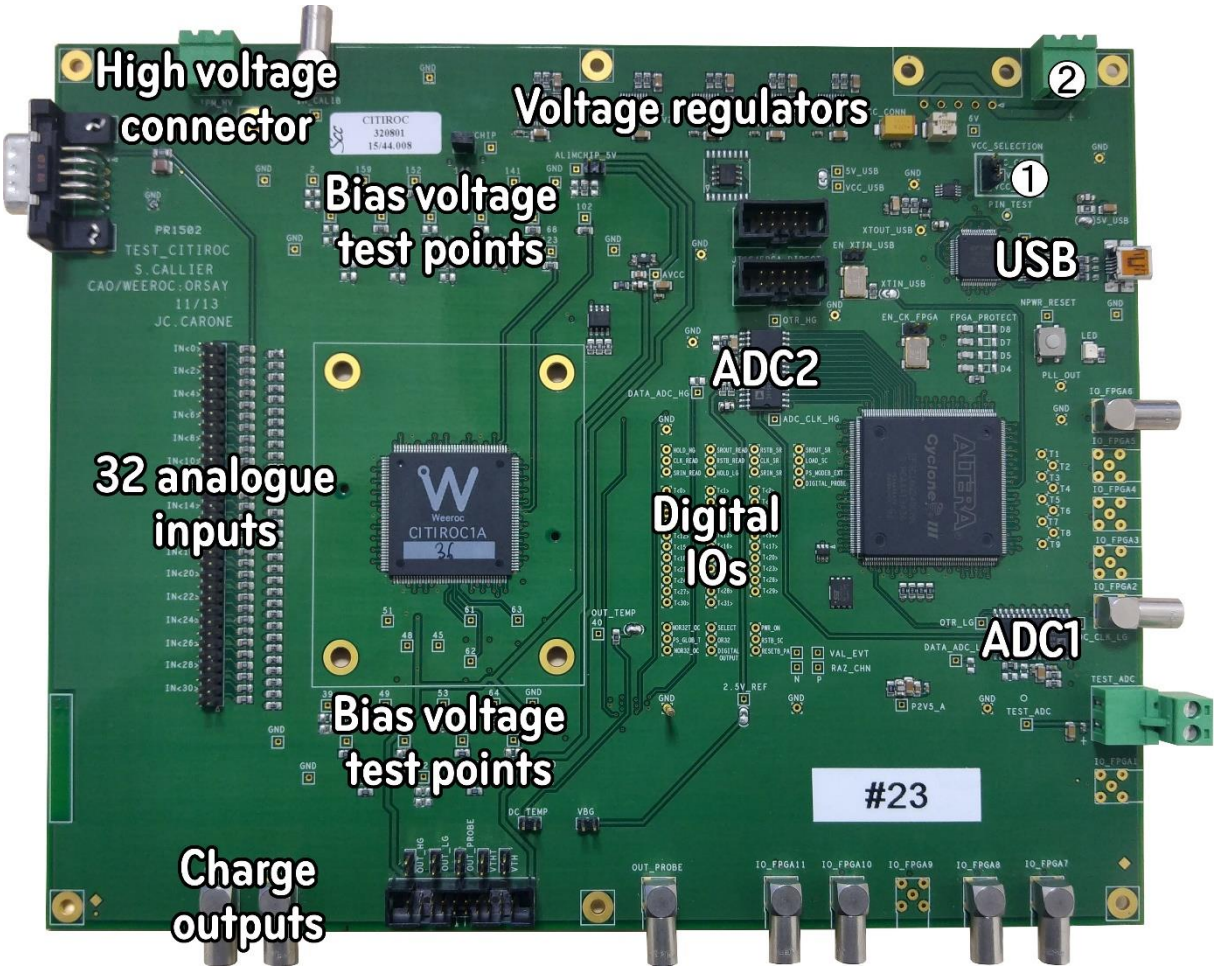

Figure 1 – Citiroc 1A testboard

3 Software description

The software has been written in the C# language with the help of visual studio (free version). The source code is available to help comprehend the functioning of the software. This is especially useful if users aim to develop their own DAQ system.

Figure 2 – Citiroc 1A software connect tab.

To start the test board you need to:

1. Connect the USB cable from the PCB to your computer.
2. Provide power supply to the PCB if not provided by the USB (the power supply can be switched between external and USB with the jumper on the top right of the evaluation board).
3. Start the software and click on the "Connect" round button.

When connecting the evaluation board, drivers for the USB device should install automatically. If it is not the case, the drivers can be found on the FTDI website (http://www.ftdichip.com/Drivers/D2XX.htm).

When this software is launched and the "Connect" button clicked, no error should occur, meaning that the installation has been done successfully and all the drivers and dll have been found. If a crash occurs or if you need assistance for any other issue with the software, contact the Weeroc support by opening a new support ticket at the address http://www.weeroc.com/my-weeroc/support.

While this user guide will help the user to use the software and evaluation board, it should be noted that there is an embedded help in the software. By hovering controls with the mouse, the green bottom part will be filled with information on the object being hovered.

The firmware version is automatically detected by the software. If the firmware version doesn't correspond to the expected version, the software will propose to load the correct firmware version. The expected firmware version corresponds to the last number in the software version. The firmware version is 129 on Figure 2, while the software version is 0.9.8.129. On the title bar is also displayed the temperature of the board given by the TMP275 component on the board.

Screenshots can be take thanks to the button with the photo icon on the title bar. The screenshots in this user guide have been taken with this feature.

3.1 The slow control page

All the slow control parameters of the CITIROC 1A are displayed on this tab control, allowing tuning & tests for different settings.

To program the CITIROC 1A, users must set the Slow Control parameters and click on the "Send SC" button on the bottom right of the page. The slow control parameters are loaded twice in the ASIC and a checksum is done to verify that the slow control has been correctly loaded in the ASIC. The "Send SC" button turns green if the load succeeded. If it turns red, then there is an error in the slow control bits loading. Verify the board is plugged and powered correctly.

The settings can be saved in a text format file thanks to "Save SC" button, and reloaded from this file by the "Load SC" command or by drag and dropping the file on the software window. This is very helpful as there are 1144 bits of slow control.

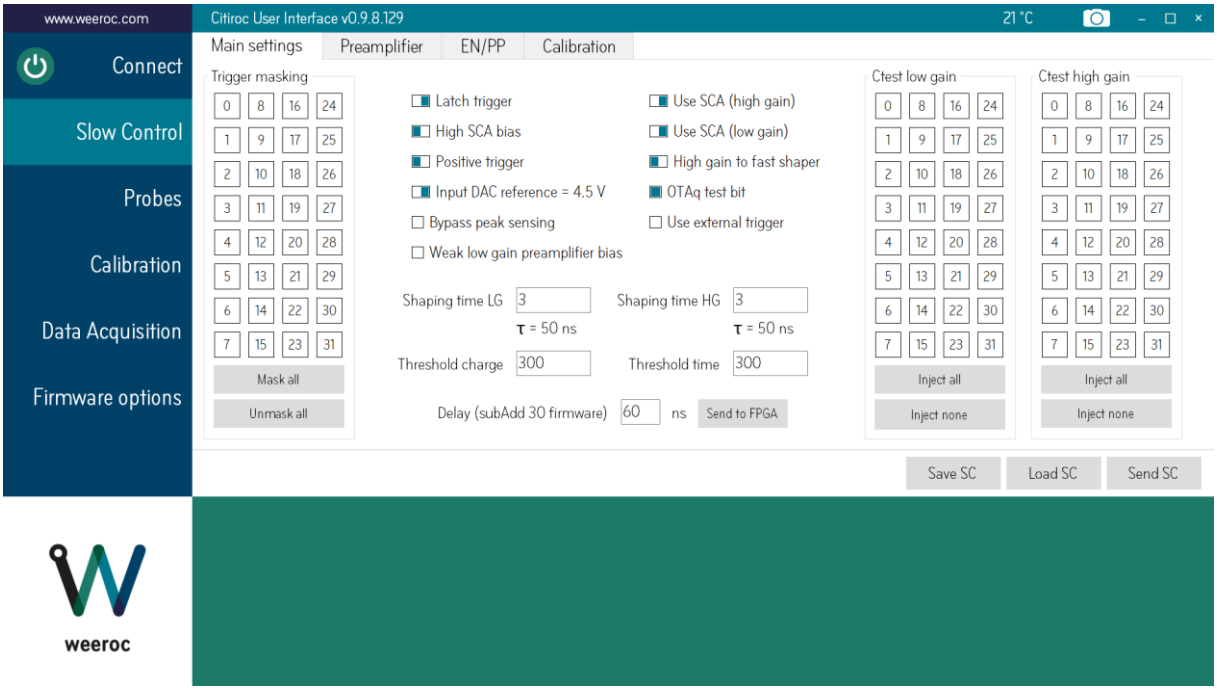

Figure 3 – Slow control main settings tab.

The main slow control page brings together slow control parameters such as the common thresholds for time and charge triggers or the shaping behavior of the charge shaper. Please note that the "delay" parameter is actually written to the FPGA and have to be sent separately. It has been placed under this tab for convenience when programming the ASIC behavior without having to go under the "Firmware options" page.

The mask group box allow masking triggers from the "charge" discriminator. With the mask, "hit" information will not be registered on these channels and a trigger will not initiate data acquisition. The number

in the checkbox corresponds to the channel number. A check means the channel is masked. "Ctest" checkboxes allow to inject signal in the checked channels via the "IN_CALIB" LEMO connector (Figure 4).

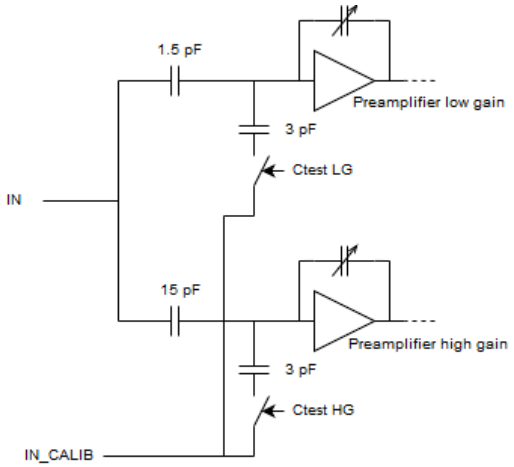

Figure 4 - Ctest injection schematic

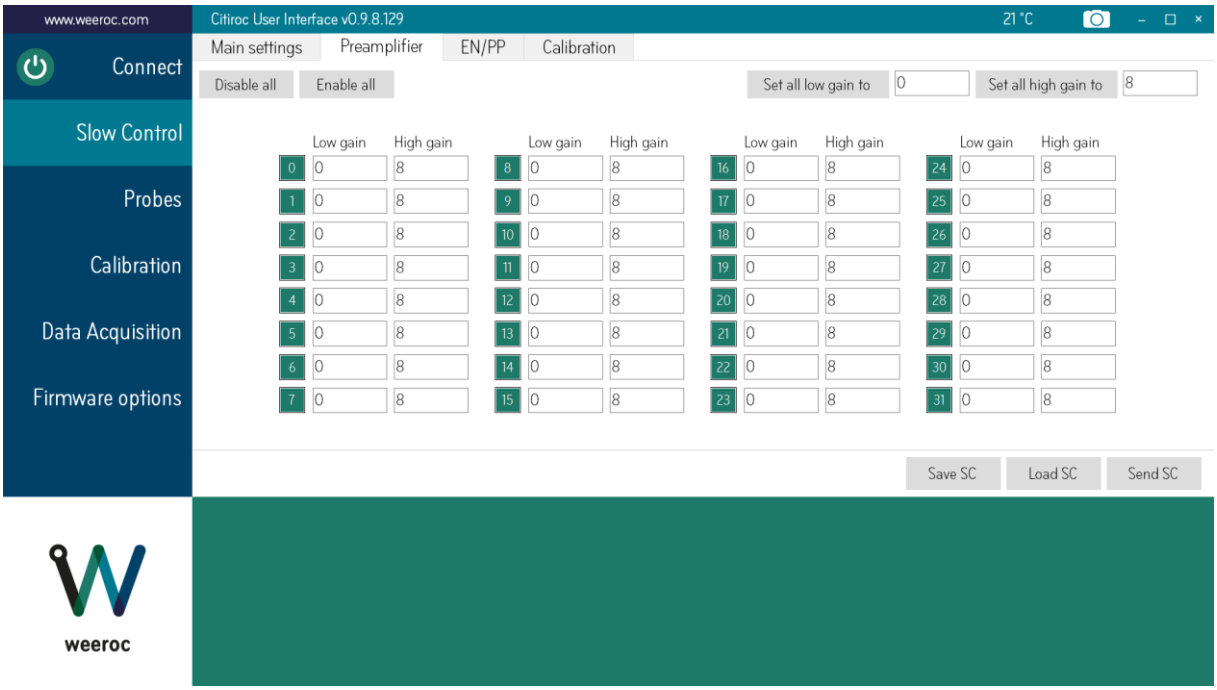

Figure 5 – Preamplifiers tab.

Users can disable preamplifiers channel by channel by clicking the checkboxes. The gain of preamplifiers can also be tuned by individual channels following the formula $-C_{in}/C_f$ with C_f the feedback capacitor adjustable from 0 to 1575 fF with a 25 fF step and C_{in} = 15 pF for the high gain preamplifier and 1.5 pF for the low gain preamplifier.

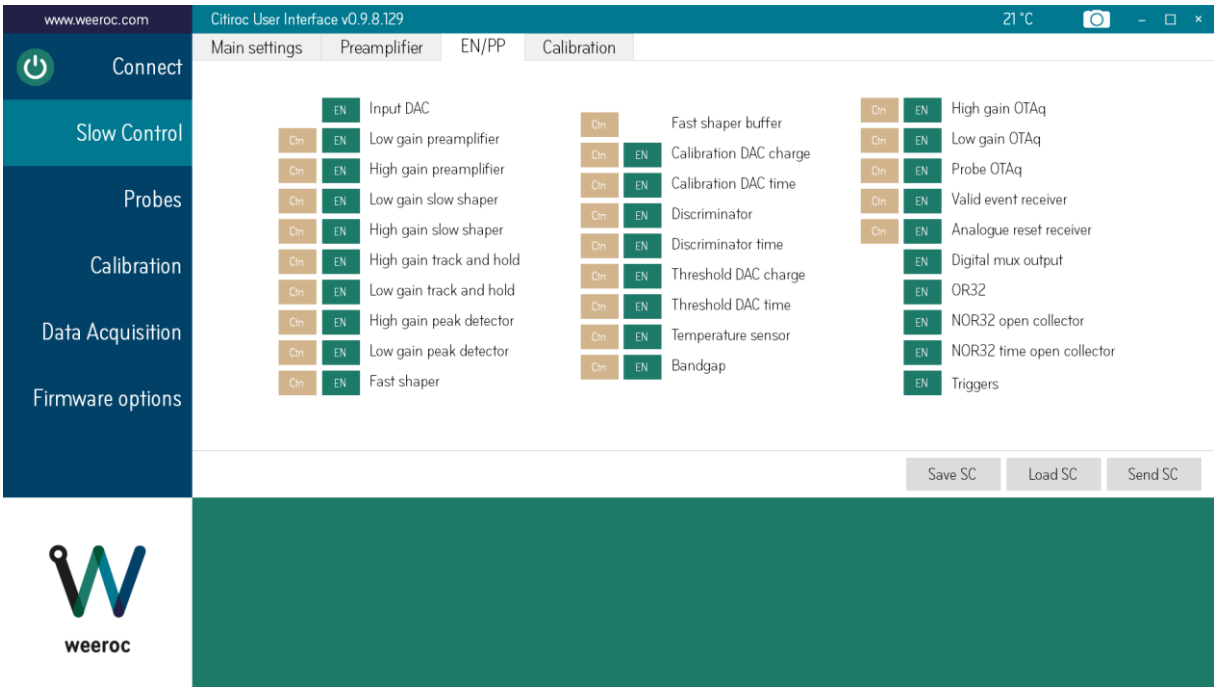

Figure 6 – Slow control enable and power management tab.

The EN/PP tab stands for "Enable" and "Power Pulsing". On this tab it is possible to disable certain parts of the chip in order to reduce the power consumption by disabling unused blocks or for test purpose. Some of these blocks can also be power managed in continuous power mode (Ctn) or in power pulsing mode[1] (PP).

[1] In power pulsing mode, various components in the ASIC could be shut down or powered on according to the sequences provided by users.

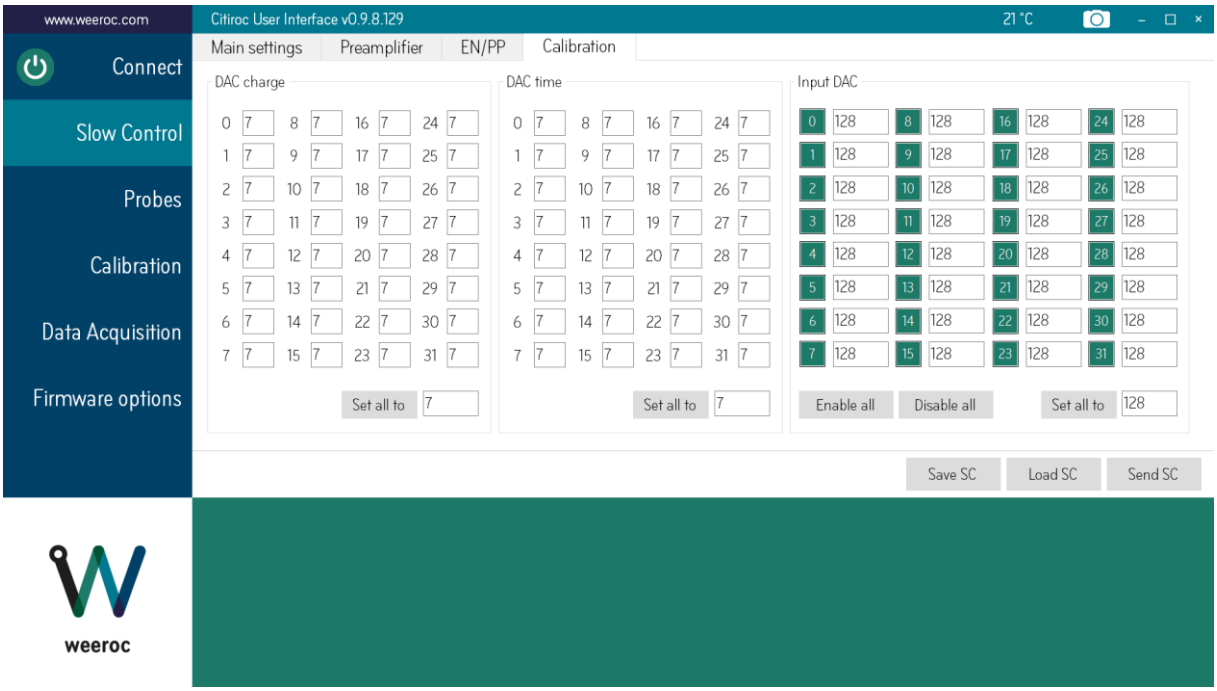

Figure 7 – Slow control calibration tab.

The calibration tab is used for the input DAC and 4-bit DAC values.

The input DAC slow control group box allows user to tune the DC value of the ASIC inputs. When using CITIROC 1A with SiPM arrays, the input DAC provides the possibility to user of correcting detector gain dispersion by adjusting individually the high voltage biasing of each input channel. The number next to the textbox corresponds to the channel number. These numbers may differ from the SiPM channel number allocation. The checkbox containing the channel number on the left of the textbox allows to disable input DAC by channel. When the input DAC is disabled no acquisition can be done on the corresponding channel.

The purpose of 4-bit DAC group boxes is almost similar to input DAC except this adjustment is applicable to "time" and "charge" trigger threshold. This threshold is provided by a 10-bit DAC (available in "Main settings" tab – Figure 3) and it is common to the 32 channels. In order to correct the trigger dispersion, 4-bit DAC for trimming the two thresholds have been added for each channel. Nevertheless practice has shown that this calibration is not needed to perform optimized measurements.

3.2 The probe page

An internal ASIC shift register allows to monitor each channel and to display them on oscilloscope. User can chose to monitor the preamplifiers and shapers signals from analogue probe register.

The analogue signal (available after a click on "Send probes" command) is outputted and buffered to the "OUT_PROBE" LEMO connector onboard. This probe system is usually used for debugging. In typical ASIC operation, it is advised to turn off the OTA for probes and set the analogue probe to "No analogue probe" in order to avoid analogue performances degradation.

For the internal digital signal, the peak detector mode can be probed, i.e. track mode or peak sensing mode.

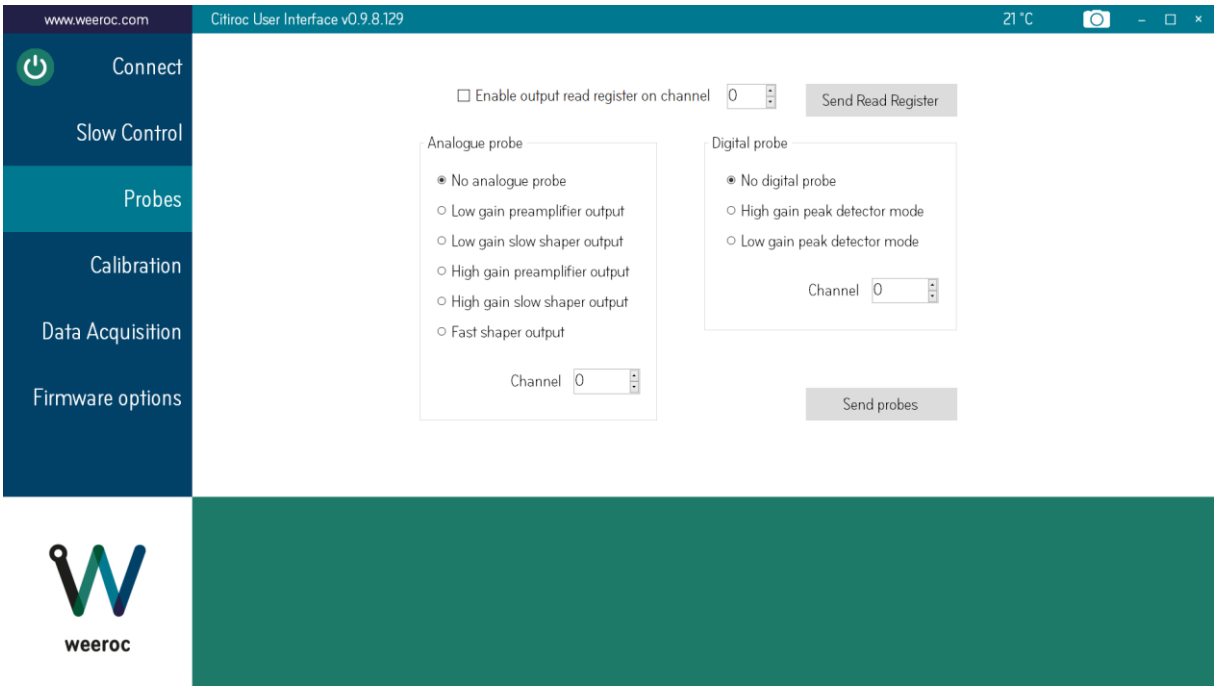

Figure 8 – Probes register page

3.3 The calibration page

3.3.1 S-curves

The first tab in this page is called "S-curves" and its aim is to perform trigger efficiency test (named S-curves). It is done by scanning through several values of threshold and measuring if a trigger happens on the output signal of the fast shaper. The acquisitions are windowed by a clock Clk which toggle the "valid event" firmware signal. If a trigger happens outside the window it will not be taken into account.

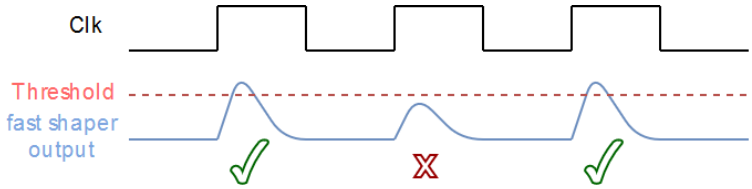

Figure 9 - S-curves acquisition chronogram

When the threshold is way below the signal, the trigger efficiency will be 100%. With a threshold way over the signal, trigger efficiency drops to 0%. On Figure 9 the threshold is set near the tip of the noiseless signal so the ASIC will have a ~50% chance of triggering depending on the noise. Following the Figure 9 the ASIC would trigger 2 times in 3 acquisition windows, resulting with a 67 % trigger efficiency.

The user has the choice of plotting the S-curves with the current slow control configuration on the "time" or "charge" triggers thanks to a checkbox. The acquisition is started by clicking on the "Start S-curves" button. The S-curves can be plotted on the pedestal or on the signal thanks to a switchbox. To plot the S-

curves on a signal you will need to inject signal through the "IN_CALIB" connector. The injected signal must be synchronized with the clock signal on "IO_FPGA9" to send the signal in each acquisition window as seen on Figure 9. The clock speed can be adjusted from 1 kHz to 100 kHz. Slower clock will make the acquisition of the S-curves longer. For more information on S-curves, see appendix.

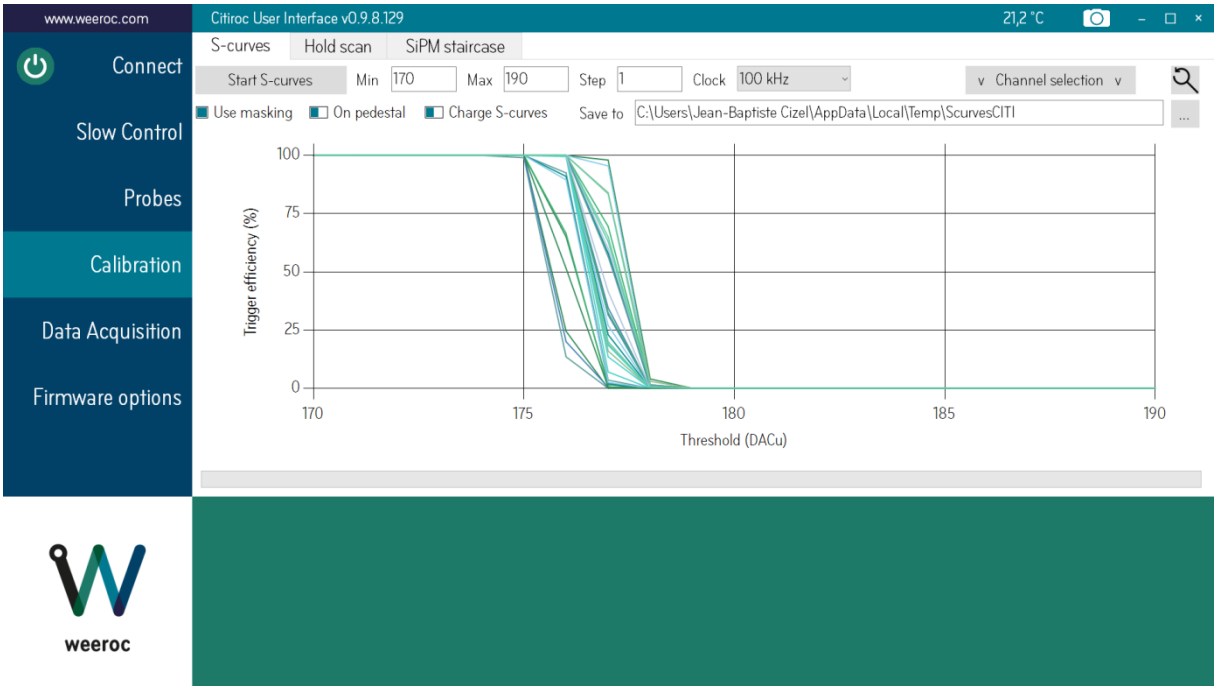

Figure 10 – S-curves tab.

It is also possible to plot only selected channels in the channel selection. Plotting the S-curve on one channel will be 32 times faster than doing it on the 32 channels. It can be useful if the user want to have a fast idea of where the pedestals are since the distribution is narrow.

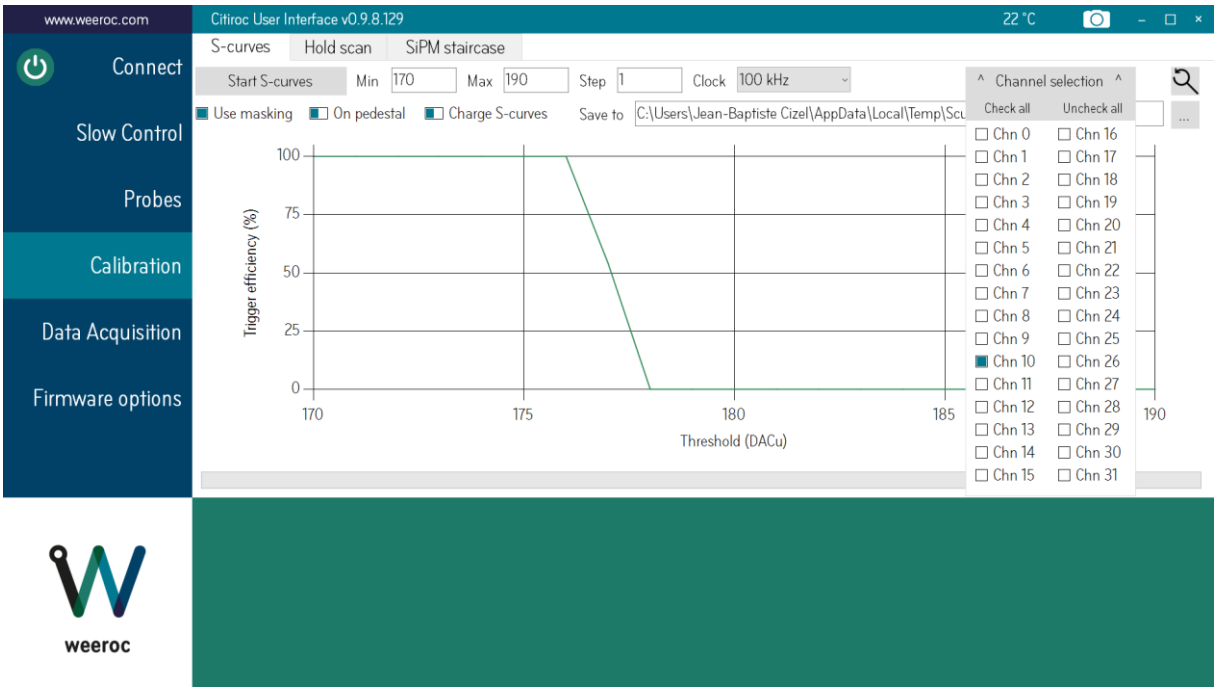

Figure 11 –S-curve on channel 0.

3.3.2 Hold scan

The second tab under the calibration page is the "hold scan". It traces the low gain or high gain shaper output signal by varying the "hold" delay value. In order to have it working properly a signal should be injected in the measured channel and a trigger must start the data acquisition. A fit on the result of the scan is performed and the x-axis value corresponding to the maximum of the fit is automatically extracted. The delay parameter (in Main settings tab – Figure 3) is updated with the extracted value. The fit is meant to be used with the SCA. When using the peak detector a high delay value can be used since the ASIC doesn't need to trigger the "hold" on the peak of the shaper signal.

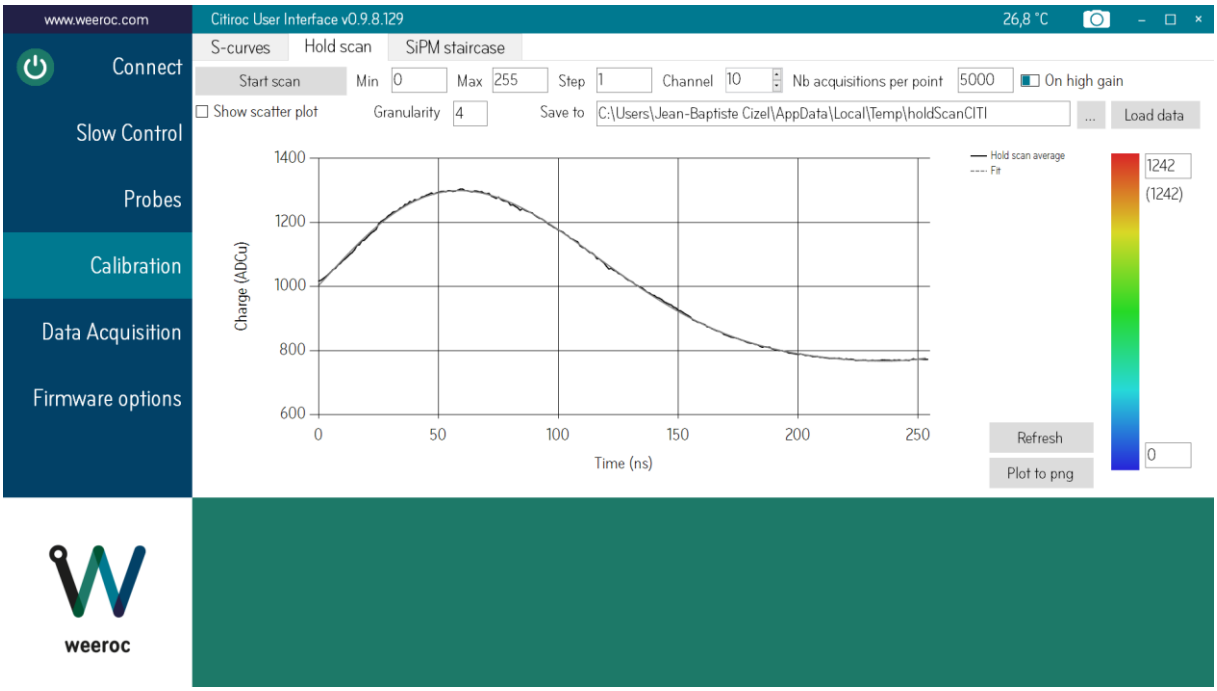

Figure 12 – Hold scan tab.

It is advised that the hold scan should be redone if the charge shaping parameters are changed through the slow control parameters because the peaking time of the shaper will vary. Once the proper delay parameter corresponding to required shaper peaking time is selected, data acquisition can be effectively done.

When doing the hold scan on a SiPM signal it is interesting to be able to see all the acquisitions. It can be done by checking the "Show scatter plot" checkbox. This plot, depending on the total number of points, can be very consuming for a pc so the user can change the "granularity" parameter. It will merge adjacent points on the Y-axis. For example with a granularity of 4, there will be 4 times less points to plot because they will be merged 4 by 4. The following figures have been done with a 3x3 SiPM with a high gain preamplifier gain of 54.

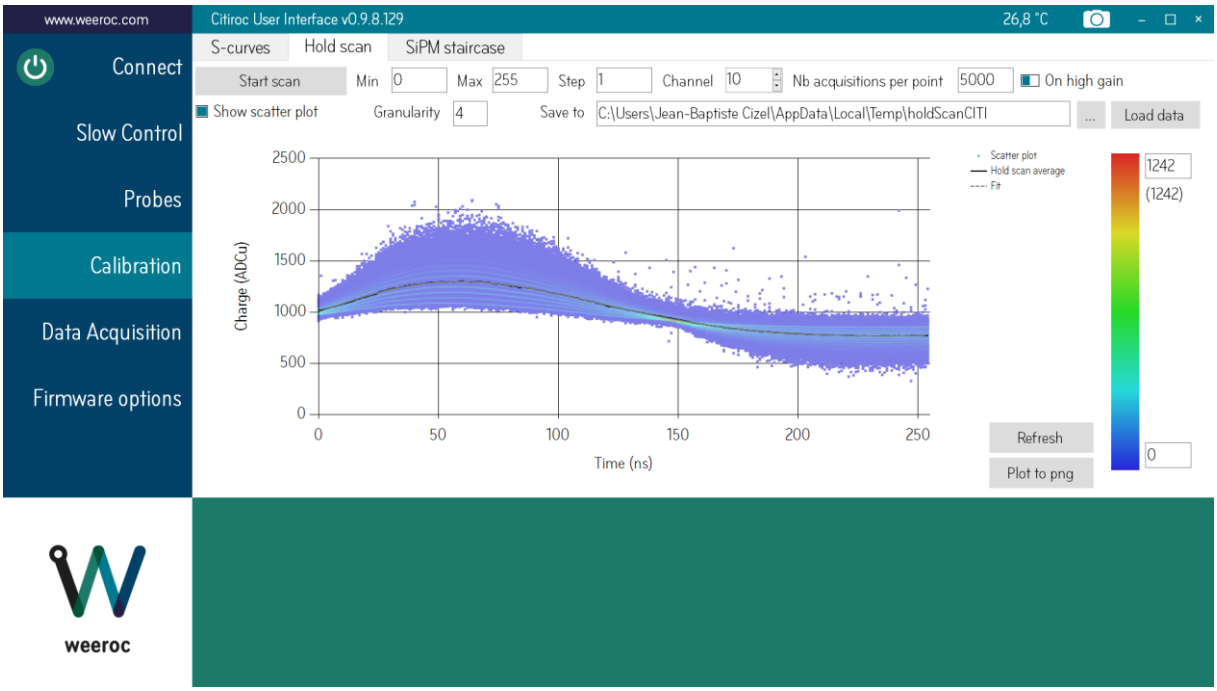

Figure 13 – Hold scan scatter plot.

By reducing the maximal value on the gradient color scale, the contrast on the scatter plot can be improved. The maximal value is automatically set as being the highest redundancy, most likely around 150 ns where all the photoelectron signal cross the baseline. By changing the max value to 250, the color scale will be done between 0 and 250 and every value above 250 will have the same color.

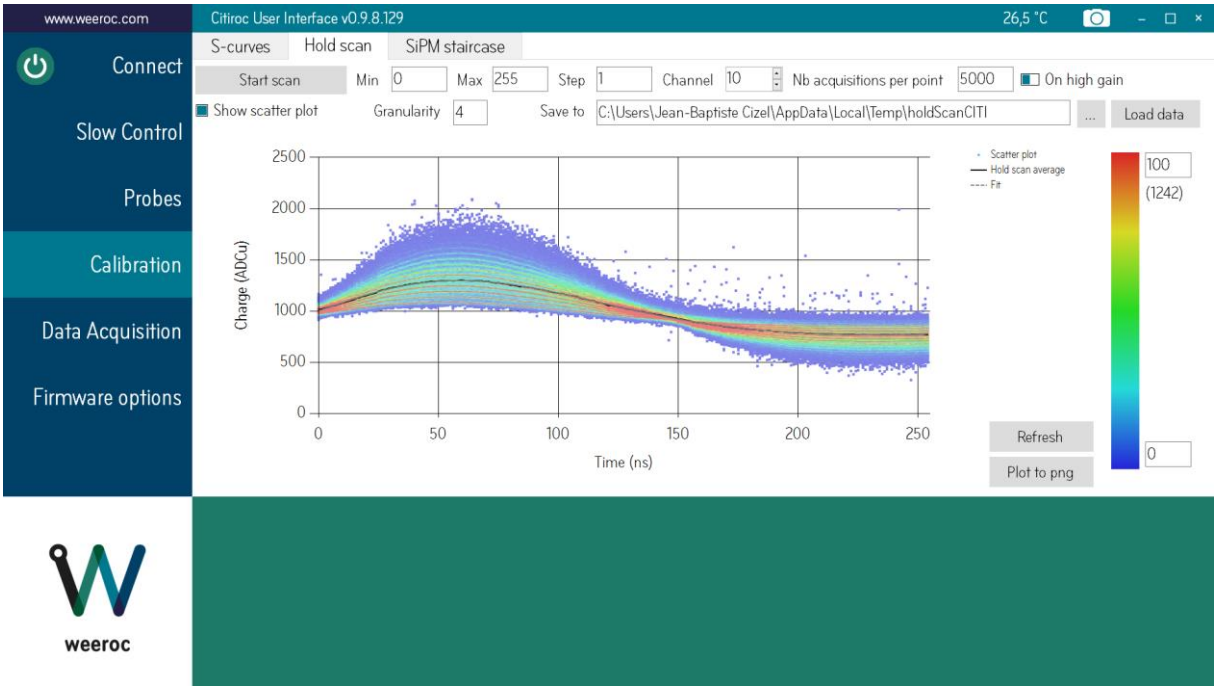

Figure 14 – Maximal color gradient value change.

By choosing a value other than 0 on the minimal value of the gradient color scale, the user will cut all the low-redundancy events and "clean-up" the plot. Note that changing this value will reload the scatter plot and reset the maximal value of the gradient color scale.

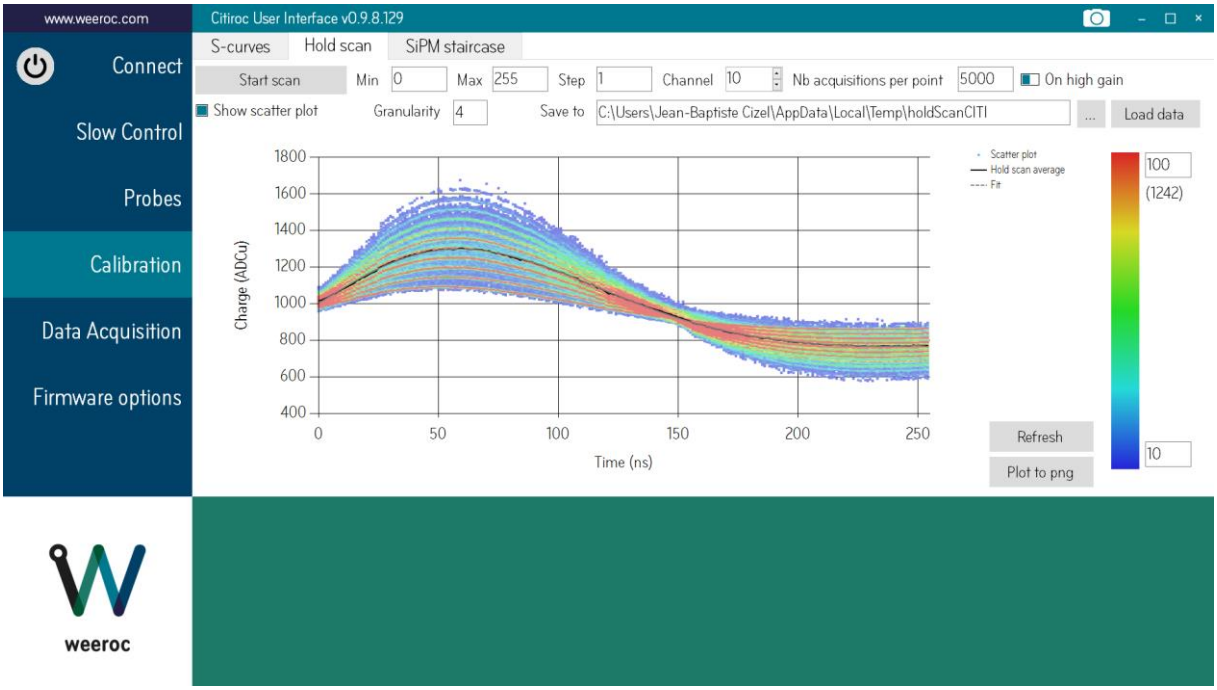

Figure 15 – Minimal color gradient value change.

To allow to visualize the scatter plot with the highest resolution (granularity = 1) on a large number of points without any lag it is advised to export the scatter plot as a .png image. Uncheck the "Show scatter plot" checkbox and choose the granularity, min gradient value and max gradient values to fit your needs. Then click "scatter plot to png" to do the export.

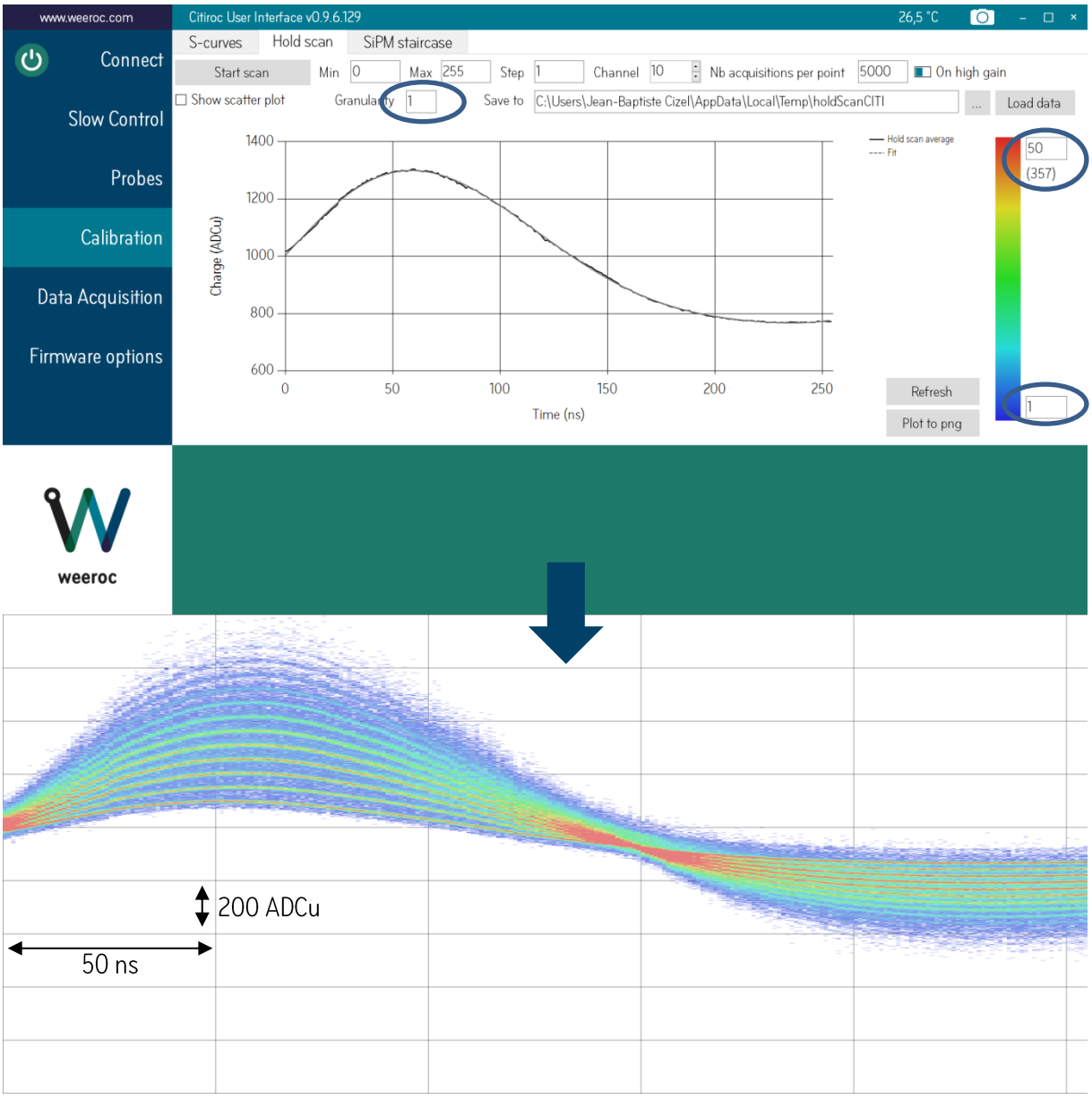

Figure 16 – Exporting scatter plot to png image. X-axis = 50 ns/div ; Y-axis = 200 ADCu/div.

On the Y-axis and with granularity = 1, 1 pixel = 1 ADCu. With granularity = 4, 1 pixel = 4 ADCu, etc.

3.4 SiPM staircase

The SiPM staircase measurement is used to locate the pedestal and 1, 2, 3 photoelectrons positions relative to the threshold DAC code. The SiPM must be plugged on the board and set in the dark with no parasitic light. A scan through the threshold DAC values will allow to locate the pedestal and the first photoelectrons values thanks to the dark noise of the SiPM.

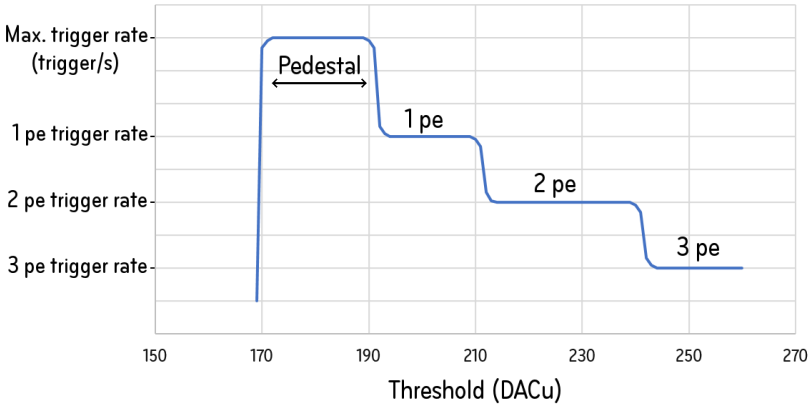

Figure 17 – Staircase principle.

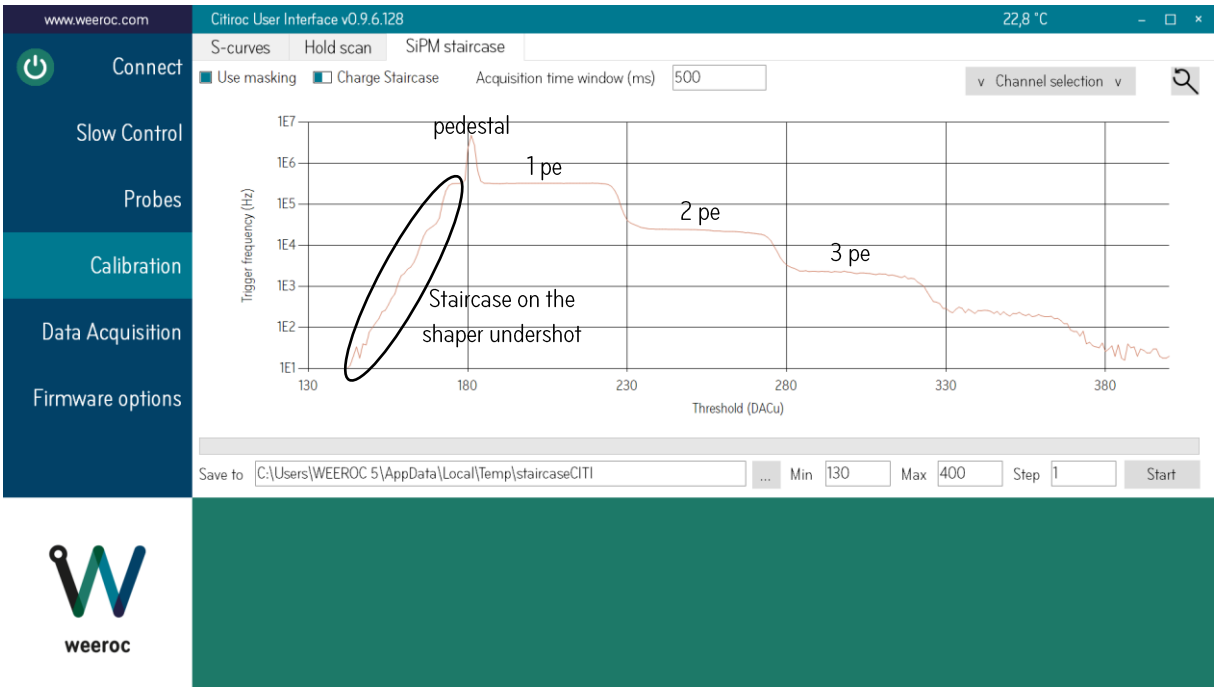

Figure 18 – Staircase on charge trigger.

The same can be done on the time trigger.

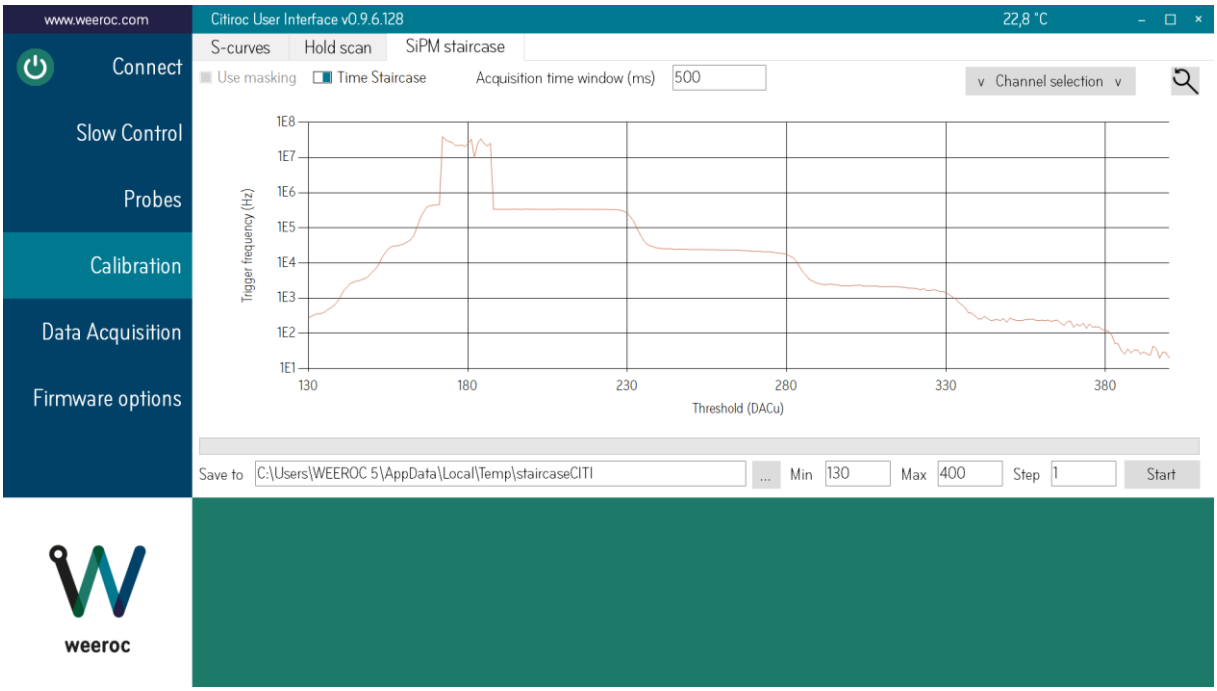

Figure 19 – Staircase on time trigger.

Those values can be used to choose the threshold value or to calibrate the gain of the 32 SiPM cells thanks to the input DACs.

When doing the staircase on a threshold, make sure that the other one is not in the pedestal or dark noise, as having high rate triggers will cause a lot of crosstalk noise during the measurement. If you are doing the staircase on the time threshold for example, put the charge threshold high enough so it doesn't trigger anything.

3.5 The data acquisition page

To start an acquisition, simply click on the "Start acquisition" button. On the top of the page can be set the number of acquisitions OR the acquisition time and the name of the output file, where the data will be saved.

Output data can be visualized in two different ways. If the number of acquisitions is very large (> 10 Go) the data won't be open in soft as this software is not developed to handle such large data. Large data set, depending on the performances of the computer, can take some time to be displayed. The output data file is constructed as shown on Figure 20.

hit0	ChargeLG0	ChargeHG0	hit1	ChargeLG1	ChargeHG1	...	hit31	ChargeLG31	ChargeHG31	temp
1	1171	3758	0	916	916	...	0	923	911	927
1	1174	3767	0	914	915	...	0	921	909	934
1	1174	3760	0	913	912	...	0	922	913	927
1	1174	3761	0	917	913	...	0	920	910	923
1	1177	3763	0	916	916	...	0	918	912	918

Figure 20 – Output data format.

The column are self-explanatory. The "hit" flag tells which channels have triggered the acquisition. ChargeLG is the low gain charge measurement and ChargeHG the high gain charge measurement. Each row corresponds to 1 acquisition. On the Figure 20, 5 acquisitions are represented. The "temp" data is given by a temperature sensor inside the ASIC.

The first way to visualize data in the software is "per channel". It displays the histograms of low gain and high gain charge for the whole bunch of acquisitions. The number of registered hit in the currently displayed channel is given on a label over the charts (Figure 21). By right-clicking the chart, the user has access to a context menu with a fit option (Gaussian only) to fit energy peaks. Chart data can also be exported to various output format (.txt, .xls, .csv or .xml). Note that the "load data" button only works with the output data format shown on Figure 20 and is used to load previous acquisitions data set in the software. Exports of the charts data will have to be opened in third-party software.

Figure 21 – "Per channel" data visualization. Photoelectron spectrum of a SiPM (pulsed LED).

An energy cut can be performed on the spectrum. This is very useful on the high gain charge measurement where a lot of saturated events can happen.

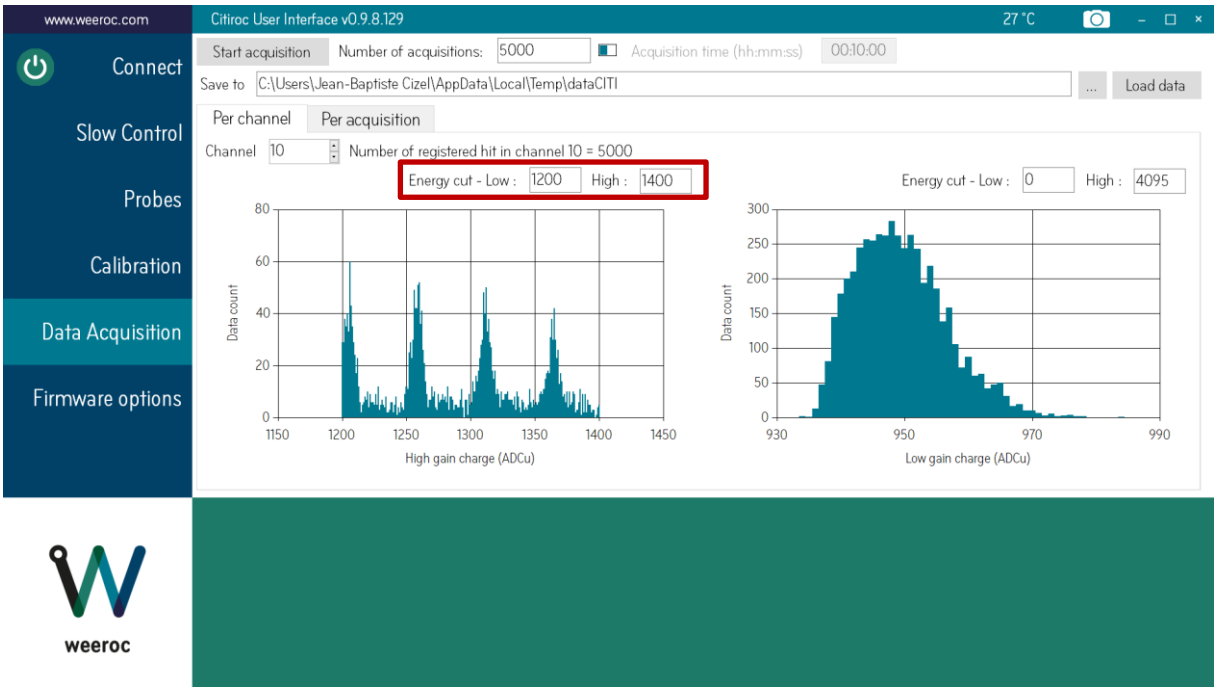

Figure 22 – Energy cut.

The visualization can also be done per acquisition (Figure 23). The two charge measurements are displayed for all the channels during a single acquisition. The acquisition number can be changed to browse through all the acquisitions. The bar will be red if the corresponding channel has registered a hit.

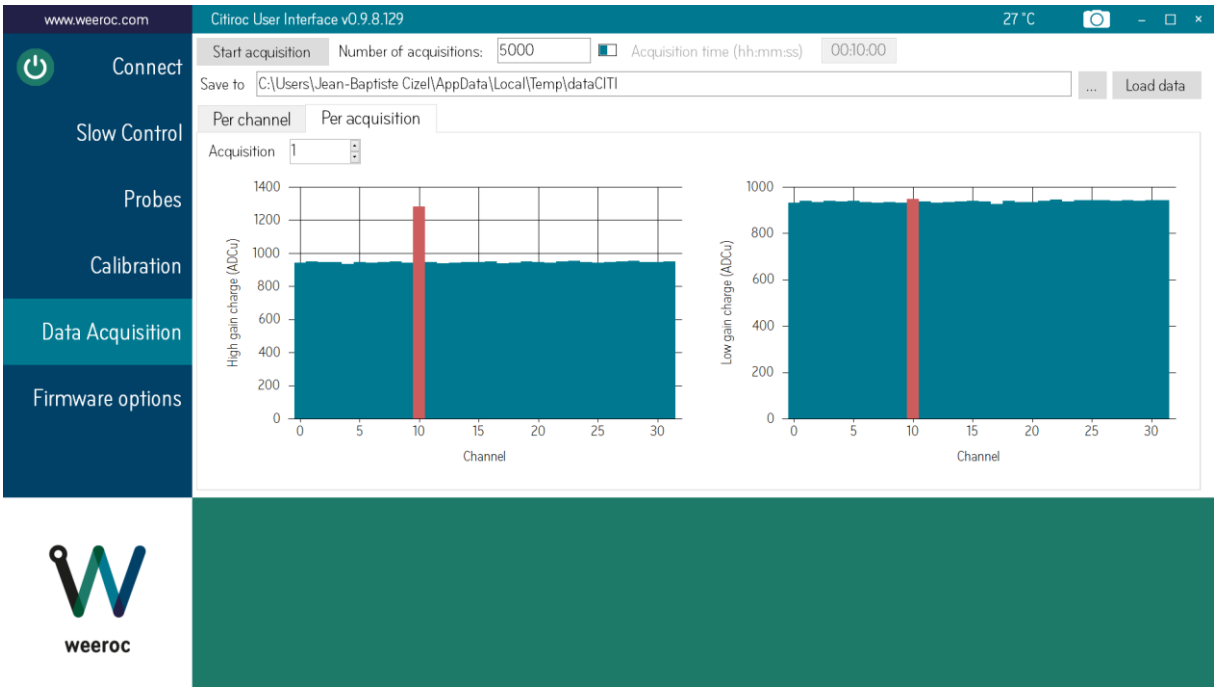

Figure 23 – "Per acquisition" data visualization. Red data in channel means a hit happened in that channel.

The elapsed acquisition time is given at the end of the acquisition on the top right corner. The dead time (DT) is also given and corresponds to the data processing time where the ASIC isn't working. On Figure 24 it is shown that on a 10 seconds acquisition there is about 12 % of dead time. This is the maximal dead-time since the ASIC is triggering at its maximal rate with a threshold below the pedestal. It is worth noting that the firmware send the acquisitions to the computer 100 by 100. It means that, in the case of the acquisitions on a certain amount of time, if the total of acquisitions when the timer stops is 5382 for example, the 82 last acquisitions will be lost.

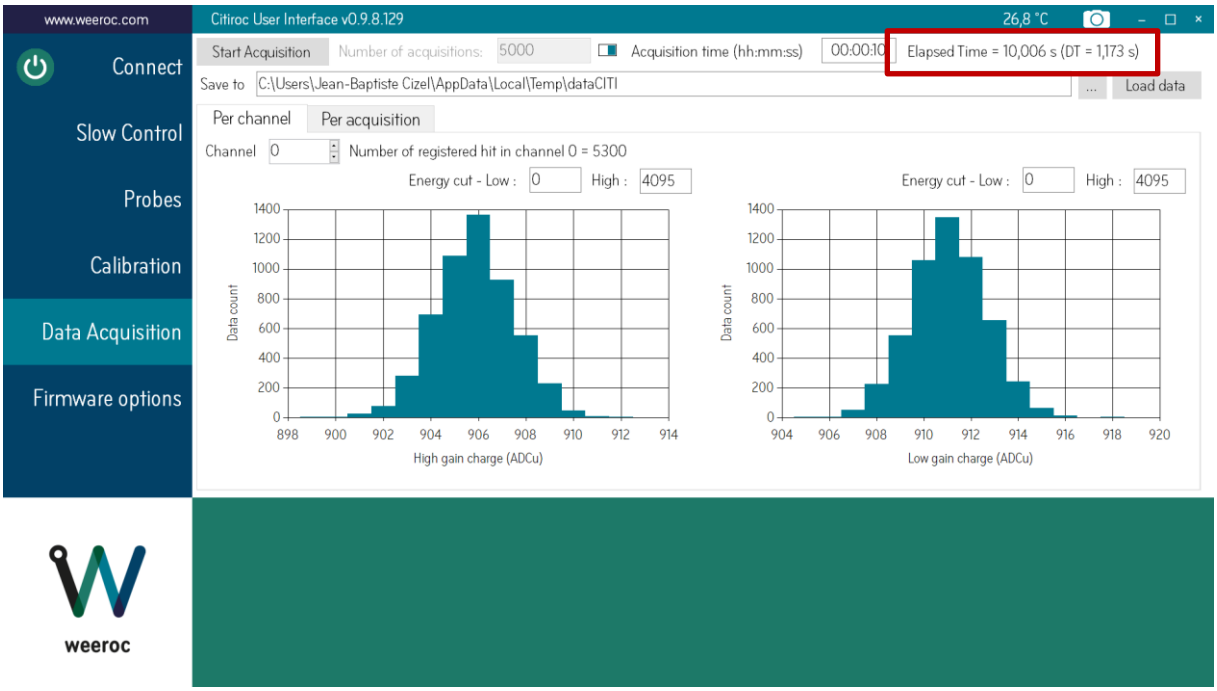

Figure 24 – Elapsed time and dead time

3.6 The firmware options page

Most of the settings on this page are reserved for advanced users. The most useful things for a standard use on this page are the trigger presets and the time trigger masking.

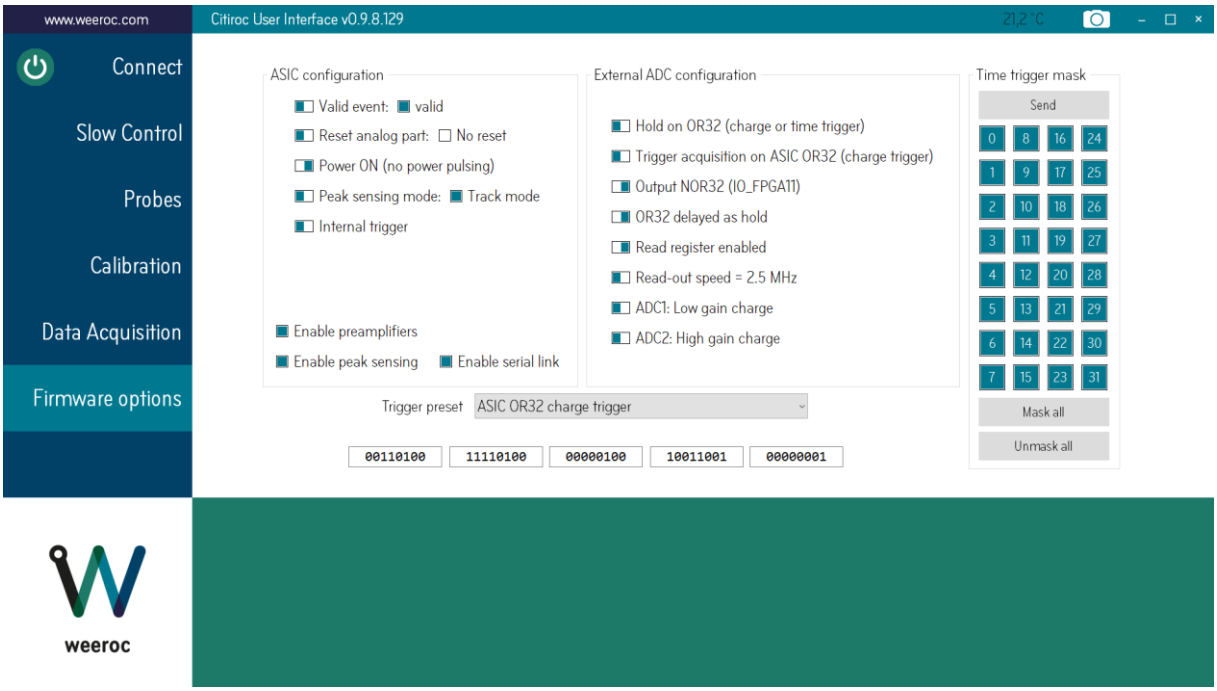

Figure 25 – Firmware options.

Since there is no trigger masking on the time trigger in the ASIC, the masking is done in the FPGA. The time trigger can be used as an external trigger to control the peak detector. When using the time trigger to trigger an acquisition without it being the external trigger, the peak detector and delay box will still rely on the charge trigger.

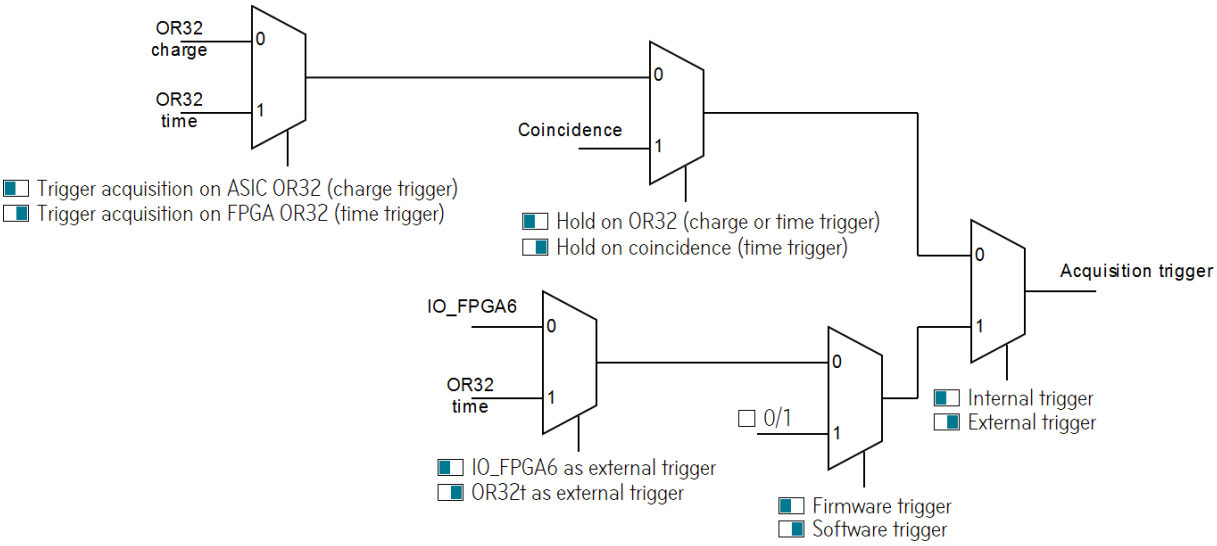

Figure 26 - Firmware trigger schematic

When using the external or internal trigger the corresponding slow control parameter on the slow control "Main Settings" tab must be set accordingly.

3.7 Setup to inject signals

3.7.1 Injection of a voltage step

First tests to be more familiar with the board and the software should be done using the following setup. A positive voltage step can be injected in one channel in series with a 100 pF capacitor to create a charge injection. A specific cable with a female "BERG" connector must be "homemade" to inject in each channel as the input connector is a male HE13 - 2x32pins. Alternatively the "IN_CALIB" input can be used for easier testing but the slow control need to be sent in order to take into account any change in the injected channel. The capacitance here is 3 pF and the signal doesn't go through the input capacitance of the voltage preamplifier.

The waveform of the injected signal is displayed Figure 21. A slow negative ramp allows to inject no significant signal in the ASIC before the next step. A voltage attenuator is needed to diminish the noise from the waveform generator. With a 100 pF injector, a 1.6 mV voltage step in a channel corresponds more or less to 1 photoelectron with a SiPM of gain $1{\cdot}10^6$.

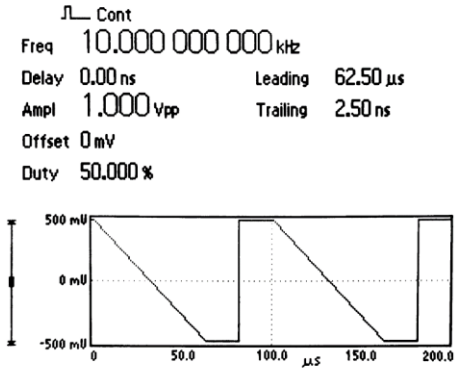

Figure 27 – Injection in each channel

You can then probe the output of the shapers using the "probes" page and check the waveform on the scope.

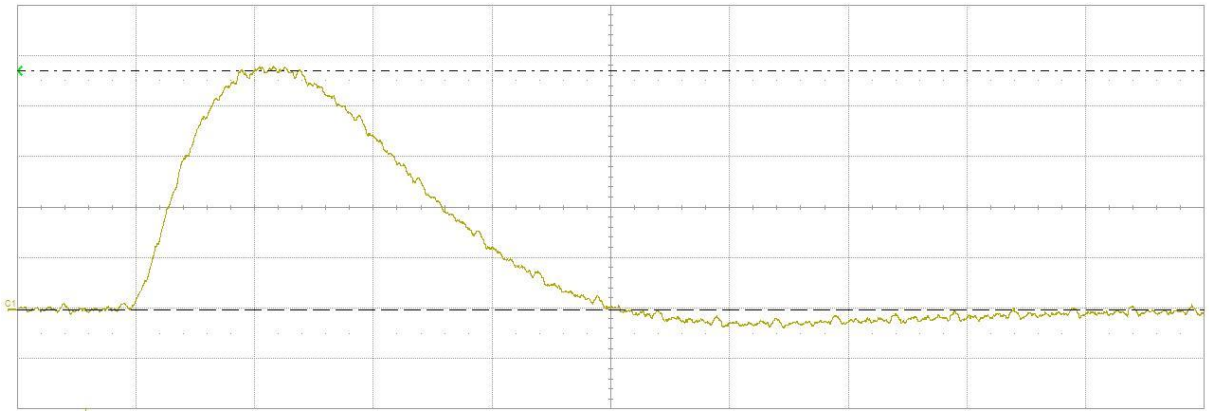

Figure 28 – Slow shaper output through the probe.

3.7.2 *Setup for SiPM connected to the PCB*

32 SiPMs (or SiPM array) can be connected directly to the evaluation board. Indeed, this board has been designed to host the detector and to simplify global setup.

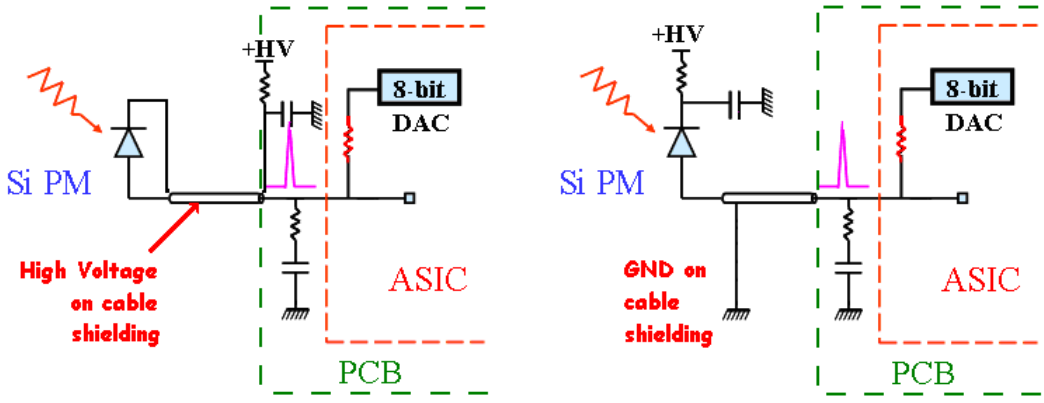

Figure 29 - 2 differents schemes of the SiPM connection to the ASIC

2 different setups can be implemented : High Voltage (HV) either local to the detector or distributed on cable shielding through the evaluation board and its connector J3 (female, DB-9). In both case, the SiPM(s) has to be plugged onto the connector J2 (male HE13 - 2x32pins). For each setup, individual High Voltage tuning is still available.

CAUTION: when the High Voltage is applied to the board/chip, check that the High Voltage has a slow ramp-up to avoid input-DAC destruction.

4 Appendix

4.1 S-curves

Two Gaussians are plotted on Figure 30. The red Gaussian stands for the noise probability density function around the pedestal of the signal with the average set at x = 0 and the standard deviation σ = 1. In the case of a perfect Gaussian distribution, the RMS noise corresponds to the standard deviation σ so here is represented a signal with a RMS noise of 1. The blue Gaussian represent a signal with a RMS noise of 1 and the signal over noise ratio is 10.

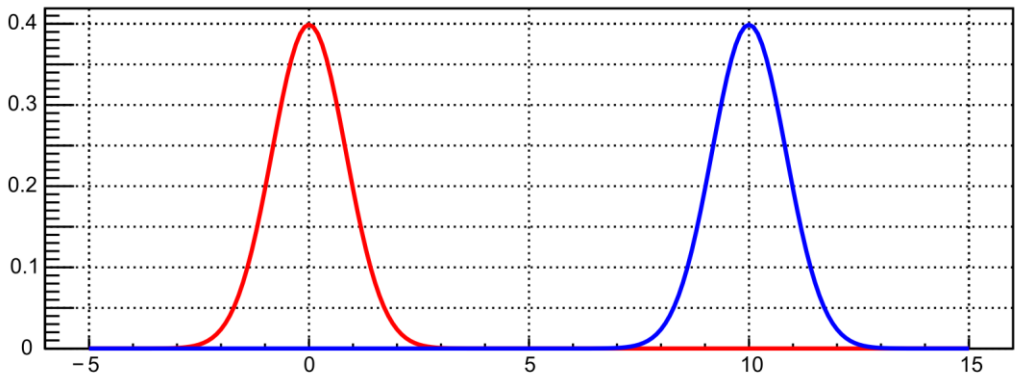

Figure 30 – Red : Normalized Gaussian with average = 0 and σ = 1 (arbitrary units). Blue : Normalized Gaussian with average = 10 and σ = 1.

By setting a threshold at x = 5 and by checking the position of the signals noise at a random time, the probability for the noise of the pedestal to be over the threshold is

$$0{,}5 \times \operatorname{erfc}\left(\frac{5}{\sqrt{2}}\right) = 2{,}8665 \cdot 10^{-7} \quad (1)$$

With *erfc()* the complementary error function. This result corresponds to one chance in 3.5 million. On the other hand the probability for the noise on the signal to be under the threshold is also 1/3.5M. The above equation is the complementary cumulative distribution function of the normal distribution evaluated at x = 5, μ = 0 and σ = 1. This function is written

$$S(x) = 0{,}5 \times \operatorname{erfc}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right) \quad (2)$$

With μ the mean (average of the signal or pedestal here) and σ the standard deviation (equivalent to the RMS noise). This function allows to evaluate the probability for an event to happen over a set threshold. The graphical representation of this function is shown on Figure 31.

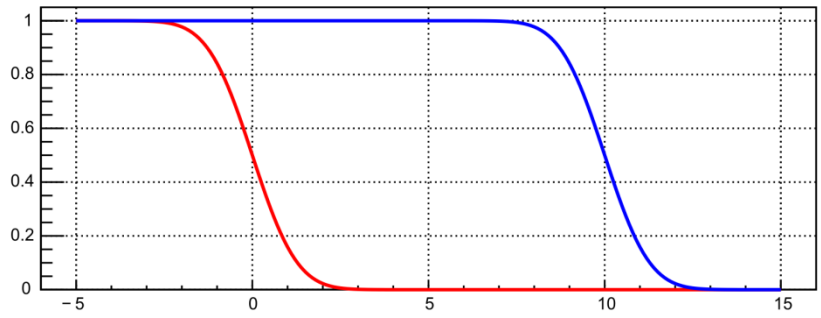

Figure 31 – S-curve representation of the signals shown on Figure 30.

This describes the probability to trigger on a discrete signal but concerning the pedestal it is a bit more complex because the trigger probability depends on the acquisition time as demonstrated on Figure 32 with a threshold at 5 whose trigger happens at the beginning and a threshold at 10 which triggers at 900 (arbitrary units).

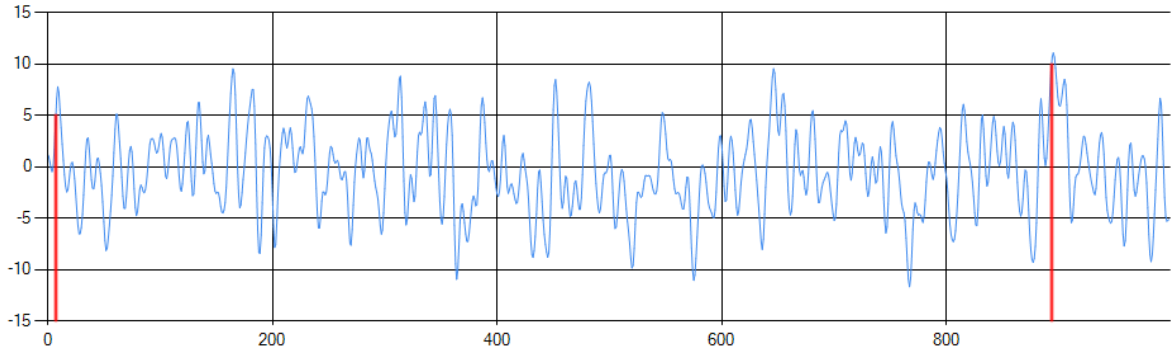

Figure 32

A study shown in *Mathematical Analysis of Random Noise* (Rice) give a zero-crossing frequency as

$$f_0 = 2\left[\frac{1}{3}\frac{f_b^3 - f_a^3}{f_b - f_a}\right]^{\frac{1}{2}} \quad (3)$$

With f_b and f_a high cut and low cut frequencies. In the case of an ideal CRRC bandpass filter the zero frequency is near 3 x f_c. Noise cross zero in both ascending and descending ways so the number of triggers on zero would be half the number of crossing. With a shaper central frequency of 5.3 MHz (shaping time of 30 ns), the number of triggers per seconds with a threshold at 0σ is N_0 = 1,5 x f_c = 7,95 M.

From P. Da Silva, «Élaboration d'un banc de tests pour l'électronique front-end du détecteur de particules MICROMEGAS pour l'expérience COMPASS.» (2000) it is known that the number of triggers on a threshold x during a time interval T is

$$N = N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \quad (4)$$

With N_0 = T x f_0 and μ the pedestal position. Supposing that this crossing number is a Poisson process, the probability to have k occurrences within T is as

$$P(k) = \frac{N^k e^{-N}}{k!} \tag{5}$$

Probability of having 0 events within T is

$$P(0) = e^{-N} \tag{6}$$

So the probability of having at least one event during T is

$$P(k \geq 1) = 1 - P(0) \tag{7}$$

$$P(k \geq 1) = 1 - e^{-N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \tag{8}$$

The noise trigger probability on a certain threshold within T is then

$$P(x) = 1 - e^{-N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \tag{9}$$

This is valid reasoning only in the case of a Gaussian distribution of noise. This study allows to plot the trigger efficiencies on pedestal for various acquisition window lengths (10 µs, 100 µs, 1 ms).

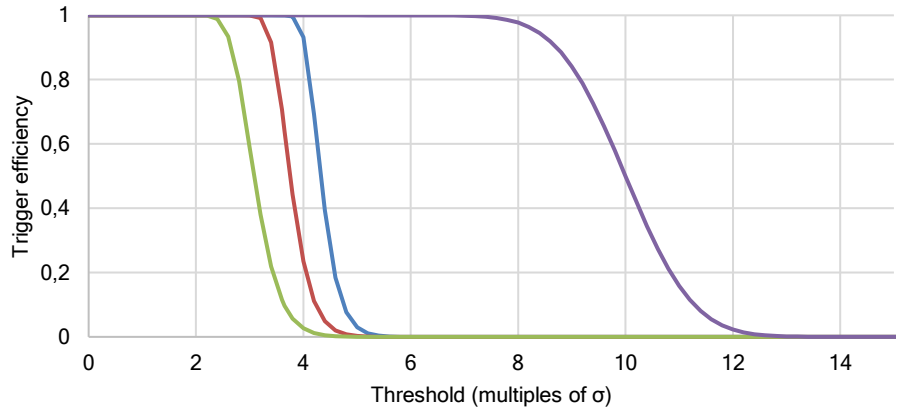

Figure 33 – Trigger efficiency on pedestal noise depending on threshold value for an acquisition window of 10 µs (green) ; 100 µs (red) and 1 ms (blue). Purple : S-curve of a signal with μ = 10 and σ = 1 (SNR = 10). The pedestal position is 0.

Hence having a wider acquisition window will shift the trigger efficiency along the x-axis in the case of the pedestal trigger efficiency acquisition.