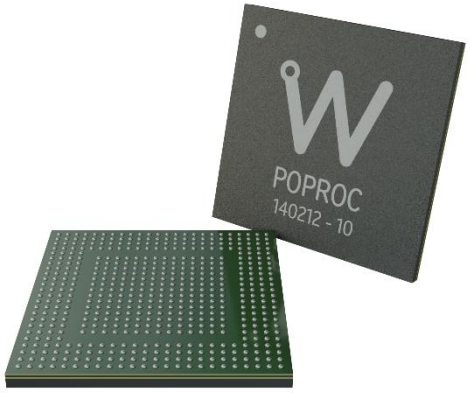
POPROC
TSMC 013G
V 0.1

POPROC is a MA-PMT readout out chip, specifically design for fast counting output. This chip is fully analog and features differential trigger output for each detector channel. The ASIC is designed to accept negative polarity input and can readout up to 64 channels.

POPROC allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 3 ns separated single photo-electrons). POPROC allows fast single photon counting over 300MHz per channel.

Channel-by-channel calibration on the trigger threshold is also possible thanks to 6-bit DACs.

POPROC features a GHz measurement line composed of a current conveyor followed by a fast discriminator and low swing differential output driver.



Detector Read-Out	PMT, MA-PMT
Number of Channels	64
Signal Polarity	Negative (selectable to work on Positive)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 3 ns double-peak separation on single photo-electron Over 300MHz photon counting rate
Dynamic Range	Over 100 photo-electrons
Packaging & Dimension	BGA 20x20 mm^2 Flip-Chip low inductance packaging technology
Power Consumption	210mW (TBC) – Supply voltage: 1.2 V
Inputs	64 analogue inputs
Outputs	64 differential (CLPS) triggers
Internal Programmable Features (I^2C)	trigger threshold programming (10bits), 64 x 6-bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp bandwidth adjustment, individual trigger masking.

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Maximum ratings

Ref.	Name	Description, comments or Ballout	Min.	Typ.	Max.	Unit
001	Operating Temperature	Asic operating temperature	-40	25	120	C
002	Power Supply	VDD, VDDI, DVDD	1.08	1.2	1.32	V
003	Ground	GND	0	0	0	V
004	Analog Inputs	IN<0:63>	0	-	1.5	V
005	Digital Inputs (Single ended)	POWER_ON, SDA, RESETB_i2C, CLK_SM_I2C, SCL, RSTB_SC, RSTB_PROBE, CHIP_ID<0:3>	0	-	1.5	V
006	Digital Inputs (Differential - Common Model)	VALEVENT_N/P	520	580	640	mV
007	Digital Inputs (Differential - Swing)	VALEVENT_N/P	300	410	410	mV
008	Digital Outputs (Single Ended)	ERROR_SC, SDA, SCL	1.08	1.2	1.32	V
009	Digital Outputs (Differential - Common Model)	TRIG<0:63>_n/p	520	580	640	mV
010	Digital Outputs (Differential - Swing)	TRIG<0:63>_n/p	300	410	410	mV

Table 1 - Maximum ratings

ASIC Architecture

The block diagram of the ASIC, shown in Figure 1, where the design is mostly consisting of full custom analog components. The only block containing digital standard cells is I2C slave core IP which is used for sending Slow Control[1] parameters. The ASIC has been designed to be optimized for reading out MA-PMT with negative polarity.

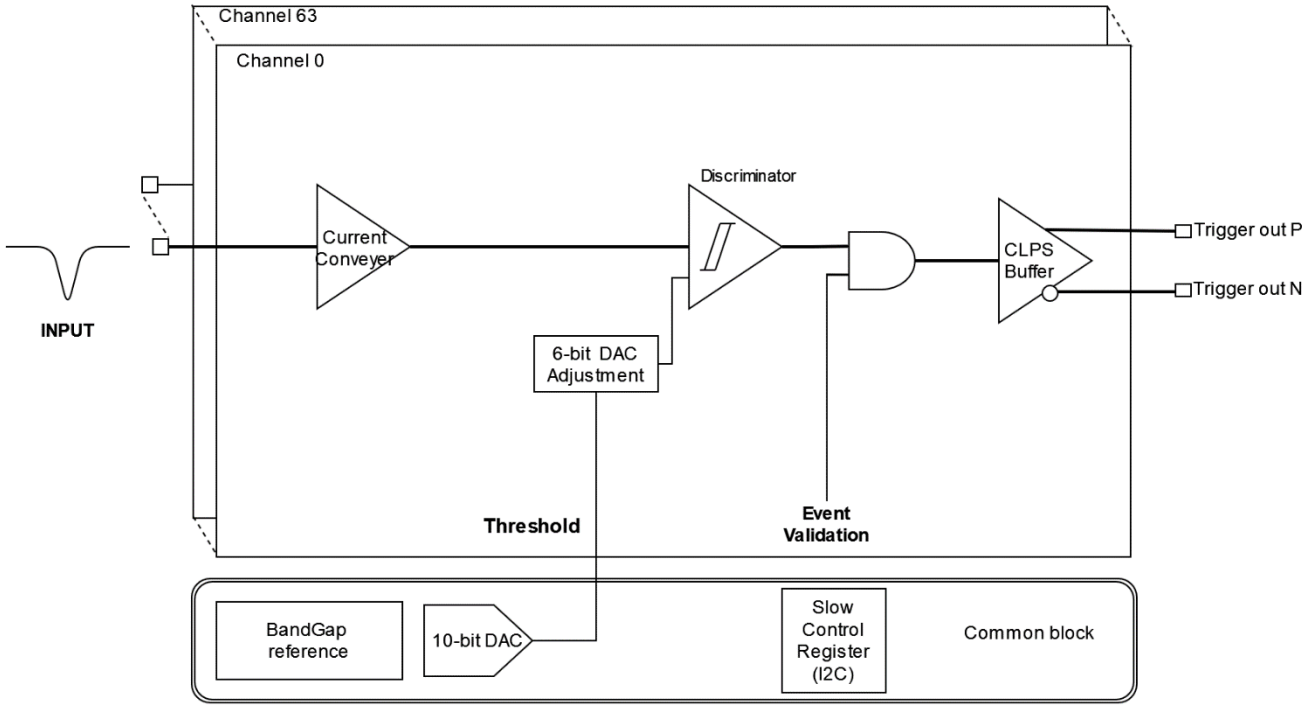

Figure 1 - ASIC block diagram

Power consumption & DC levels

Following DC levels are observed at the references and biasing point of POPROC :

Signal name	*Description*	*Sim @ 27°C*	*Sim @-40°C*	*Sim @125°C*
vbg	Bandgap output	0.621	0.621	0.621
Vref_1v	1V reference output	1.001	1	1
Vcp_probe	Probe amp P cascode	0.597	0.597	0.597
Vcn_probe	Probe amp N cascode	0.597	0.597	0.597
Vcasc_rx	LVDS receiver cascode	0.546	0.545	0.547
Vcasc_discri	Discriminator cascode	0.999	0.999	0.999
Vbias_1V	1V low impedance ref output	1.006	1.003	1.009
Ib_conv	Current conveyor bias	0.379	0.378	0.379
Ibo_probe	Output stage probe amp bias	0.809	0.773	0.857
Ibi_N_probe	Input stage probe amp bias	0.335	0.372	0.292
Ibi_P_probe	Input stage probe amp bias	0.817	0.781	0.865

[1] Slow Control stands for the register (TMR) storing the data for analog block parameters.

Ibo_discri	Output stage discriminator bias	0.192	0.219	0.162
Ibm1_discri	Medium stage discriminator bias	0.308	0.348	0.259
Ibm2_discri	Medium stage discriminator bias	0.308	0.348	0.259
Ibi_discri	Input stage discriminator bias	0.356	0.390	0.316
I_offset_discri	Hysteresis discriminator bias	0.355	0.390	0.315
Ib_10b_dac	Threshold DAC bias	0.657	0.614	0.707
Ibpi_amp_conv	Input stage current conveyor bias	0.631	0.600	0.679
Ibpi_conv	Input stage current conveyor bias	0.325	0.333	0.314
Ibpo_discri	Output stage Discriminator bias	0.549	0.540	0.561
Ibpm1_discri	Medium stage Discriminator bias	0.843	0.801	0.896
Ibpm2_discri	Medium stage Discriminator bias	0.843	0.802	0.896

Table 2 - DC points

Power consumption of static power (amplifier biasing) has been simulated at 146mA over 1.2V thus 175mW for the full chip at room temperature. Power consumption is 159mA (191mW) at -40°C and 149mA (179mW) at 125°C.

I²C configuration

This ASIC can be configured using I²C interface. The I²C slave core can be programmed using a custom I²C protocol that does not follow the IEEE standard. The I²C slave core has been designed with SEU mitigations in place.

Features of this IP are the following:

- Triplicated Design
- 256 addresses for the channel numbers
- 256 addresses for the register numbers
- 15 Chip ID numbers

The I²C slave core must receive a clock through the clk_sm_i2c port. This clock must have a frequency 20 times higher than the clock sent by the I²C master on the SCL line. These clocks must be synchronous.

Figure 2 and Table 3 describe the I²C slave core structure in the ASIC and the registers content.

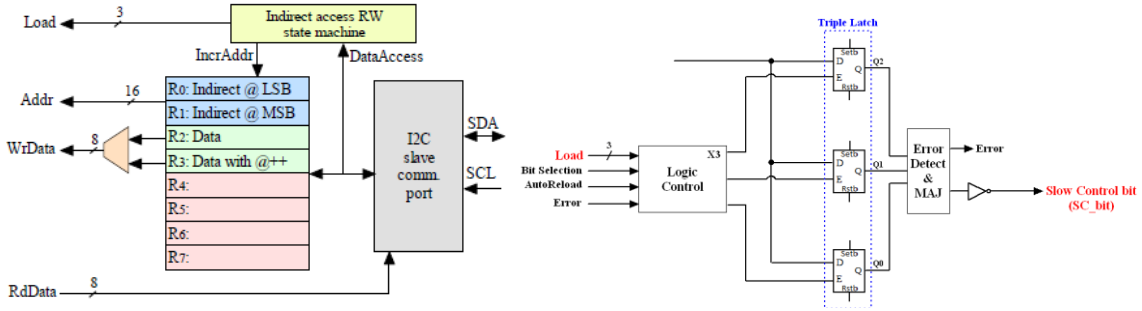

Figure 2 - Left: I2C slave core registers. Right: Slow Control bit cell design

I2C Address	Register
0	ASIC parameter address (LSB): Channel
1	ASIC parameter address (MSB): Register

2	Data Read/to Write
3	Data with auto-incremental Address
4-5-6	TBD
7	Status register (error, parity)

Table 1 - I2C slave core register descriptions

To address the Slow control parameters, the user can read or write each sub-address directly or it can use the auto increment feature that increments the sub-address based on the previous sub-address.

Figure 3 describes simple read and write I2C procedures. Such transfer is performed by sending 3 I2C frames of 16 bits as described in Figure 3. The full address to be sent is composed of the address and the sub-address of the slow control register, as described in Figure 4. The slow control registers associated addresses and sub-addresses can be found in Table 4.

Figure 5 shows a screenshot of an I²C write procedure to the slow control register with address 3 and sub-address 225.

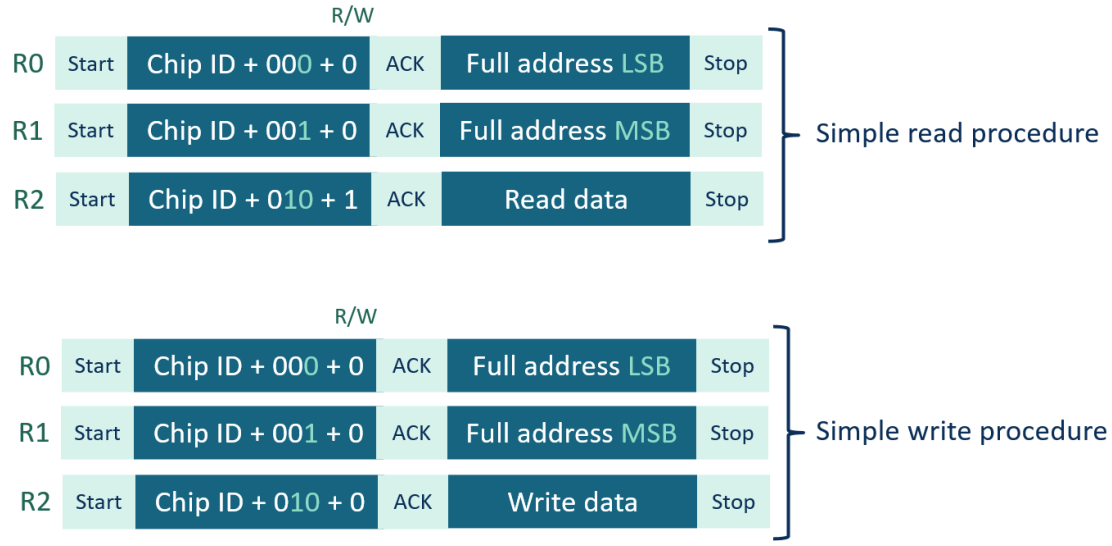

Figure 3 - Slow Control simple or direct parameter sub-addressing procedure

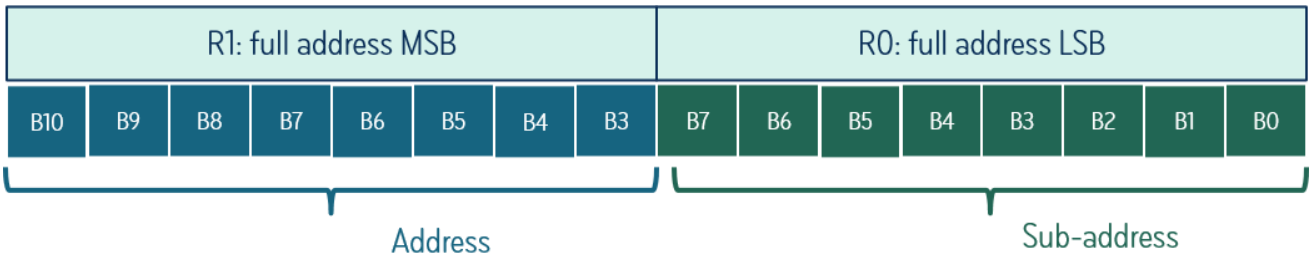

Figure 4 - Address and Sub-Address of the I²C register for setting the Slow Control of LirocvO

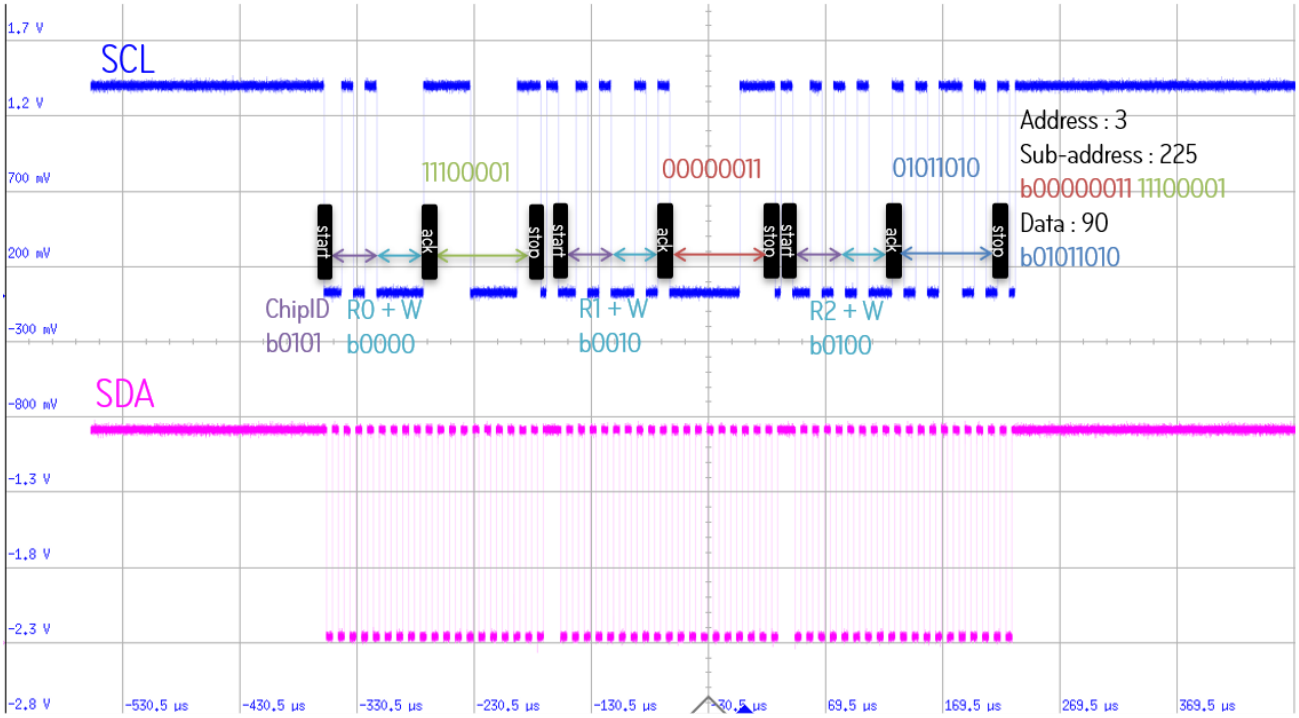

Figure 5 – SDA and SCL signals during an I²C write procedure of value 90 to address 3 sub-address 225

Slow control parameters available for this ASIC are listed in the Table 3. "NC" term denotes non used slow control bits. Data in "Address" and "Subadd" columns denote the "Full address" in R1 & R0 read/write sequences respectively (Figure 3). Data payload in R2 (direct parameter addressing - Figure 3) will be based on data in "Parameters/Default value" column.

Address	Subadd	Bit#	Default value	Name	Description
0-63	0	7-6	00	NC	Not connected
		5-0	100000	Dac_trim	Allow channel by channel threshold trimming. Default is mid-range
	1	7-3	00000	NC	Not connected
		2	0	Cmd_test	Injection capacitance connection switch. Default is switch open (0)
		1	0	Sw_input_clamp	Input Clamp switch state (in case of defective detector). Default is not clamped (0)
		0	0	Mask_disc	Trigger masking at discriminator stage. Default is not masked (0)
	99	7-2	0000000	NC	Not connected
		1	0	Probe_Vth	Connect channel {Address} threshold signal (Vth) to output probe. Default is disconnected (0)
		0	0	Probe_out_pa	Connect channel {Address} preamplifier output to output probe. Default is disconnected (0)
65	0	7	1	EN_bg	Enable bandgap bit. Default is enabled (1)
		6-1	100000	Bg(5:0)	Bandgap trimming value. Default is mid-range.
		0	0	NC	Not connected
	1	7	1	EN_10b_dac	Enable 10b threshold DAC. Default is enabled (1)
		6-3	0000	NC	Not connected
		2	1	Sign	Sign offset for threshold. Default is (1) for negative polarity input
		1-0	01	DAC<9:8>	MSB DAC values. Default is 01.
	2	7-0	00000000	DAC<7:0>	LSB DAC value. Default is 00000000.
	3	7	1	EN_pa	Enable preamplifiers. Default is enabled (1)
		6	1	PP_pa	Power pulsing preamplifiers. Default is on (1)
		5-0	010000	DAC_conv<5:0>	Preamplifier (Current Conveyor) bias trimming. Default is mid-range Range : 0~361uA. Step: 5.6uA. Default : 100uA
	4	7-6	00	NC	Not connected
		5-0	010000	DAC_amp_conv<5:0>	Preamplifier (Current Conveyor feedback amplifier) bias trimming. Default is first quarter

					Range : 0~400uA. Step: 6.25uA. Default : 104uA
	5	7	1	EN_discri	Enable discriminators. Default is enabled (1)
		6	1	PP_discri	Power pulsing discriminators. Default is enabled (1)
		5-0	010000	DAC_bias_discri	Discriminator bias trimming. Default is 010000.
	6	7	1	Cmd_hyst	Hysteresis toggle. Default is hysteresis enabled (1)
		6-3	1111	NC	Not connected
		2-0	000	Sw_cp<2:0>	Preamplifier bandwidth trimming
66	0	7-4	0010	EN-CLPS<3:0>	CLPS buffer size trimming. Default value is 0010
		3-0	0000	EN-pE<3:0>	CLPS pre-emphasis trimming. Default is 0000.
	1	7-6	00	S<1:0>	CLPS pre-emphasis delay trimming. Default is 00
		5-0	000000	NC	Not connected
	2	7	1	EN_Rx	Enable LVDS receiver for ValEvt
		6	0	PP_Rx	Power pulsing for LVDS receiver for ValEvt
		5	1	Forced_ValEvt	Bypass ValEvt
		4-0	00000	NC	Not connected
67	0	7	1	EN_probe	Enable analogue probe. Default is ON
		6	0	PP_probe	Power pulsing of analogue probe. Default is OFF
		5-3	000	NC	Not connected
		2-0	100	MillerComp	Probe amplifier compensation capacitance trimming. Default is 100. Range : 0 ~ 700fF. Step : 100fF. Default : 400fF
	1	7-6	10	Ibi_probe	Input bias of probe amplifier. Default is 10 "00" - 20uA "01" – 30uA "10" – 40uA "11" – 80uA
		5-0	100000	Ibo_probe	Output bias of probe amplifier. Default is 100000. Range : 0 ~ 38uA. Step : 0.6uA. Default : 20uA

Table 3 - Slow control list

Specifically, for Address 0-63, each subadd in this section will correspond only to the selected channel. This means that, in order to have all channels wide operation, each Address will have to be selected when writing the Slow Control operation. Otherwise, all the other Address (65-67) operations will be effective for the whole ASIC.

Pinout, Power supplies & mechanics

Mechanics

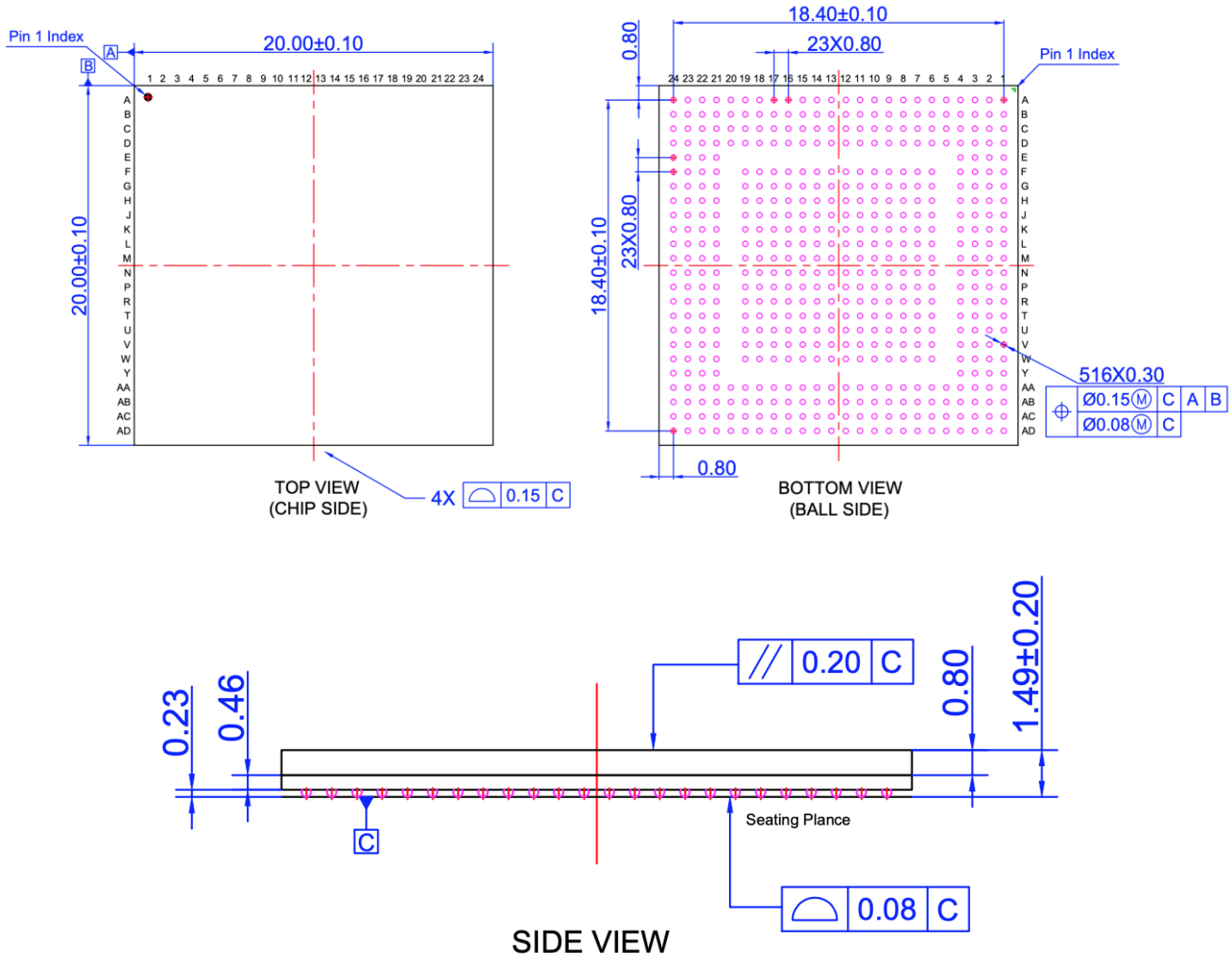

Figure 6 - BGA packaging mechanical outline

Altium Footprint

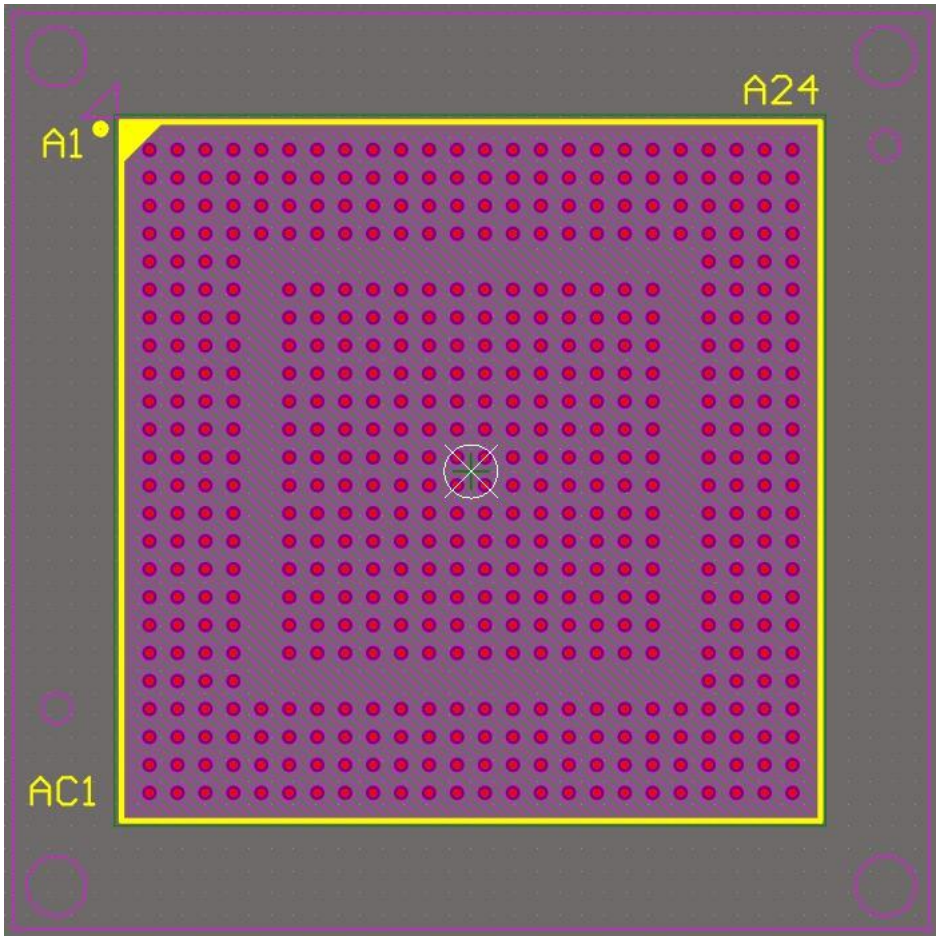

Figure 7 - Altium footprint

The footprint of the ASIC package is available for board design under Altium. The ballout follows the configuration in Figure 8 and Figure 9.

BGA package Ball-out

	1	2	3	4	5	6	7	8	9	10	11	12
A	IN<53>	IN<55>	IN<57>	IN<59>	IN<61>	IN<63>	IN<62>	power_on	sda	clk_sm_i2c	valevent_n	valevent_p
B	in<51>	in<52>	in<54>	in<56>	in<58>	in<60>	IN<64>	NC5	resetb_i2c	scl	vcasc_rx	GND
C	in<49>	in<50>	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND
D	in<47>	in<48>	ib_10b_dac	NC	NC	NC	NC	NC	NC	NC	NC	GND
E	in<45>	in<46>	i_offset_discri	NC								
F	in<43>	in<44>	vcasc_discri	NC		VDDI	VDDI	VDDI	VDD	VDD	VDD	GND
G	in<41>	in<42>	ibi_discri	NC		VDDI	VDDI	VDDI	VDD	VDD	VDD	GND
H	in<39>	in<40>	ibm1_discri	NC		VDD	VDD	NC	GND	GND	GND	GND
J	in<37>	in<38>	ibm2_discri	NC		VDD	VDD	NC	GND	GND	GND	GND
K	in<35>	in<36>	ibo_discri	NC		VDD	VDD	NC	GND	GND	GND	GND
L	in<33>	in<34>	ib_conv	NC		VDDI	VDDI	NC	GND	GND	GND	GND
M	analog_probe2	in<32>	vref_1v	NC		VDDI	VDDI	NC	GND	GND	GND	GND
N	analog_probe1	in<30>	vbias_1v	NC		VDDI	VDDI	NC	GND	GND	GND	GND
P	in<31>	in<28>	vbg	NC		VDDI	VDDI	NC	GND	GND	GND	GND
R	in<29>	in<26>	NC	NC		VDD	VDD	NC	GND	GND	GND	GND
T	in<27>	in<24>	NC	NC		VDD	VDD	NC	GND	GND	GND	GND
U	in<25>	in<22>	vcp_probe	NC		VDD	VDD	NC	GND	GND	GND	GND
V	in<23>	in<20>	vcn_probe	NC		VDDI	VDDI	VDDI	VDD	VDD	VDD	GND
W	in<21>	in<18>	ibi_p_probe	NC		VDDI	VDDI	VDDI	VDD	VDD	VDD	GND
Y	in<19>	in<16>	ibi_n_probe	NC								
Z	in<17>	in<14>	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND
AA	in<15>	in<12>	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND
AB	in<13>	in<10>	in<8>	in<6>	in<4>	in<2>	NC	NC0	NC	NC	NC	GND
AC	in<11>	in<9>	in<7>	in<5>	in<3>	in<1>	in<0>	reserved	in_ctest	NC2	NC3	rstb_sc
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 8 - POPROC Ball-out west part

12	13	14	15	16	17	18	19	20	21	22	23	24	
valevent_p	NC	NC	trig<62>_p	trig<62>_n	trig<63>_p	trig<63>_n	trig<61>_p	trig<61>_n	trig<52>_p	trig<52>_n	trig<53>_p	trig<53>_n	A
GND	NC	NC	trig<60>_p	trig<60>_n	trig<56>_p	trig<56>_n	trig<59>_p	trig<59>_n	trig<50>_p	trig<50>_n	trig<51>_p	trig<51>_n	B
GND	NC	NC	trig<58>_p	trig<58>_n	trig<54>_p	trig<54>_n	trig<57>_p	trig<57>_n	trig<48>_p	trig<48>_n	trig<49>_p	trig<49>_n	C
GND	NC	NC	NC	NC	NC	NC	trig<55>_p	trig<55>_n	trig<46>_p	trig<46>_n	trig<47>_p	trig<47>_n	D
									trig<44>_p	trig<44>_n	trig<45>_p	trig<45>_n	E
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		trig<42>_p	trig<42>_n	trig<43>_p	trig<43>_n	F
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		trig<40>_p	trig<40>_n	trig<41>_p	trig<41>_n	G
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<38>_p	trig<38>_n	trig<39>_p	trig<39>_n	H
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<36>_p	trig<36>_n	trig<37>_p	trig<37>_n	J
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<34>_p	trig<34>_n	trig<35>_p	trig<35>_n	K
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<32>_p	trig<32>_n	trig<33>_p	trig<33>_n	L
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	chip_id<0>	errorb_sc	M
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	chip_id<3>	chip_id<2>	chip_id<1>	N
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<30>_p	trig<30>_n	trig<31>_p	trig<31>_n	P
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<28>_p	trig<28>_n	trig<29>_p	trig<29>_n	R
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<26>_p	trig<26>_n	trig<27>_p	trig<27>_n	T
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig<24>_p	trig<24>_n	trig<25>_p	trig<25>_n	U
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		trig<22>_p	trig<22>_n	trig<23>_p	trig<23>_n	V
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		trig<20>_p	trig<20>_n	trig<21>_p	trig<21>_n	W
									trig<18>_p	trig<18>_n	trig<19>_p	trig<19>_n	Y
GND	NC	NC	NC	NC	NC	NC	trig<9>_p	trig<9>_n	trig<16>_p	trig<16>_n	trig<17>_p	trig<17>_n	Z
GND	NC	NC	trig<4>_p	trig<4>_n	trig<8>_p	trig<8>_n	trig<7>_p	trig<7>_n	trig<14>_p	trig<14>_n	trig<15>_p	trig<15>_n	AA
GND	NC	NC	trig<2>_p	trig<2>_n	trig<6>_p	trig<6>_n	trig<5>_p	trig<5>_n	trig<12>_p	trig<12>_n	trig<13>_p	trig<13>_n	AB
rstb_sc	rstb_probe	NC4	trig<0>_p	trig<0>_n	trig<1>_p	trig<1>_n	trig<3>_p	trig<3>_n	trig<10>_p	trig<10>_n	trig<11>_p	trig<11>_n	AC
12	13	14	15	16	17	18	19	20	21	22	23	24	

Figure 9 - POPROC ball-out East part

POPROC pinout

Net Name	BGA Ball	Type
ANALOG_PROBE1	N1	Bias
ANALOG_PROBE2	M1	
CHIP_ID<0>	M23	I/O Digital Single Ended
CHIP_ID<1>	N24	
CHIP_ID<2>	N23	
CHIP_ID<3>	N22	
	AC14	
CLK_SM_I2C	A10	
DVDD	F13	Power Supply - DVDD
DVDD	F14	
DVDD	F15	
DVDD	F16	
DVDD	F17	
DVDD	F18	
DVDD	F19	
DVDD	G13	
DVDD	G14	
DVDD	G15	
DVDD	G16	
DVDD	G17	
DVDD	G18	
DVDD	G19	
DVDD	H18	
DVDD	H19	
DVDD	J18	
DVDD	J19	
DVDD	K18	
DVDD	K19	
DVDD	L18	
DVDD	L19	
DVDD	M18	
DVDD	M19	
DVDD	N18	
DVDD	N19	
DVDD	P18	
DVDD	P19	
DVDD	R18	
DVDD	R19	
DVDD	T18	
DVDD	T19	
DVDD	U18	
DVDD	U19	
DVDD	V13	
DVDD	V14	
DVDD	V15	
DVDD	V16	
DVDD	V17	
DVDD	V18	
DVDD	V19	
DVDD	W13	
DVDD	W14	
DVDD	W15	
DVDD	W16	
DVDD	W17	
DVDD	W18	

DVDD	W19	
ERRORB_SC	M24	I/O Digital Single Ended
GND	AA12	Ground
GND	AB12	
GND	B12	
GND	C12	
GND	D12	
GND	F12	
GND	G12	
GND	H9	
GND	H10	
GND	H11	
GND	H12	
GND	H13	
GND	H14	
GND	H15	
GND	H16	
GND	H17	
GND	J9	
GND	J10	
GND	J11	
GND	J12	
GND	J13	
GND	J14	
GND	J15	
GND	J16	
GND	J17	
GND	K9	
GND	K10	
GND	K11	
GND	K12	
GND	K13	
GND	K14	
GND	K15	
GND	K16	
GND	K17	
GND	L9	
GND	L10	
GND	L11	
GND	L12	
GND	L13	
GND	L14	
GND	L15	
GND	L16	
GND	L17	
GND	M9	
GND	M10	
GND	M11	
GND	M12	
GND	M13	
GND	M14	
GND	M15	
GND	M16	
GND	M17	
GND	N9	
GND	N10	
GND	N11	

GND	N12	
GND	N13	
GND	N14	
GND	N15	
GND	N16	
GND	N17	
GND	P9	
GND	P10	
GND	P11	
GND	P12	
GND	P13	
GND	P14	
GND	P15	
GND	P16	
GND	P17	
GND	R9	
GND	R10	
GND	R11	
GND	R12	
GND	R13	
GND	R14	
GND	R15	
GND	R16	
GND	R17	
GND	T9	
GND	T10	
GND	T11	
GND	T12	
GND	T13	

GND	T14	
GND	T15	
GND	T16	
GND	T17	
GND	U9	
GND	U10	
GND	U11	
GND	U12	
GND	U13	
GND	U14	
GND	U15	
GND	U16	
GND	U17	
GND	V12	
GND	W12	
GND	Z12	
	AB8	Bias
	T3	
	C3	
IBI_N_PROBE	Y3	
IBM2_DISCRI	J3	
	Z3	
IBI_P_PROBE	W3	
I_OFFSET_DISCRI	E3	
	AC10	
	R3	
IBM1_DISCRI	H3	
	B8	
IBO_PROBE	D3	

	AC8	
	AB7	
IN<0>	AC7	Analog Input
IN<1>	AC6	
IN<2>	AB6	
IN<3>	AC5	
IN<4>	AB5	
IN<5>	AC4	
IN<6>	AB4	
IN<7>	AC3	
IN<8>	AB3	
IN<9>	AC2	
IN<10>	AB2	
IN<11>	AC1	
IN<12>	AA2	
IN<13>	AB1	
IN<14>	Z2	
IN<15>	AA1	
IN<16>	Y2	
IN<17>	Z1	
IN<18>	W2	
IN<19>	Y1	
IN<20>	V2	
IN<21>	W1	
IN<22>	U2	
IN<23>	V1	
IN<24>	T2	
IN<25>	U1	
IN<26>	R2	
IN<27>	T1	
IN<28>	P2	
IN<29>	R1	
IN<30>	N2	
IN<31>	P1	
IN<32>	M2	
IN<33>	L1	
IN<34>	L2	
IN<35>	K1	
IN<36>	K2	
IN<37>	J1	
IN<38>	J2	
IN<39>	H1	
IN<40>	H2	
IN<41>	G1	
IN<42>	G2	
IN<43>	F1	
IN<44>	F2	
IN<45>	E1	
IN<46>	E2	
IN<47>	D1	
IN<48>	D2	
IN<49>	C1	
IN<50>	C2	
IN<51>	B1	
IN<52>	B2	
IN<53>	A1	
IN<54>	B3	
IN<55>	A2	

IN<56>	B4	
IN<57>	A3	
IN<58>	B5	
IN<59>	A4	
IN<60>	B6	
IN<61>	A5	
IN<62>	A7	
IN<63>	A6	
IN<64>	B7	
IN_CTEST	AC9	Bias
VSASC_DISCRI	F3	
VDDI	F6	Power Supply - VDDI
VDDI	F7	
VDDI	F8	
VDDI	G6	
VDDI	G7	
VDDI	G8	
VDDI	L6	
VDDI	L7	
VDDI	M6	
VDDI	M7	
VDDI	N6	
VDDI	N7	
VDDI	P6	
VDDI	P7	
VDDI	V6	
VDDI	V7	
VDDI	V8	
VDDI	W6	
VDDI	W7	
VDDI	W8	
POWER_ON	A8	I/O Digital Single Ended
RSTB_PROBE	AC13	
SCL	B10	
RESETB_I2C	B9	
SDA	A9	
RESETB_SC	AC12	
	AC11	
TRIG_N<0>	AC16	I/O Digital Differential (1GHz)
TRIG_N<1>	AC18	
TRIG_N<2>	AB16	
TRIG_N<3>	AC20	
TRIG_N<4>	AA16	
TRIG_N<5>	AB20	
TRIG_N<6>	AB18	
TRIG_N<7>	AA20	
TRIG_N<8>	AA18	
TRIG_N<9>	Z20	
TRIG_N<10>	AC22	
TRIG_N<11>	AC24	
TRIG_N<12>	AB22	
TRIG_N<13>	AB24	
TRIG_N<14>	AA22	
TRIG_N<15>	AA24	
TRIG_N<16>	Z22	
TRIG_N<17>	Z24	
TRIG_N<18>	Y22	
TRIG_N<19>	Y24	

TRIG_N<20>	W22	
TRIG_N<21>	W24	
TRIG_N<22>	V22	
TRIG_N<23>	V24	
TRIG_N<24>	U22	
TRIG_N<25>	U24	
TRIG_N<26>	T22	
TRIG_N<27>	T24	
TRIG_N<28>	R22	
TRIG_N<29>	R24	
TRIG_N<30>	P22	
TRIG_N<31>	P24	
TRIG_N<32>	L22	
TRIG_N<33>	L24	
TRIG_N<34>	K22	
TRIG_N<35>	K24	
TRIG_N<36>	J22	
TRIG_N<37>	J24	
TRIG_N<38>	H22	
TRIG_N<39>	H24	
TRIG_N<40>	G22	
TRIG_N<41>	G24	
TRIG_N<42>	F22	
TRIG_N<43>	F24	
TRIG_N<44>	E22	
TRIG_N<45>	E24	
TRIG_N<46>	D22	
TRIG_N<47>	D24	
TRIG_N<48>	C22	
TRIG_N<49>	C24	
TRIG_N<50>	B22	
TRIG_N<51>	B24	
TRIG_N<52>	A22	
TRIG_N<53>	A24	
TRIG_N<54>	C18	
TRIG_N<55>	D20	
TRIG_N<56>	B18	
TRIG_N<57>	C20	
TRIG_N<58>	C16	
TRIG_N<59>	B20	
TRIG_N<60>	B16	
TRIG_N<61>	A20	
TRIG_N<62>	A16	
TRIG_N<63>	A18	
TRIG_P<0>	AC15	
TRIG_P<1>	AC17	
TRIG_P<2>	AB15	
TRIG_P<3>	AC19	
TRIG_P<4>	AA15	
TRIG_P<5>	AB19	
TRIG_P<6>	AB17	
TRIG_P<7>	AA19	
TRIG_P<8>	AA17	
TRIG_P<9>	Z19	
TRIG_P<10>	AC21	
TRIG_P<11>	AC23	
TRIG_P<12>	AB21	
TRIG_P<13>	AB23	

TRIG_P<14>	AA21	
TRIG_P<15>	AA23	
TRIG_P<16>	Z21	
TRIG_P<17>	Z23	
TRIG_P<18>	Y21	
TRIG_P<19>	Y23	
TRIG_P<20>	W21	
TRIG_P<21>	W23	
TRIG_P<22>	V21	
TRIG_P<23>	V23	
TRIG_P<24>	U21	
TRIG_P<25>	U23	
TRIG_P<26>	T21	
TRIG_P<27>	T23	
TRIG_P<28>	R21	
TRIG_P<29>	R23	
TRIG_P<30>	P21	
TRIG_P<31>	P23	
TRIG_P<32>	L21	
TRIG_P<33>	L23	
TRIG_P<34>	K21	
TRIG_P<35>	K23	
TRIG_P<36>	J21	
TRIG_P<37>	J23	
TRIG_P<38>	H21	
TRIG_P<39>	H23	
TRIG_P<40>	G21	
TRIG_P<41>	G23	
TRIG_P<42>	F21	
TRIG_P<43>	F23	
TRIG_P<44>	E21	
TRIG_P<45>	E23	
TRIG_P<46>	D21	
TRIG_P<47>	D23	
TRIG_P<48>	C21	
TRIG_P<49>	C23	
TRIG_P<50>	B21	
TRIG_P<51>	B23	
TRIG_P<52>	A21	
TRIG_P<53>	A23	
TRIG_P<54>	C17	
TRIG_P<55>	D19	
TRIG_P<56>	B17	
TRIG_P<57>	C19	
TRIG_P<58>	C15	
TRIG_P<59>	B19	
TRIG_P<60>	B15	
TRIG_P<61>	A19	
TRIG_P<62>	A15	
TRIG_P<63>	A17	
VALEVENT_N	A11	I/O Digital Differential (50MHz)
VALEVENT_P	A12	
VBG	P3	Bias
vbias_1v	N3	
IBI_DISCRI	G3	
VCASC_RX	B11	
VCN_PROBE	V3	
VCP_PROBE	U3	

	AA3	
VDD	F9	Power Supply - VDD
VDD	F10	
VDD	F11	
VDD	G9	
VDD	G10	
VDD	G11	
VDD	H6	
VDD	H7	
VDD	J6	
VDD	J7	
VDD	K6	
VDD	K7	
VDD	R6	
VDD	R7	
VDD	T6	
VDD	T7	
VDD	U6	
VDD	U7	
VDD	V9	
VDD	V10	
VDD	V11	
VDD	W9	
VDD	W10	
VDD	W11	
IBO_DISCRI	K3	Bias
IB_CONV	L3	
vref_1v	M3	

Table 4 - POPROC pin list

Power supply

The core of the ASIC is powered by 1.2V and power supplies are separated in several zone for reducing EMC influence from various section of the ASIC. It is recommended to at least separate the digital power supply from the analog power supply and to use decoupling capacitors for stabilizing & filtering the power supply. An example of power supply connection this is illustrated in Figure 10.

Pin Name	Pin Type	Description	Connected to
VDD	Power Supply	Analog power supply	1.2V
VDDI	Power Supply	Input stage power supply	1.2V
DVDD	Power Supply	Digital power supply	1.2V
GND	Ground	Ground	0

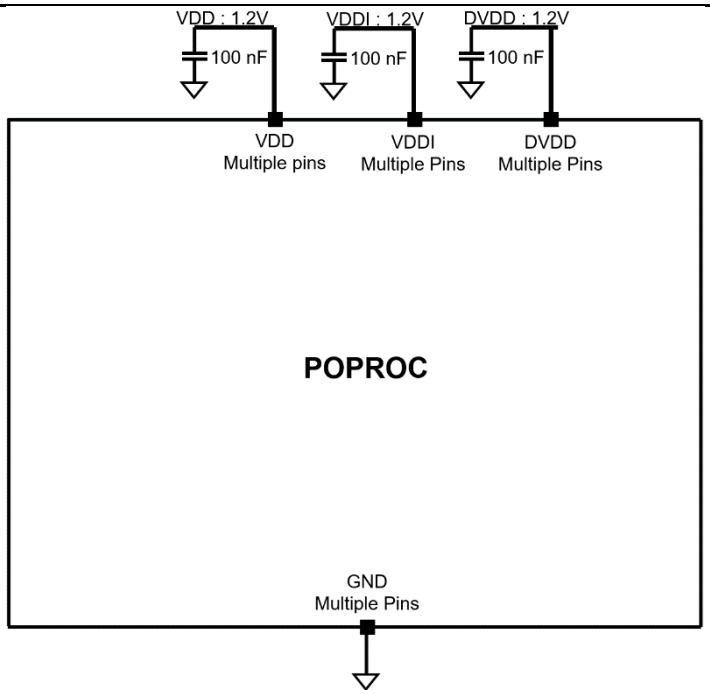

Figure 10 - POPROC power supplies connection

Input connection

The input pins are solely reserved for the detector inputs (MA-PMT). Short distance of traces for routing the input signal is highly recommended.

Pin Name	Ball Map	Description	Connected to
In<0:64>	Various location (refer to Table 4)	Connection to detector	Detector anodes

Biasing & debugging connections

Biasing pins are mostly optional I/Os which are available for debugging and analog section biasing modification if required. It could be left open or connected to decoupling capacitors in most cases. However, if a biasing modification is required, it is also possible to connect the pin to resistor-based voltage divider (refer Figure 11). The expected DC value of each pin can be found in Table 2. Additionally, the proposed connection for debugging pins (ANALOG_PROBE1/2 & IN_CTEST) is shown in Figure 12.

Pin Name	Ball Map	Description	Connected to
ANALOG_PROBE1	N1	Probe monitoring output for North side (channel 0 - 32)	Analog buffer & oscilloscope
ANALOG_PROBE2	M1	Probe monitoring output for South side (channel 33 - 63)	Analog buffer & oscilloscope
IBI_N_PROBE	Y3	Input stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
IBM2_DISCRI	J3	Medium stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBI_P_PROBE	W3	Input stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
I_OFFSET_DISCRI	E3	Hysteresis discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBM1_DISCRI	H3	Medium stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBO_PROBE	D3	Output stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
IN_CTEST	AC9	Charge injection input	Waveform generator or pulser
VCASC_DISCRI	F3	Discriminator cascode	Decoupling capacitor and/or voltage divider
VBG	P3	Bandgap output	Decoupling capacitor and/or voltage divider
VBIAS_1V	N3	1V low impedance ref output	Decoupling capacitor and/or voltage divider
IBI_DISCRI	G3	Input stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
VCASC_RX	B11	LVDS receiver cascode	Decoupling capacitor and/or voltage divider
VCN_PROBE	V3	Probe amp N cascode	Decoupling capacitor and/or voltage divider
VCP_PROBE	U3	Probe amp P cascode	Decoupling capacitor and/or voltage divider
IBO_DISCRI	K3	Output stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IB_CONV	L3	Current conveyor bias	Not connected, decoupling capacitor and/or voltage divider

VREF_1V	M3	1V reference output	Decoupling capacitor and/or voltage divider

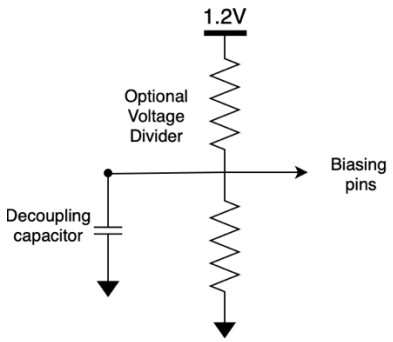

Figure 11 - Proposed connection for biasing points.

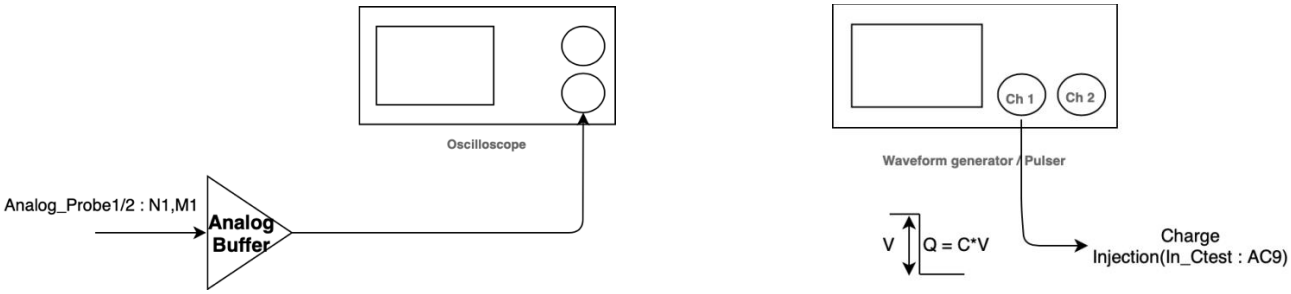

Figure 12 - Proposed connection for ANALOG_PROBE1/2 (Left figure) and IN_CTEST (Right figure)

Digital connections

The digital I/Os are divided into 4 types : open collector, single-ended, bidirectional and differential (CLPS[2]). The proposed connection for bidirectional and differential pins are shown in Figure 13 and for I2C, resets and trigger I/Os is shown in Figure 15. The pins are active high unless it is stated to be active low.

Pin Name	Ball Map	Description	Connected to
CHIP_ID<0:3>	M23,N24, N23, N22	Chip ID for I2C : Single Ended	FPGA
CLK_SM_I2C	A10	Clock for I2C slave core : Single Ended	FPGA
ERRORB_SC	M24	Bit flip error output, low level flag : Open Collector	FPGA with 47k Ohm pull up resistor to 1.2V
POWER_ON	A8	Power ON signal for sequentially powering on/off the whole ASIC : Single Ended	FPGA
RSTB_PROBE	AC13	Low level reset (min 50ns) for probe (analog debugging & signal monitoring) : Single Ended	FPGA
SCL	B10	SCL line for I2C	FGPA with 47k Ohm pull up resistor to 1.2V
RESETB_I2C	B9	Low level reset (min 50ns) for I2C slave core : Single Ended	FPGA
SDA	A9	SDA line for I2C : Bidir	FGPA with 47k Ohm pull up resistor to 1.2V
RESETB_SC	AC12	Low level reset (min 50ns) for Slow Control registers : Single Ended	FPGA
TRIG_N/P<0:63>	Various location (refer to Table 4)	Differential trigger outputs : CLPS	FPGA
VALEVENT_N/P	AA11, A12	Differential fast discriminator masking inputs : CLPS	FPGA

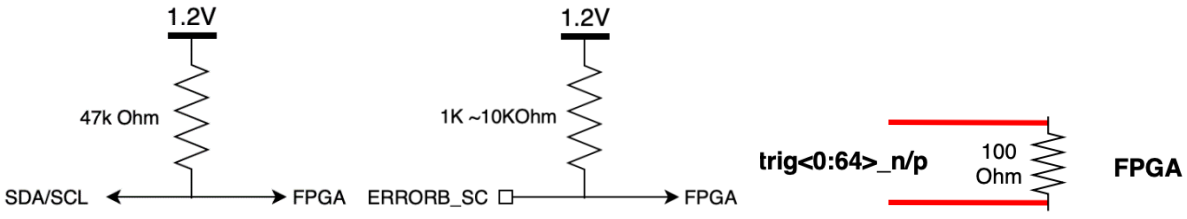

Figure 13 – Left : Proposed connection for SDA/SCL. Middle : ERROB_SC. Right : trig_n/p<0:64> differential connection.

[2] CLPS stand for CERN Low Power Signaling. It is not a fairly common digital I/Os standard. The common voltage is set at 0.6V with signal swing of 300mV.

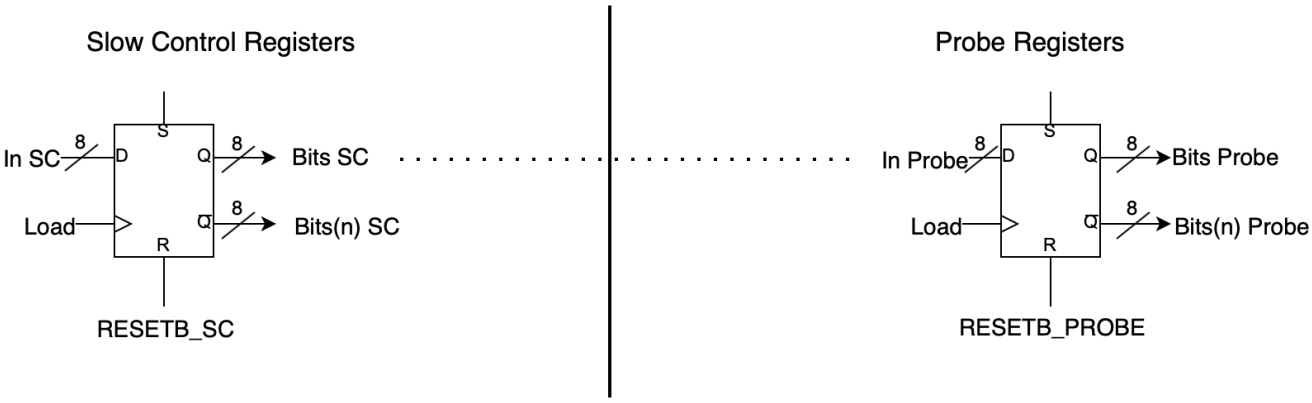

Figure 14 - Resets for Slow Control and Probe register separation

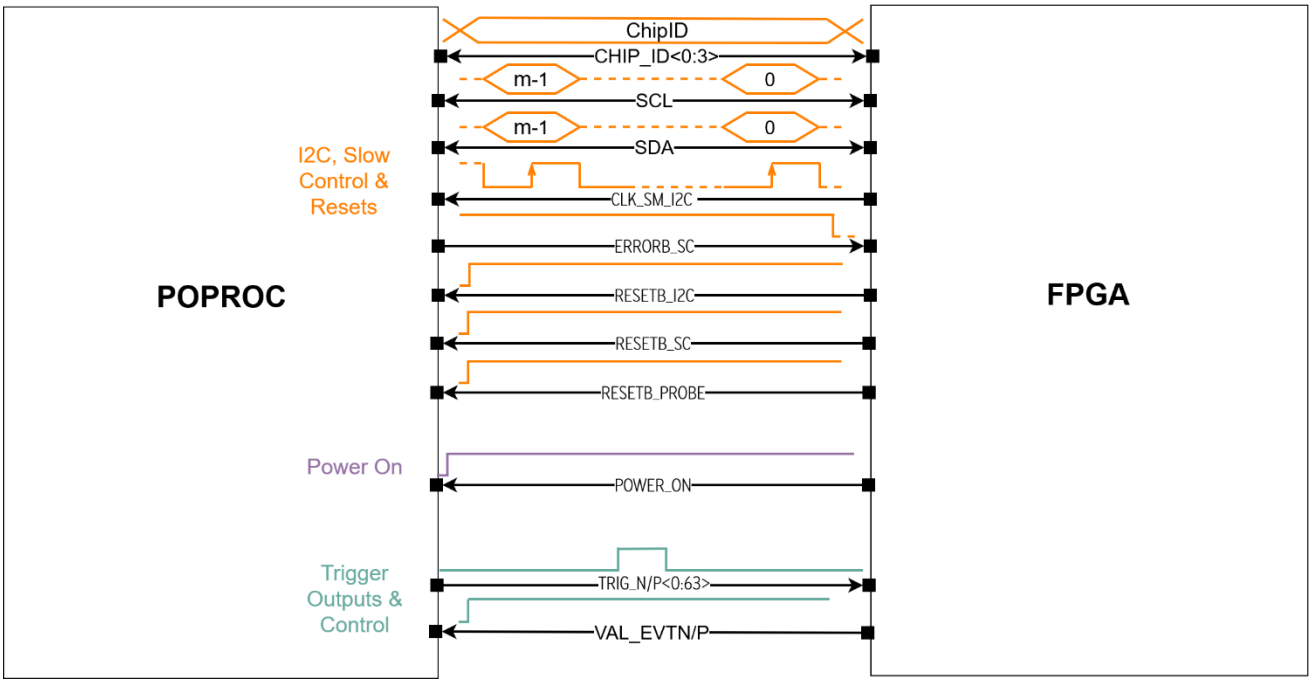

Figure 15 - Proposed connections for I2C, Reset and trigger I/Os

POPROC analog operation

The analog part of POPROC is composed of the dual polarity pre-amplifier followed by a discriminator for input signal discrimination and triggering. The threshold is set with 10-bit DAC (ASIC wide threshold) and followed with 6-bit trimming which is embedded in each channel. Simplified block diagram of the analog section is shown in Figure 16. The values reported in this section is the expected simulated values. The measured analog values are reported in Analog performances section.

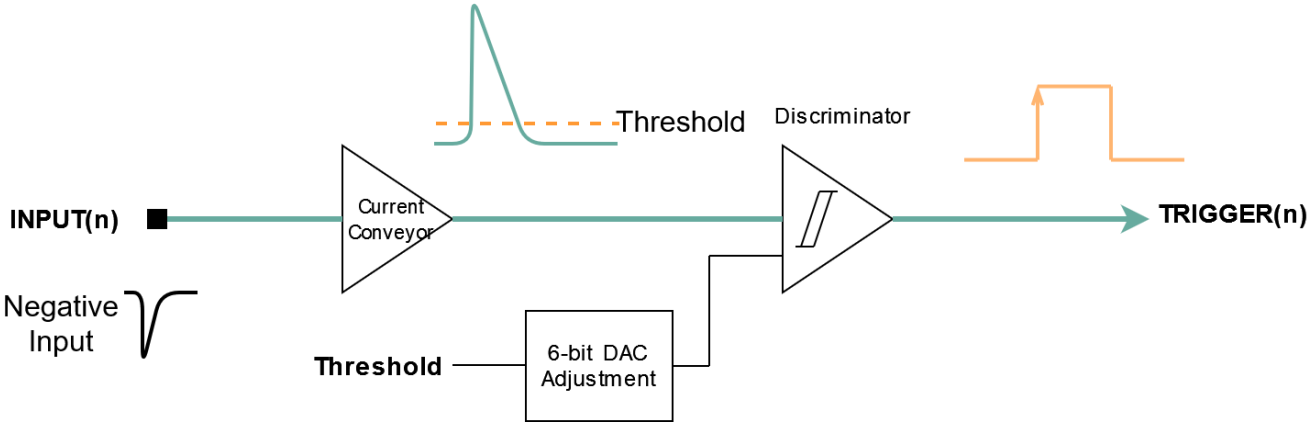

Figure 16 - Analog section block diagram.

The pre-amp employed here is common gate type or current amplifier. This pre-amplifier type will take current pulses from the input, and transform this signal into voltage through a resistor. The Slow Control setting available for this part will change the bandwidth of the pre-amplifier :

- Sw_cp<2:0> (Address: 65; Subadd : 6; Bits : 2-0). Range (default bias) : 220MHz@3dB ~ 648MHz@3dB. Default value (default bias) : 684MHz@3dB

The DC level of the pre-amplifier is about 600mV (with default setting) and the resulting DC level of the pre-amplifier will depend on the following Slow Control bits:

- DAC_conv<5:0> (Address: 65; Subadd : 3; Bits : 5-0). Range : 446mV ~ 825mV. Step ~6.5mV. Default value: 600mV

It should be noted "DAC_conv<5:0>" is a bias Slow Control, therefore setting this Slow Control bits will also affect the performance of this ASIC. Figure 17 illustrates the influence of this bias Slow Control settings to the pre-amplifier.

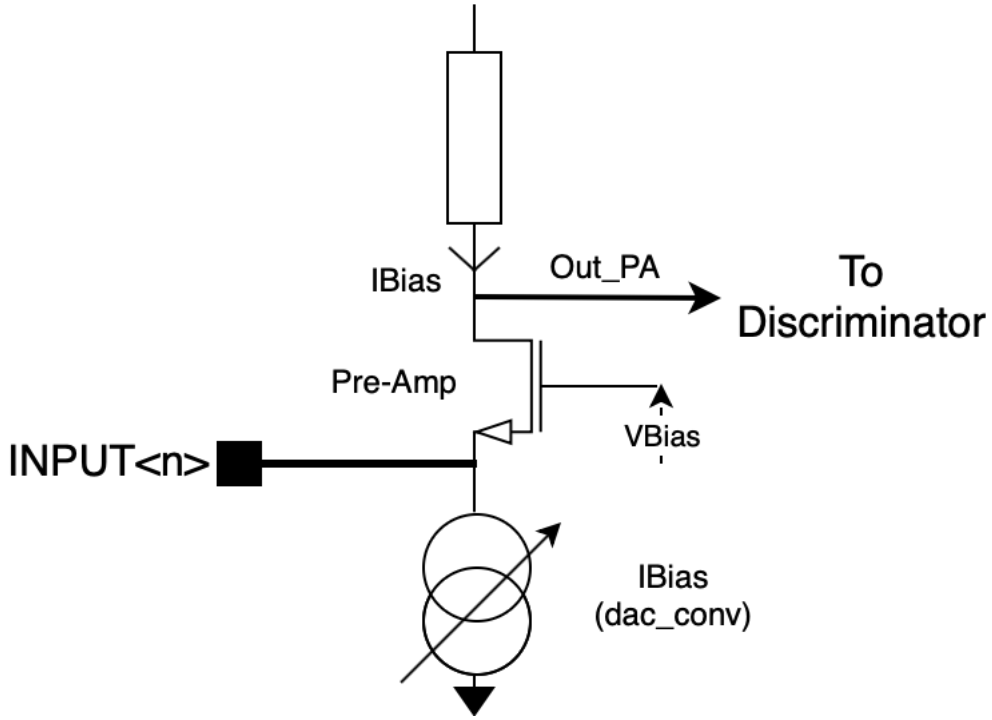

Figure 17 - Pre-amp block diagram with bias current

A 10-bit DAC used as a common threshold for the discriminator and the resulting output will depend on the on the input polarity configuration (refer to Slow Control bit "Sign" (Address: 65; Subadd : 1; Bits : 2)). The settings of this threshold are accessible through the following Slow Control bits:

- DAC<9:8> (Address: 65; Subadd : 1; Bits : 1-0) & DAC<7:0> (Address: 65; Subadd : 1; Bits : 7-0). Range (with default trim) : 595mV~898mV, Step :0.3mV, Default value : 692mV (with default trim) → Incremental configuration (refer to SC "Sign")
- DAC<9:8> (Address: 65; Subadd : 1; Bits : 1-0) & DAC<7:0> (Address: 65; Subadd : 1; Bits : 7-0). Range (with default trim) : 595mV~229mV, Step :0.3mV, Default value : 483mV (with default trim) → Decremental configuration (refer to SC "Sign")

Additionally, to fine tune this threshold, there is a 6-bit trimming which is available for each channel. The threshold after the trim will be the effective trigger threshold in each channel. This setting is accessible through the following Slow Control bits :

- Dac_trim (Address: 0-63; Subadd : 0; Bits : 5-0). Range : 0~216mV , Step : 3.5mV, Default value:123mV → Incremental configuration (refer to SC "Sign")
- Dac_trim (Address: 0-63; Subadd : 0; Bits : 5-0). Range : 0~268mV , Step : 4.2mV, Default value:157mV → Decremental configuration (refer to SC "Sign")

The discriminator embedded is a 3-stage discriminator designed for fast output response. A few settings are available for this discriminator. The first one is setting the threshold polarity based on the input signal, this setting can be done through the following Slow Control bit :

- Sign (Address: 65; Subadd : 1; Bits : 2). '0' decremental DAC value, '1' incremental DAC value.

This Slow Control bit will set the direction of DAC value. Depending on the setting, the resulting DAC value will increase or decrease with respect to the value applied to DAC <9:0> Slow Control bits. The direction of the DAC is illustrated in Figure 18.

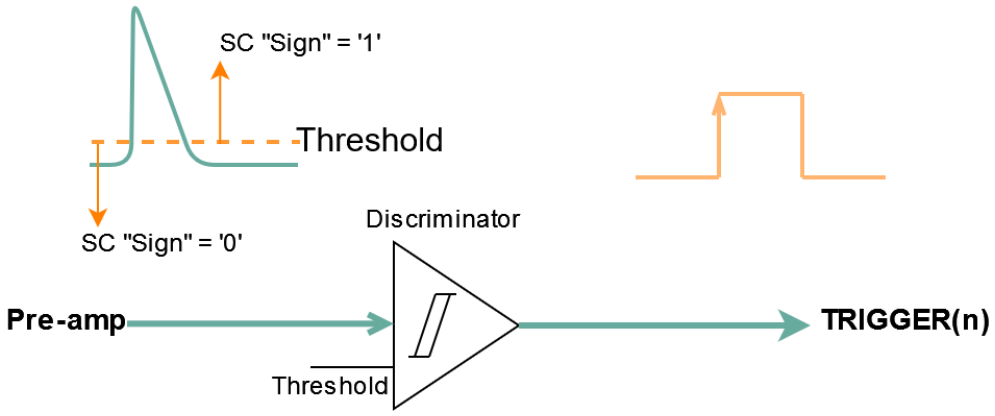

Figure 18 - Trigger threshold and discriminator output for positive et negative polarity input

The other features available is for controlling the discriminator output width. This option is available through the following Slow Control bits:

- DAC_bias_discri (Address: 65; Subadd : 5; Bits : 5-0). Range : 0.5ns ~3.1ns (TBC), Default value: 0.74ns (TBC)

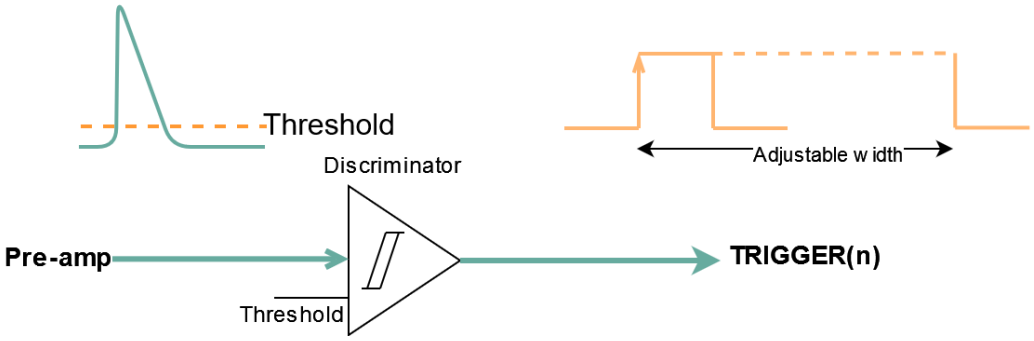

Figure 19 – Trigger output width adjustment

The last setting available for the discriminator is the output masking, and this setting is effective channel per channel. The Slow Control bit for this purpose is the following:

- Mask_discri (Address: 0-63; Subadd : 1; Bits : 0). '0' for no mask, '1' for mask.

In order to have ASIC wide trigger masking, an external signal has to be used instead. It is a differential input at the following pin :

- VALEVENT_N/P (Ball map : AA11/AA12) : Low Level for mask, High Level for no mask.

Other analog settings available are for charge injection, input clamping and CLPS differential driver tuning. For the charge injection, this Slow Control bit is used to enable or disable this part for each channel :

- Cmd_test (Address: 0-63; Subadd : 1; Bits : 2). '0' for disable charge injection, '1' for enable charge injection.

The charge injection has to be used in conjunction with a dedicated ASIC input, available at the following pin :

- In_Ctest (Ball map : AC9) : Low Level for negative polarity charge injection, High Level for positive polarity charge injection.

The input clamping setting, also for each channel, is available at the following Slow Control bits :

- Sw_input_clamp (Address: 0-63; Subadd : 1; Bits : 1). '0' for disable input clamp '1' for enable input clamp.

For the differential output driver, users can control the buffer size (EN-CLPS<3:0>, setting overall amplitude), pre-emphasis (EN-pE<3:0>, for edge slope) and pre-emphasis delay (S<1:0>, setting the delay for reaching the transmission amplitude) at the following Slow Control bits:

- EN-CLPS <3:0> (Address: 67; Subadd : 0; Bits : 7-4). Range : 58mV ~ 348mV, Step : 19mV, Default value:348 mV
- EN-pE <3:0> (Address: 67; Subadd : 0; Bits : 3-0). Range : 536MV/s ~831MV/s , Step : 18.5MV/s, Default value:748MV/s
- S<1:0> (Address: 67; Subadd : 1; Bits : 7-6). "00" : 122ps; "01" :252ps; "10"|"11" :377ps. Default value : 377ps

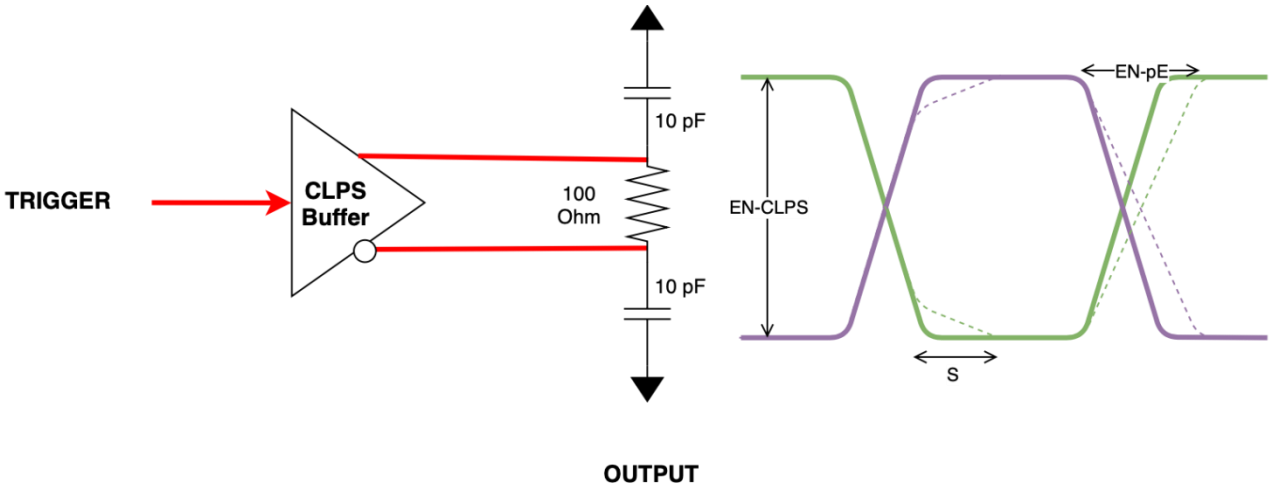

Figure 20 - Setting for CLPS differential buffer outputs

POPROC floorplan & packaging

Preliminary mechanics give a naked die size of 4.72mm*11.12mm including scribe line giving a die area of 52.5 mm2. The ASIC has 516 bump pads which will be bonded to BGA substrate.

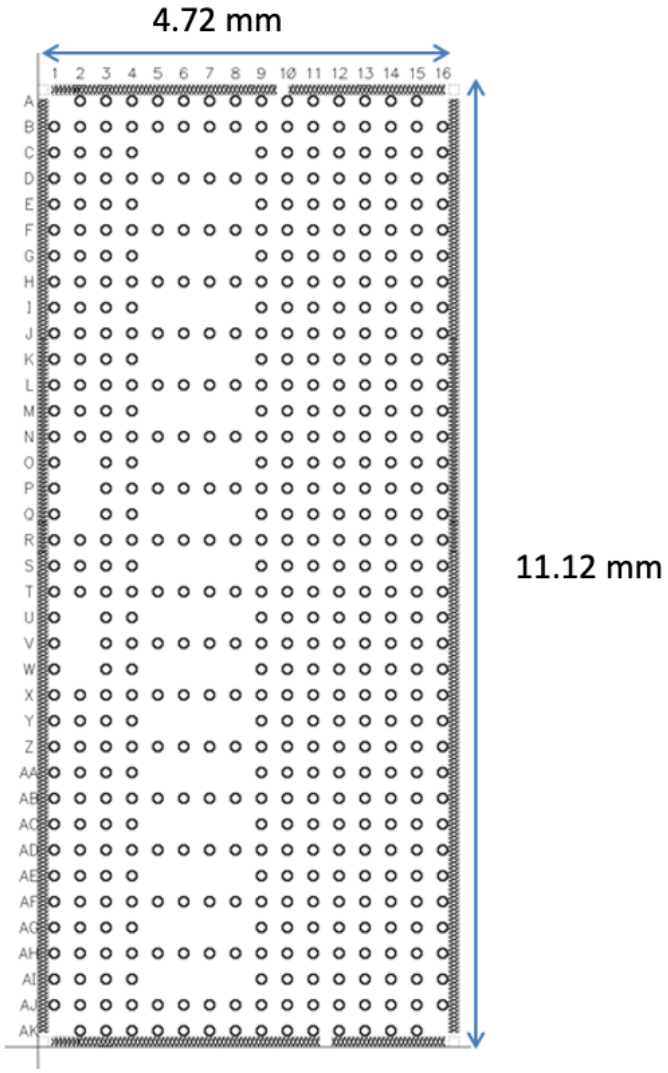

Figure 21 - Padring and ASIC form factor

Analog performances

Several analog static measurements have been performed for the trigger threshold (Figure 22), threshold trimming (Figure 23), pre-amp biasing setting (Figure 24), input impedance (Figure 25) and reference voltage trimming (Figure 24).

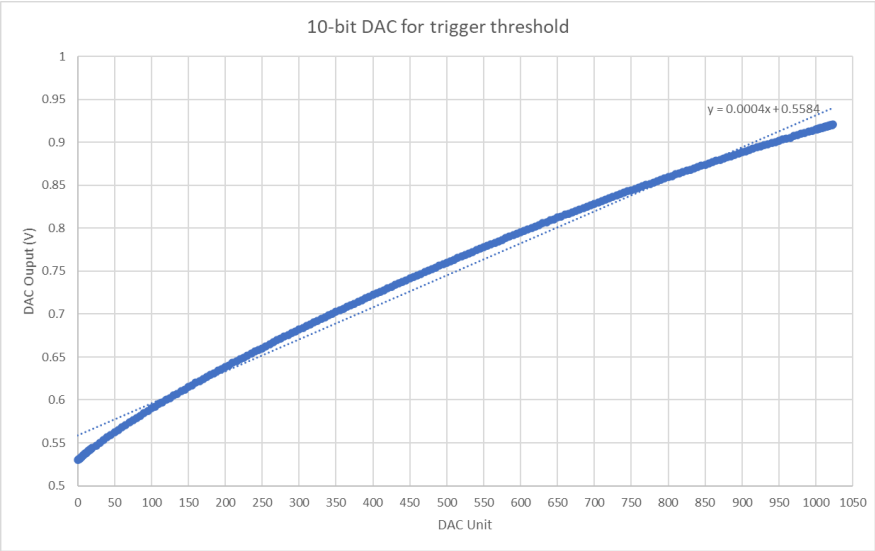

Figure 22 - 10-bit DAC output for trigger threshold

As shown in Figure 22, the 10-bit DAC used for setting the threshold can be set from 0.53 to 0.9207 V with a step of 0.4mV. In each channel, 6-bit threshold trimming is available and it is reported in the following figure.

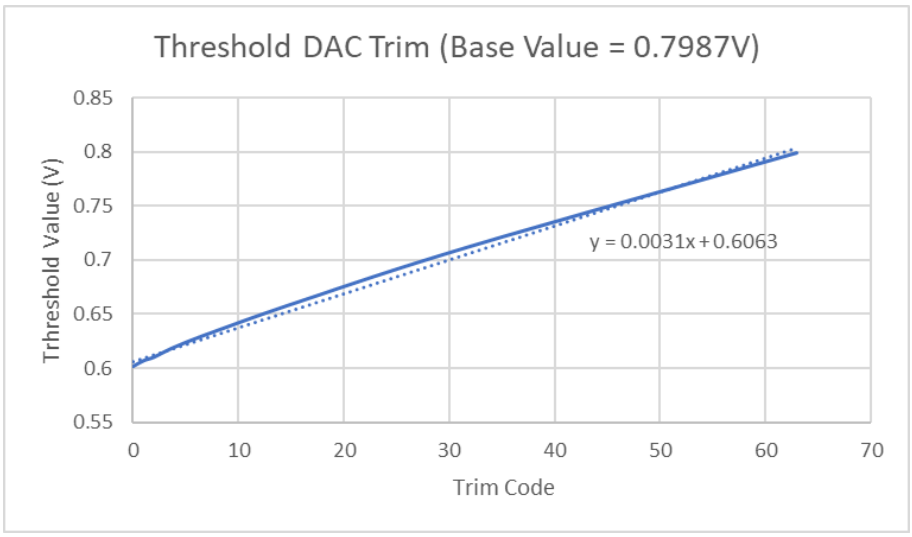

Figure 23 - Trigger Threshold DAC trimming

As shown in Figure 23, the trim is performed for threshold base value of 0.7989V or 256 DAC Unit. The trimming has a voltage span of 198mV with a step of 3.1mV.

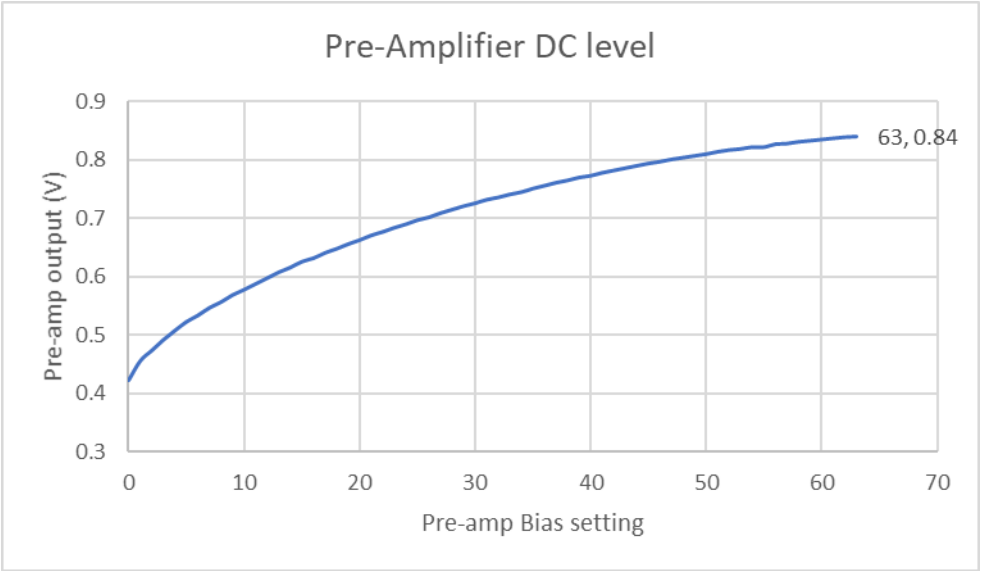

Figure 24 - Pre-amp DC level output versus bias setting

Figure 24 shows the pre-amplifier DC level versus its bias trimming setting. The minimum value could be set is about 0.423V and the maximum value is about 0.84V. For the recommended trimming setting (DAC_conv<5:0> (Address: 65; Subadd : 3; Bits : 5-0) = "01 0000"), the pre-amp DC value is expected to be about 0.632V. It should be noted that this value does not take into account dispersions between all channels.

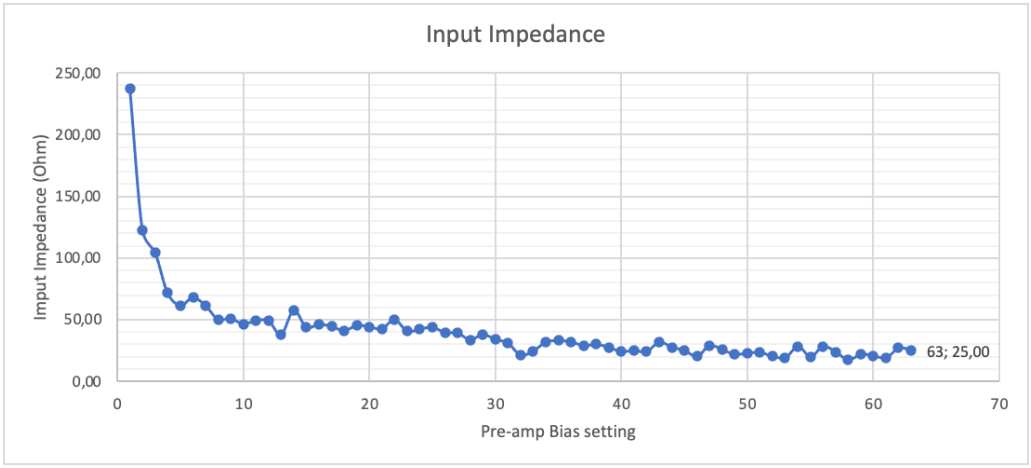

Figure 25 - Input Impedance versus pre-amplifier bias setting

With the same settings applied to the pre-amplifier, the resulting input impedance has been measured and represented in Figure 25. Based on the setting applied, the resulting input impedance varies from 237 Ohm to 25 Ohm. It should be noted the that the resulting input impedance is slightly lower than the expected value, 10-20 Ohm less than the simulated starting from pre-amplifier bias setting (DAC_conv<5:0> (Address: 65; Subadd : 3; Bits : 5-0)) = "00 1010". For the recommend setting of the pre-amplifier bias setting (DAC_conv<5:0> (Address: 65; Subadd : 3; Bits : 5-0) = "01 0000"), the input impedance is about 50 Ohm.

For both measurements in Figure 24 and Figure 25, it have been done with pre-amplifier feedback setting (DAC_amp_conv<5:0> (Address: 65; Subadd : 4; Bits : 5-0)) = "00 0011".

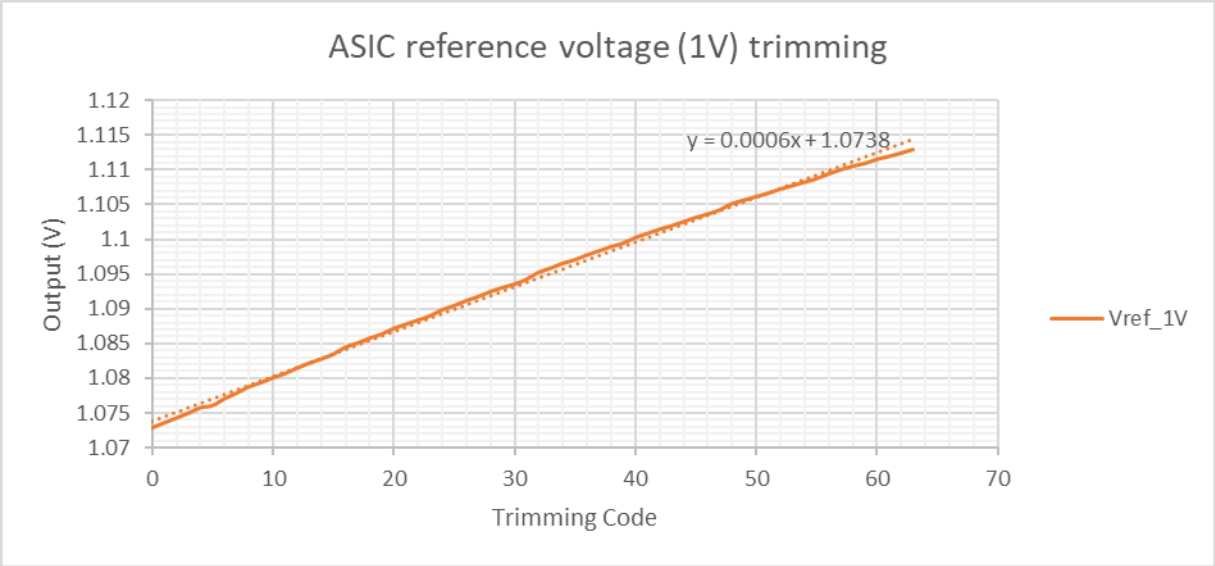

Figure 26 - ASIC reference voltage (1V) trimming

For setting up the biasing stage of the ASIC, a 1V reference value is used and can be trimmed as shown in Figure 26. The trim ranges from 1.0728 to 1.1129 with a step of 0.6 mV. The 1V reference voltage is generated a bandgap which yields a value of about 0.683V in room temperature. The measurement of this Bandgap reference versus temperature (-20°C to 12°C) is represented in Figure 27.

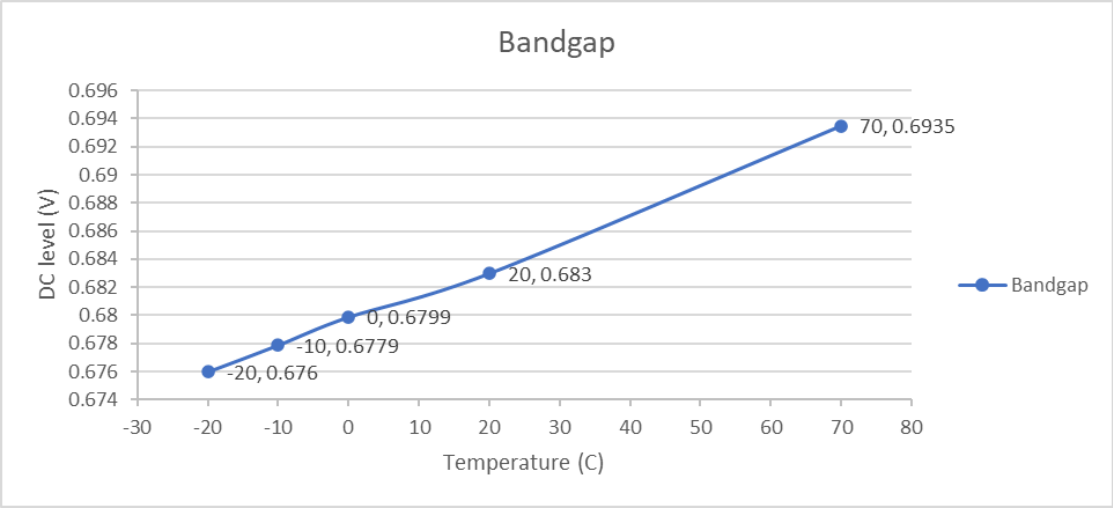

Figure 27 – Bandgap voltage for temperature range from -20°C to 70°C

For transmitting the trigger outputs, this ASIC employs CLPS differential buffers. Its differential voltage swing can be set as shown in Figure 28 and Figure 29.

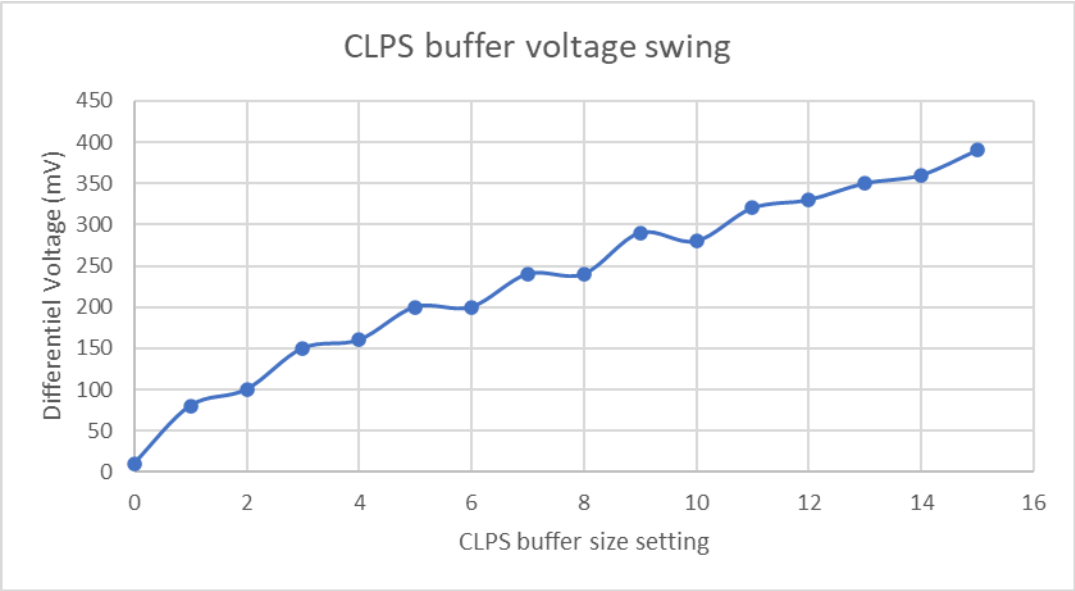

Figure 28 – CLPS buffer differential output versus buffer size setting

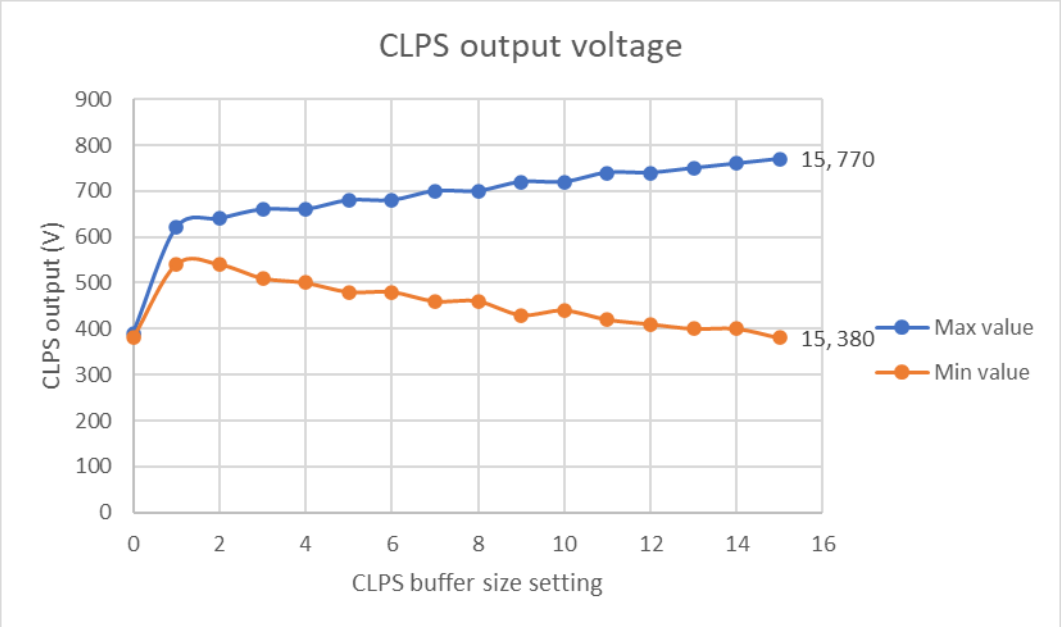

Figure 29 – CLPS min and max output loaded in 100 Ohm versus buffer size setting

As shown in the measurement results, the differential buffers can be set to output from 10 mV up to 390mV of differential voltage swing. The common mode is slightly below 600 mV.

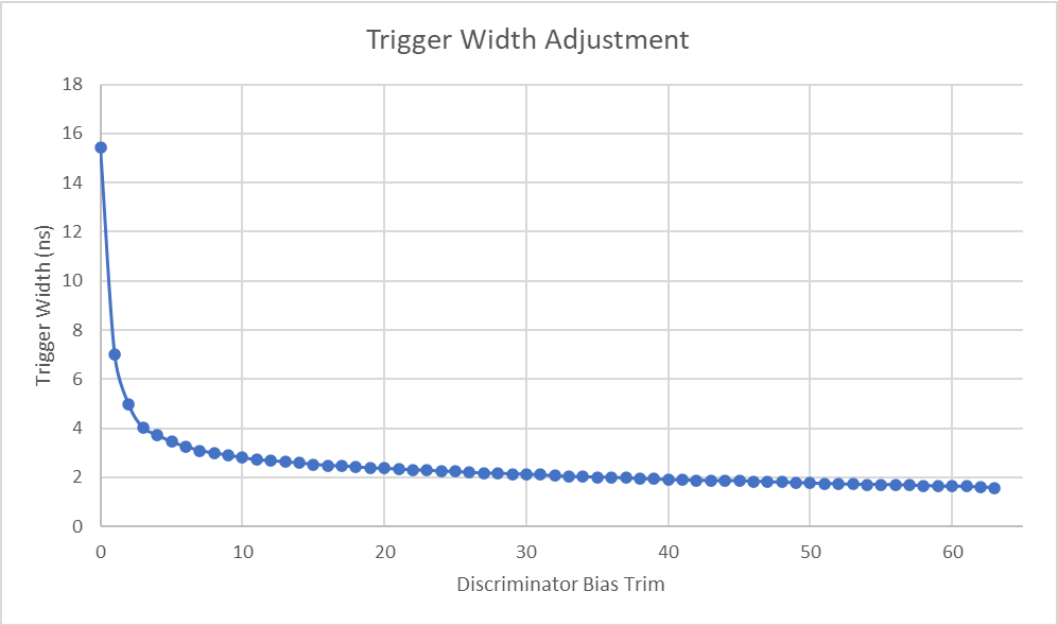

Figure 30 – Trigger width adjustment

Other feature that has been added to this ASIC, is the ability to trim its trigger output width, as shown in Figure 30. The ASIC is able to trim its trigger output width from 1.6 ns up to 15.443 ns. It should be noted that is the minimum width would be dependent on the input pulse width itself and the threshold applied to the pre-amp.

For the transient measurement, it has been done mostly on the trigger output for the jitter (Figure 31), typical response at 1/3 p.e (Figure 32) and double pulse separation (Figure 33).

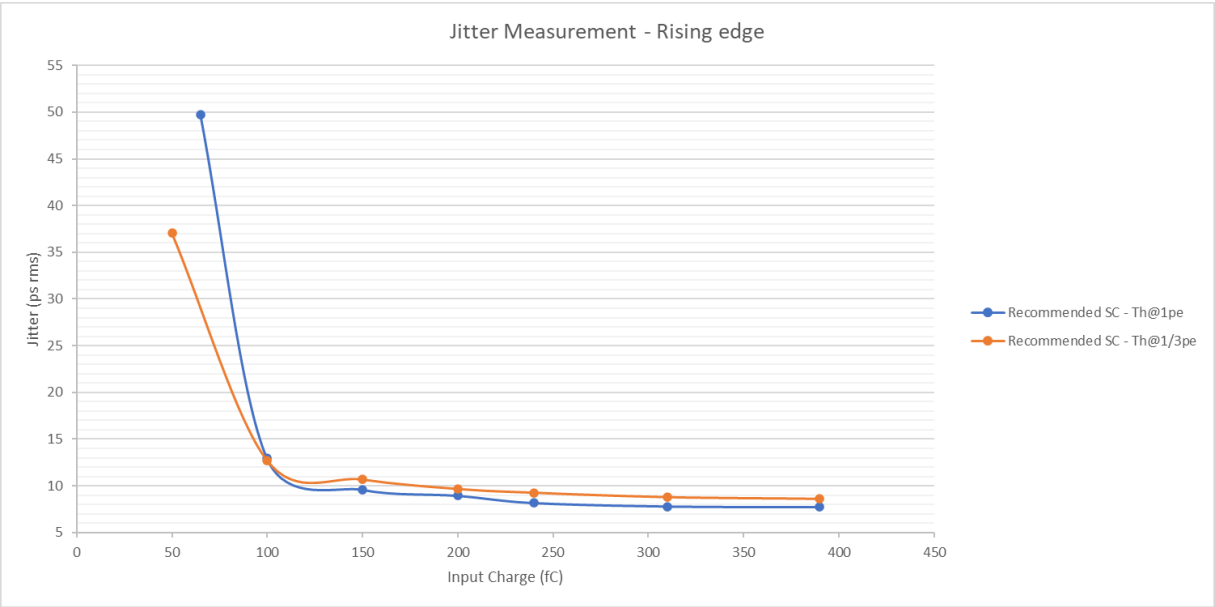

Figure 31 - Trigger output jitter

The jitter of the trigger output has been measured using charge injection with 10pF of charge injection capacitor and the result is reported in Figure 31. The threshold is set at 1 photoelectron and 1/3 photoelectron. The jitter is recorded for

various input charge. With 160fC input (about 1p.e), the jitter is about 9.57 ps RMS for threshold of 1/3p.e. In this configuration the jitter can be as low as 7.72ps for 390 fC of input signal.

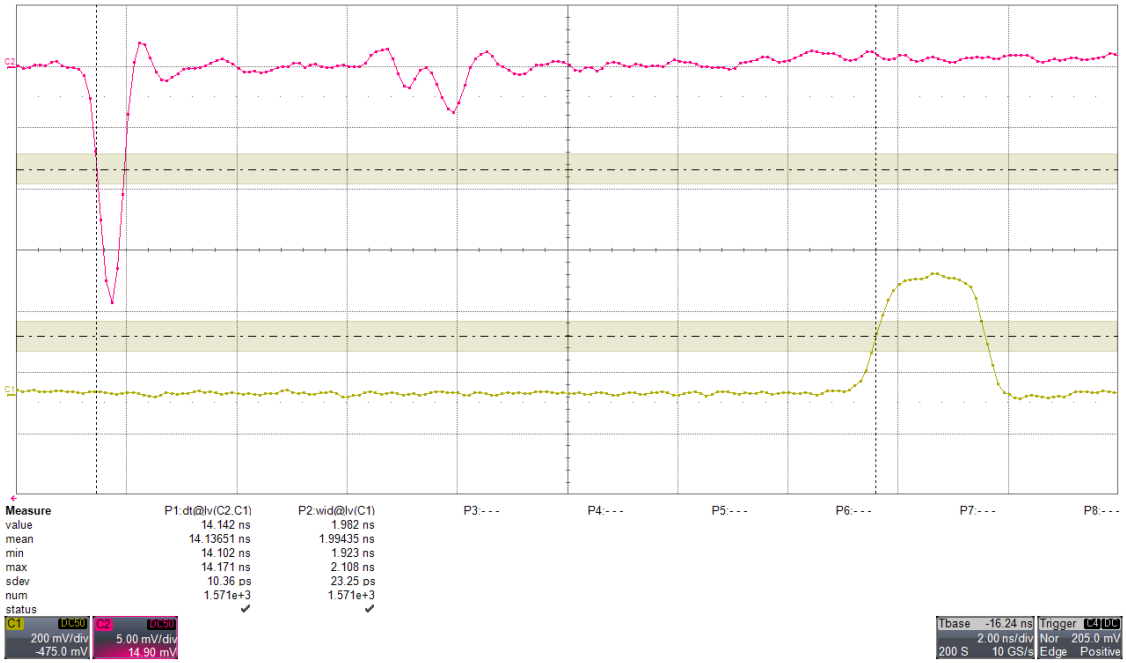

Figure 32 – Trigger output response to 20mV, 1ns of width input pulse. ASIC threshold is set slightly above the baseline (approx 1/3 p.e)

Figure 32 show the response of the ASIC trigger to a 1ns wide input pulse of 20mV amplitude. The threshold is set about 1/3 p.e. The trigger output width is about 2ns.

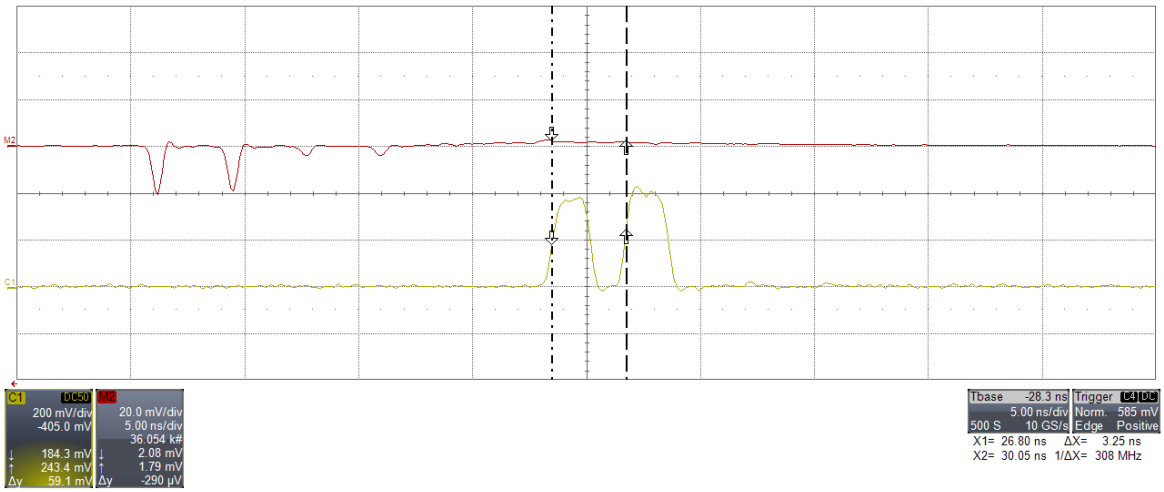

Figure 33 - Trigger output response to double input pulses of 20mV, 1ns of width separated by 3.25ns of each other.

Figure 33 shows the trigger response to double pulse input separated by 3.25ns of each other. The threshold has been set slightly above 1/3 p.e and the two trigger outputs can be clearly separated from each other.

Datasheet version history

Version	Date	Information
0.1	21/03/2024	Initial release