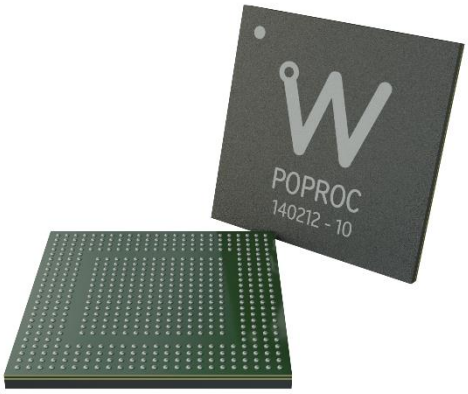
Poproc

SOFTWARE & EVALUATION BOARD USER GUIDE

Version: 27 February 2025

Abstract

POPROC is a MA-PMT readout out chip, specifically design for fast counting output. This guide explains how to install and use the evaluation board for POPROC and how to operate with the associated software. It will cover specifically the evaluation board released with Artix 7 FPGA.



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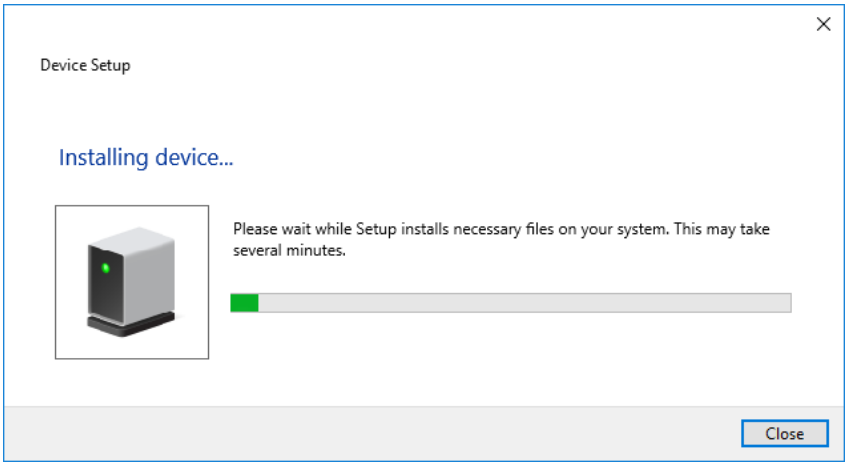
1 Installation & Test of the Test Board

1.1 Pre requisites

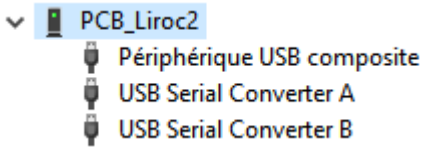
The usage of this evaluation board requires the following:

- A computer (Microsoft Windows 10 or later) with USB connection
- A USB-A to mini-USB cable
- A positive output power supply (delivering 5V and 2A)

When the first time a Weeroc evaluation board is plugged, the following message should prompt :



In order to verify that the drivers are correctly installed, go in the control panel under the "Devices and Printers" window. the PCB_POPROC device should appears as following:



1.2 Installation guide

Before running the software for the first time, please verify that the evaluation board is correctly identified in the "Devices and Printers" window under the control panel. The release of the POPROC user interface can be found in the Weeroc download center on the website http://www.weeroc.com .

2 Evaluation board description

The evaluation board has been developed to allow characterization and debug of the POPROC ASIC. Some of the features were added on the board or in the firmware/software to allow versatility and its use with detectors or within an experiment. The schematics of the evaluation board, the firmware and software sources are provided on the WEEROC website, users can use the online resources freely in order to fit into their own requirements.

- This board provides easy access to each POPROC pin, as all analog pins are connected to through-hole test points and as all digitals I/Os are connected to test points between the ASIC and the FPGA.
- Many test points are also connected to the FPGA, outputting digital internal nodes.
- 2 analogue buffers provide ASIC's analog outputs on 50-ohm load on SMA connectors. These two are analog probes (Analog_Probe1 and Analog_Probe2).
- The board needs to be externally powered by a 5V/2A supply.

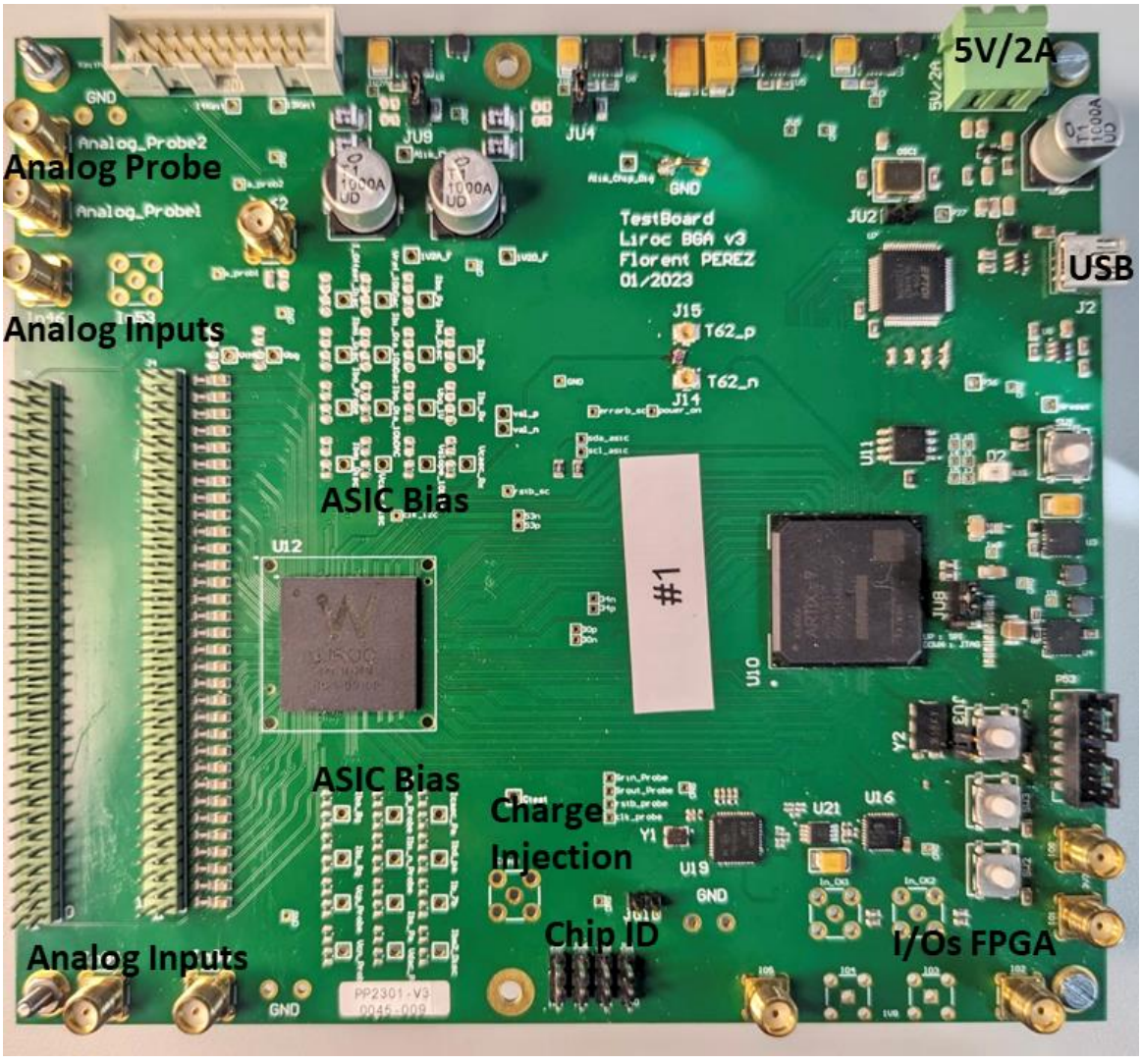


Figure 1: POPROC Evaluation Board (Artix 7)

3 Software description

The software has been written in python language. The source code is available on demand in order to help users to comprehend the functionality of the software. This is especially useful if users aim to develop their own data acquisition (DAQ) system.

To start the evaluation board, users need to:

1. Connect the USB cable from the evaluation board to your computer.
2. Provide power supply to the evaluation board using an external Power Supply (5V-2A).
3. Start the software and click on the "Connect" round button.

When connecting the evaluation board, drivers for the USB device should install automatically. If it is not the case, the drivers can be found on the FTDI website (http://www.ftdichip.com/Drivers/D2XX.htm).

When this software is launched and the "Connect" button clicked, no error should occur, meaning that the installation has been done successfully and all the drivers and dll have been found. If a crash occurs or if assistance is required for any other issue with the software, contact the Weeroc support by opening a new support ticket at the address http://www.weeroc.com/my-weeroc/support.

While this user guide will help the user to use the software and evaluation board, it should be noted that there is an embedded help in the software. By hovering controls with the mouse, the green bottom part will be filled with information on the object being hovered.

The firmware version is automatically detected by the software and is written to the interface. The expected firmware version should correspond to the last number in the software version. The firmware version is 31, while the software version is 2.0.1.31.

Screenshots can be taken thanks to the button with the # icon on the title bar.

3.1 Slow Control page

All the slow control parameters of POPROC are displayed on this tab control, allowing tuning & tests for different settings.

To program the POPROC ASIC, users must set the Slow Control parameters and press "Enter" keyboard to validate their changes. The slow control parameters are loaded in the ASIC using I2C protocol.

The settings can be saved in a text format file thanks to the "Save config" button, and reloaded from this file with the "Load SC" button.

By default, the slow control bits are accessible through various tabs in this page.

3.1.1 *Standard mode - Main*

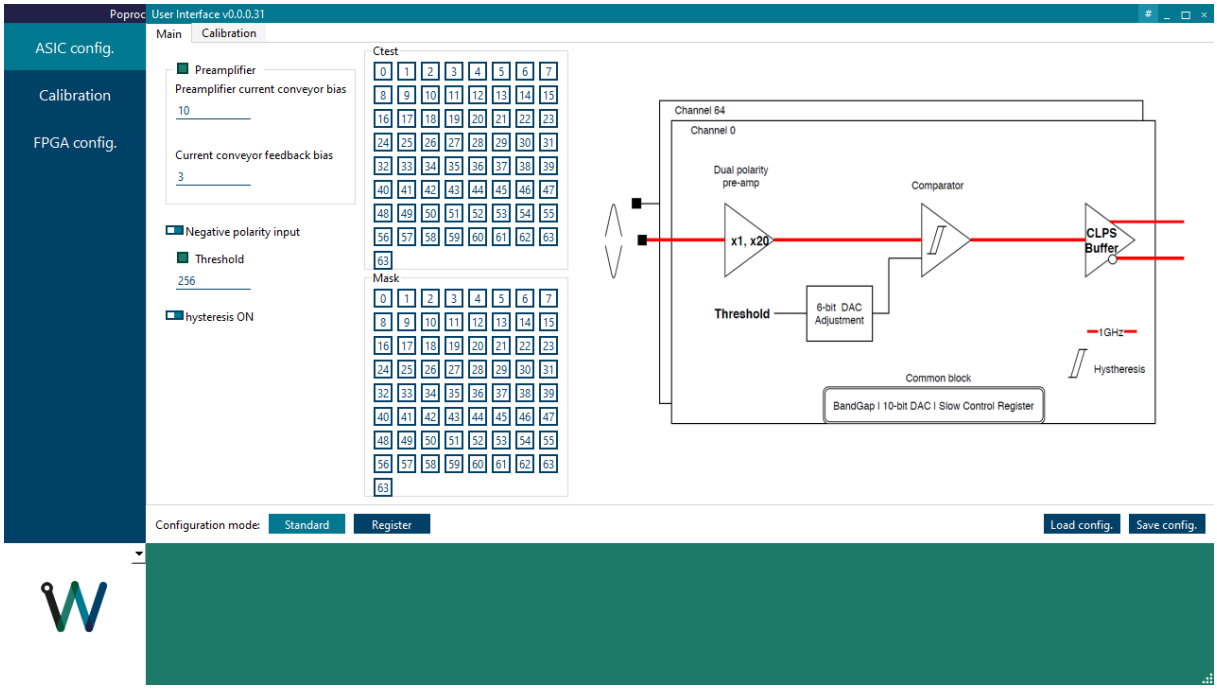


Figure 2 : ASIC configuration - Standard Mode - Main

This tab regroups several general settings of the ASIC.

The preamplifier can be adjusted by entering a new value in the textbox and pressing enter. The DC level of the pre-amplifier is about 600mV and can be adjusted by 6.5mV steps. Feedback bias can also be adjusted.

The discriminator polarity can be changed by toggling the "input polarity" checkbox. This will result in changing the Trigger Output from "low" to "high" depending on the signal type used at the input of the ASIC. Checking the checkbox allow the trigger to follow the input signal behavior (positive trigger for positive input). The behavior of trigger output is depicted in the following figure.

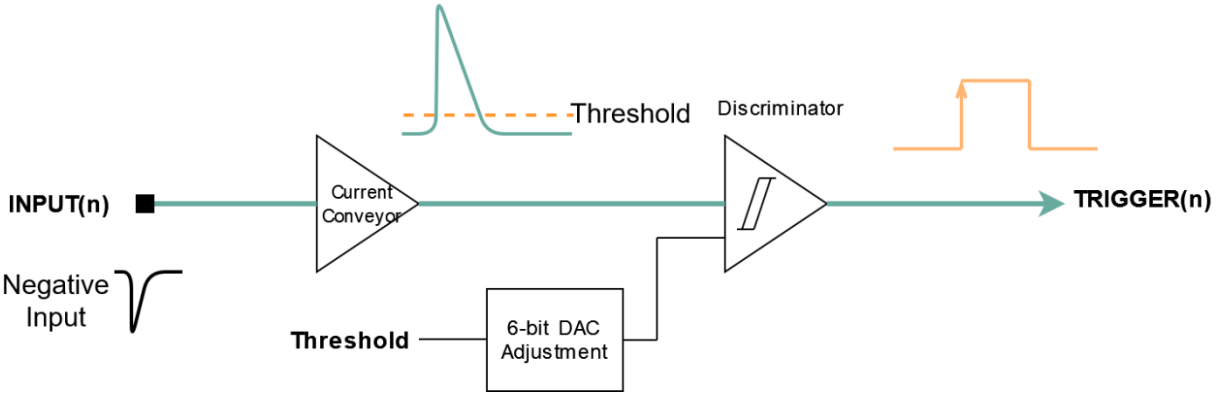


Figure 3 : Analog section polarity block diagram

The "Threshold" textbox is used to set the trigger threshold. The DC level of the pre-amplifier is about 460mV (with default setting) and this signal will be fed directly into a discriminator. In order to set the trigger threshold, a 10-bit DAC is used as a common threshold for the discriminator. Right clicking on the boxes allows to select or unselect all boxes.

- DAC <0:9> - 595mV~898mV, Step :0.3mV, Default value: 692mV (with default trim)

The "Ctest" checkboxes allow to inject signal in the checked channels via the "Ctest" SMA connector. The more channel enabled, the less charge injected in to each channel, due to the fact that input signal is shared with all enabled channels.

The "Mask" checkboxes allow to mask triggers from the discriminator. When masked, the trigger will remain low. The number in the checkbox corresponds to the channel number. The channel is masked when the checkbox is checked.

3.1.2 Standard mode - Calibration

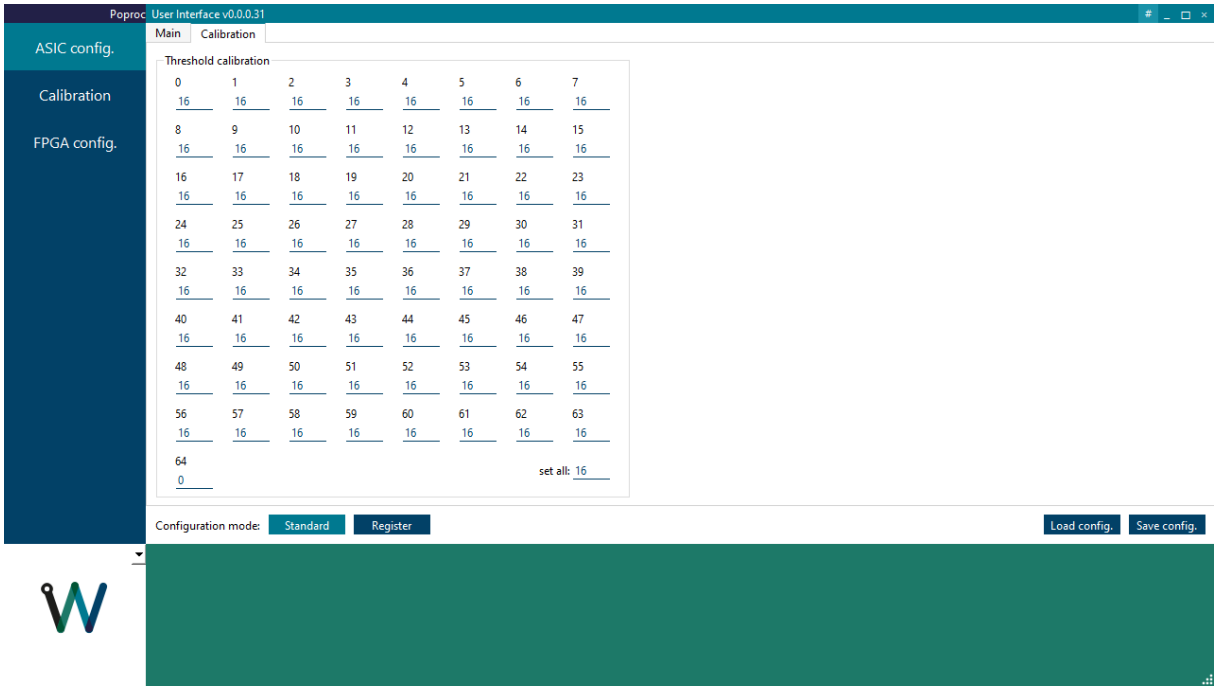


Figure 4 : ASIC configuration - Standard Mode - Calibration

This tab regroups "Threshold Calibration" settings.

The purpose of the threshold calibration (7-bit DAC) is to trim the trigger threshold. This threshold is provided by a 10-bit DAC (available in "Threshold" – Section 3.1.1) and it is common to all 64 channels. In order to correct the trigger dispersion, 7-bit DAC for trimming the threshold have been added for each channel.

- DAC local <0:6> Range : 0~216mV , Step : 3.5mV, Default value:123mV

3.1.3 Register Mode

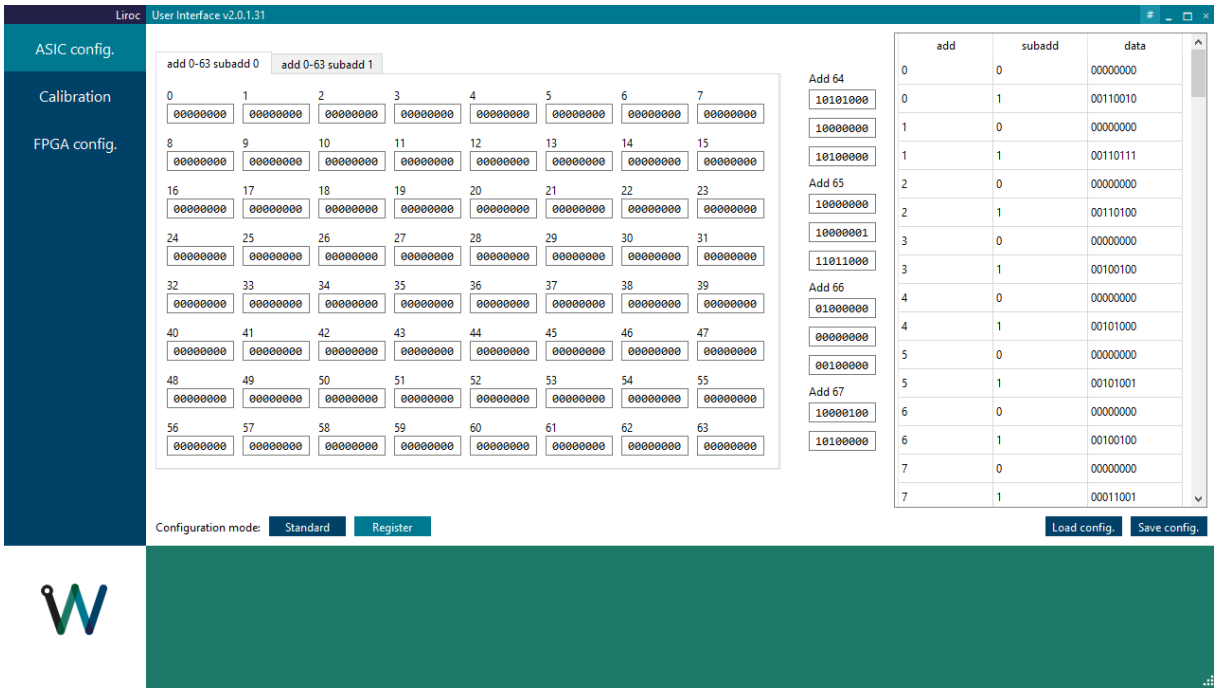


Figure 5 : ASIC configuration – Register Mode

The register mode allows to read and write directly to Poproc Slow Control registers (cf. Poproc datasheet).

3.2 The calibration pages

3.2.1 S-curves

The first tab in this page is called "S-curves" and its aim is to perform trigger efficiency test. The resulting plots is a sigmoid curve resembling the letter "S" hence the S-curve usage. It is done by scanning through several values of threshold and measuring if a trigger happens on the output signal of the pre-amplifier. The acquisitions are windowed by an internal clock (Clk - Figure 6) which toggle the Valid event signal. If a trigger happens outside the window, it will not be taken into account.

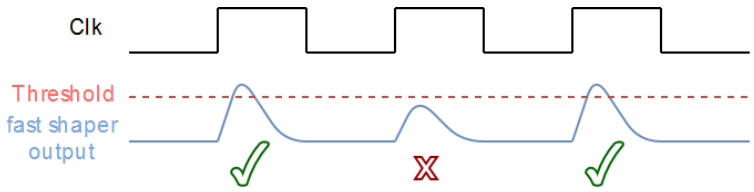


Figure 6 : S-curves data acquisition timing diagram

When the threshold is below the signal or pre-amplifier baseline, the trigger efficiency will be 100%. With a threshold over the signal/baseline, trigger efficiency drops to 0%. On **Erreur ! Source du renvoi introuvable.** the threshold is set near the tip of the noiseless signal so the ASIC will have a ~50% chance of triggering depending on the noise. Following the example in Figure 6, the ASIC would trigger 2 times in 3 acquisition windows, resulting with a 67 % trigger efficiency.

The acquisition is started by clicking on the "Start S-curves" button. The S-curves can be plotted on the baseline or on the signal thanks to a switchbox ("Use Ctest"). With "Use Ctest" switch enabled, in order to plot the S-curves user will need to inject signal through the "Ctest" connector (Figure 1). The injected signal must be synchronized with the clock signal on "IO3" connector to send the signal in each acquisition window as seen on **Erreur ! Source du renvoi introuvable.**. The clock speed can be adjusted from 1 kHz to 100 kHz. Slower clock will make the acquisition of the S-curves longer.

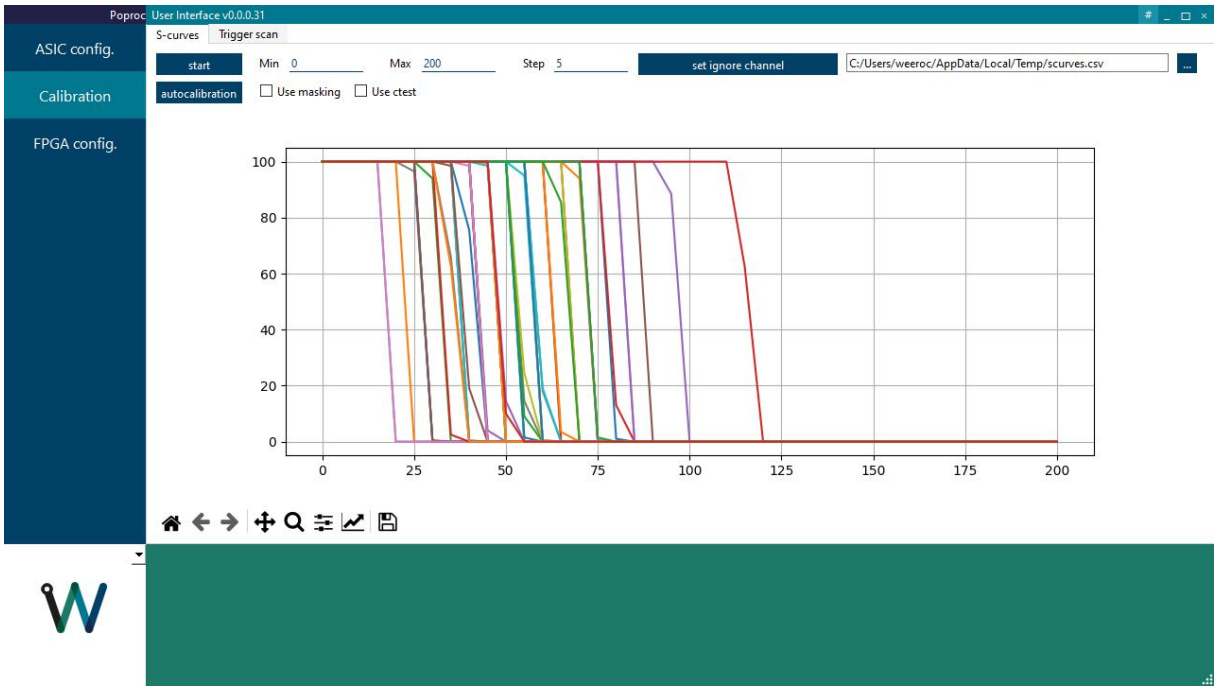


Figure 7 : S-curves tab.

It is also possible to plot only selected channels in the channel selection. Plotting the S-curve on one channel will be faster than performing it on all channels. It can be useful if would like to perform a quick assessment of the trigger response for a given channel.

3.2.2 Auto-Calibration

This feature will help users to calibrate or align the trigger threshold baseline of all channels within a few DAC steps. An example of the calibrated threshold baseline is shown in **Erreur ! Source du renvoi introuvable.**. This calibration process is done by analysing the S-curve responses of all channels. It is done automatically without any input required from users.

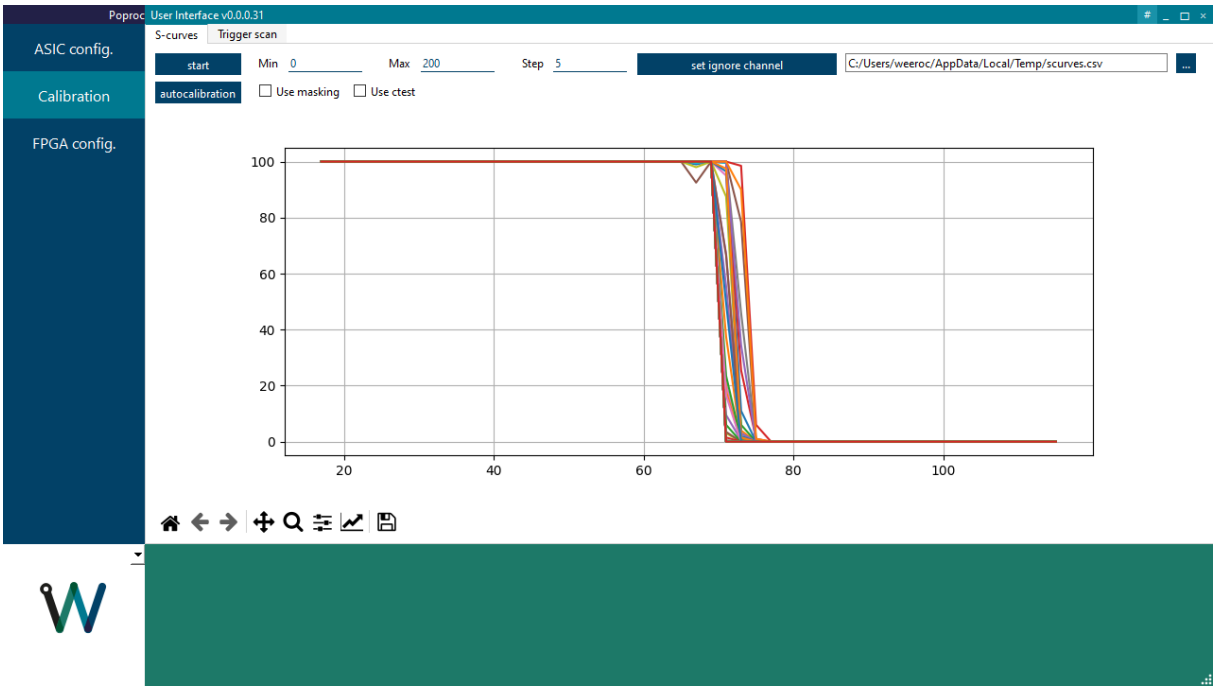


Figure 8 : Calibrated Scurve

It is advised to use the "Save SC" Button of the ASIC configuration tab, as these values can be reused every time on the same board/ASIC.

3.2.3 MA PMT staircase

The staircase measurement is used to locate the pedestal and count the trigger frequency in regarding the threshold DAC code. It will record the trigger count per second and will plot the Trigger Rate of the MA-PMT under test. The MA-PMT must be plugged on the board and set in the dark with a bit of light (with LED for example). A scan through the threshold DAC values will allow locating the baseline and the first photoelectrons values.

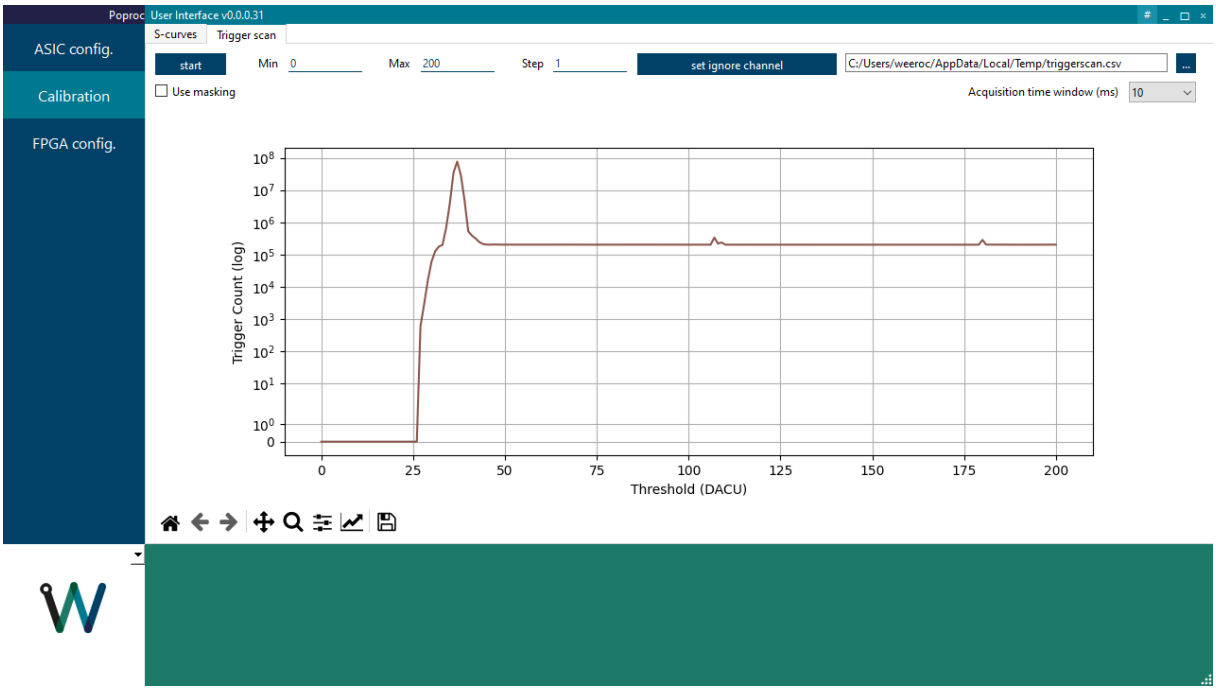


Figure 9 : Staircase plot from Poproc user interface.

Those values can be used to choose the threshold value or to calibrate the gain of the 64 MA-PMT cells.

3.3 The FPGA configuration page

Probe or signal monitoring channel selection is also available in this tab. It is divided into two sections

3.3.1 Discriminator output

Th discriminator output allows to monitor the discriminator output. 4 outputs are available for measuring purpose. Each IO FPGA can be wired to 4 different signals:

Single Trigger Channel. The selected channel number must be written to the corresponding IO textbox and enter must be pressed to send the command.

ORT. FPGA logical OR for the 64 channels

Scurve Clock. Can be used to calibrate the DAC Calib for different signal amplitude.

Val event window. Can be monitored to understand the behaviour of the val event window (not used for the moment)

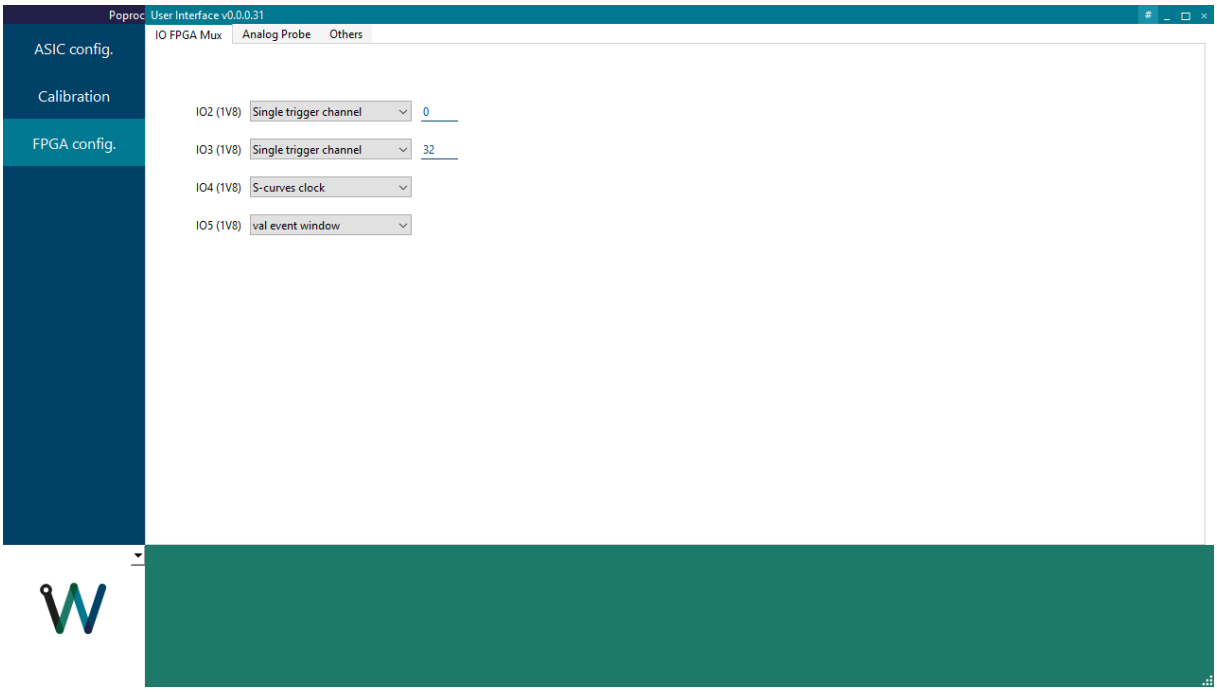


Figure 10 : FPGA configuration – Discriminator output

3.3.2 Analog Probe

The analog probe allows to monitor the pre-amplifier output or threshold DC level. The analog probe can also be used as 2 different probes, the top field is used for channel 0 to 31 and the bottom field is used for channel 32 to 63. The required channel must be written to the textbox and enter must be pressed. Additionally, a menu allows to select which of the preamplifier output and the threshold DC level must be outputted.

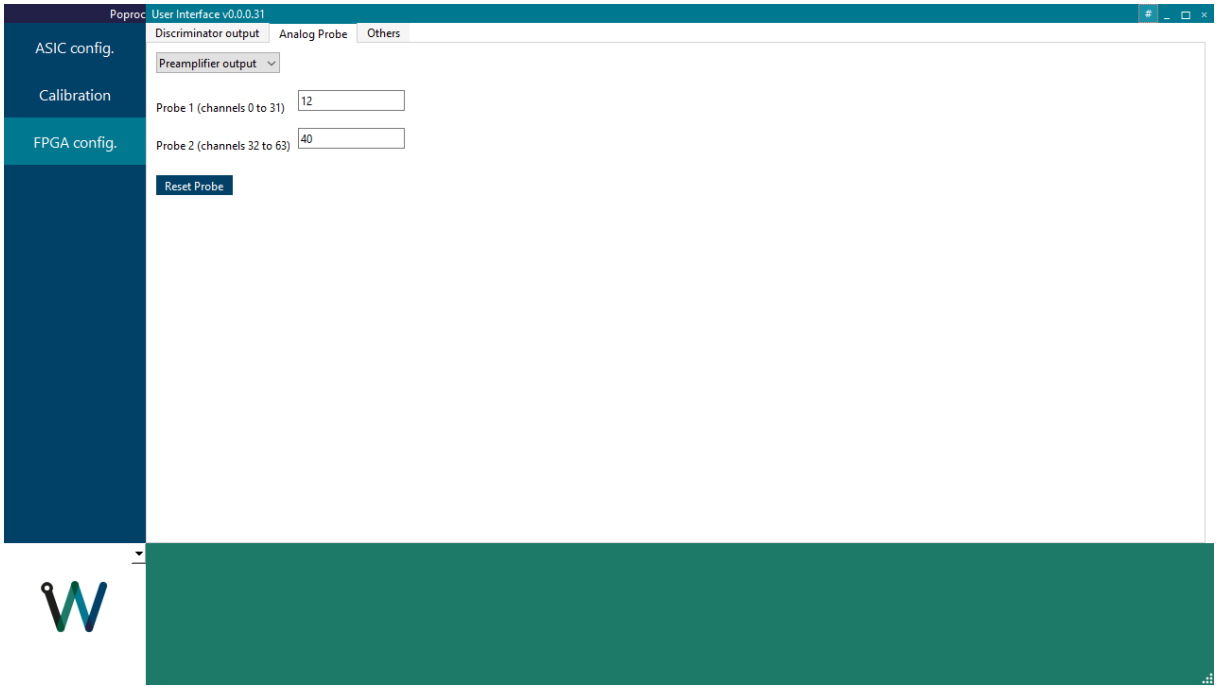


Figure 11 : FPGA configuration – Analog Probe

3.3.3 Other settings

In this tab, FPGA words can be read for debug purposes. Also, "Val event" (Validation Event) value can be changed using the switch (Low Level for mask, High Level for no mask). Then, chipID can be changed on the board by putting jumpers on ID0 to ID3 connectors. Then, it must be set accordingly on the textbox in the software. Default value (without jumpers) is 5. Finally, the component Si5344 present on the board can be programmed with a register file generated from the Clock Builder Pro software. It allows to have a clock with a custom frequency outputted on "IO1".

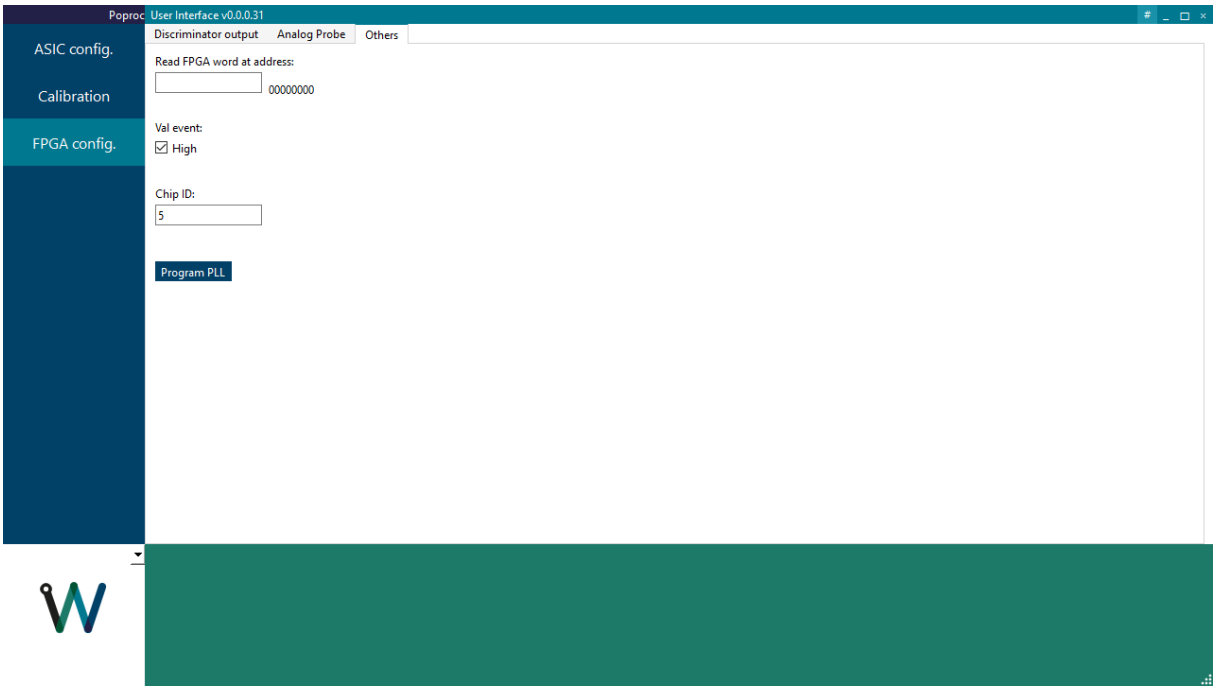


Figure 12 : FPGA configuration – Others

3.4 Trigger 62 board options

Trigger 62 is available on UMCC connector:

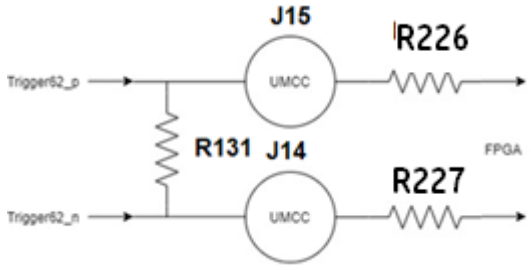


Figure 13 : Trigger 62 options

By adding 0 Ohm Resistor on R226 and R227 (Bottom of the board) will connect the Trigger to the FPGA. Be sure to remove R131 (TOP between the 2 UMCC) as there is already a 100 Ohm resistor close to the FPGA receiver.

On the other side wiring a 100 Ohm resistor (R131) between the 2 UMCC connector and removing R110 and R45 will allow the user to have both line (p and n) available on UMCC with a 100Ohm termination.

3.5 Setup to inject signals

3.5.1 Injection of a voltage step

Charge injection emulating the detector signal can be done by sending a voltage step into in series capacitor. The resulting equivalent charge injected will be the voltage amplitude multiplied by the capacitor value. Onboard, there are several ways to inject the signal:

- Dedicated SMA connectors with 10 pF capacitors. These inputs are available for channel 30, 34 ,46, 53, 62
- "Ctest" SMA connector input. This input will provide internal charge injection inside the ASIC through 100 fF capacitors. All 64 channels are accessible and need to be selected through the GUI (Figure 2)
- Onboard 2x32 pins 2.5mm pitch male break away pin strip header. These male pin headers are directly connected to the 64 channels of ASIC input. It can be used with sensor adaptation boards or external capacitors for charge injection

The waveform of the injected signal is displayed Figure 14. A slow negative ramp allows to inject no significant signal in the ASIC before the next step. A voltage attenuator is needed to diminish the noise from the waveform generator.

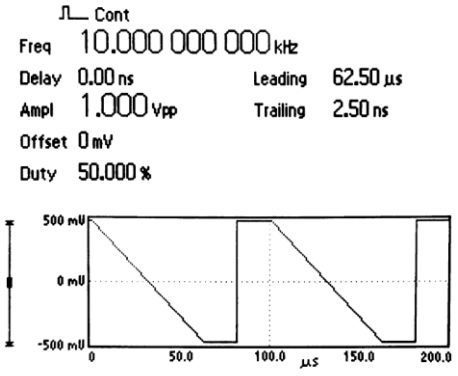


Figure 14 : Injection in each channel