Clocking and I/O Architecture

Artix FPGA Clock/Data Management: Whenever possible, utilize MRCC (Multi-Region Clock Capability) or SRCC (Single-Region Clock Capability) inputs/outputs on the Artix FPGA to manage the Temporoc clk_data signals. Additionally, ensure that all corresponding data lines are allocated to the same I/O bank.

Clock Tree Circuitry: The clock tree section is strictly dedicated to TDC (Time-to-Digital Converter) testing and characterization. It is obsolete and should be omitted on a final system-level board.

Temporoc Dedicated Test I/Os: A significant number of the I/Os present on the Temporoc ASIC are exclusively intended for chip testing and characterization; therefore, they are not required on a system development board.

PCB Layout and Routing Constraints

Timing-Coherent Routing: Special care must be taken to ensure length-matching and timing-coherent routing for dependent signal groups, specifically between clk_data(clusters) and data(clusters).

Power Supply and Voltage Adjustments

1V2D Rail Optimization: Increase the 1V2D supply voltage to 1.25V when operating at a clock frequency of 320 MHz.

val_evt_n Signal Level: Configure the val_evt_n signal to 0.6V by implementing a resistor voltage divider between the 1V2 rail and GND.

Power Supply and Thermal Issues: The current power supply circuit is undersized relative to the board's actual current consumption. The main LDO struggles to sustain the thermal load, leading to critical junction temperatures. This power stage must be thoroughly redesigned in the next board revision.

R50: Change to 0 Ohm.

R55, R60, R66: Replace with 4.7 kOhm resistors (0805 package, 5% tolerance).

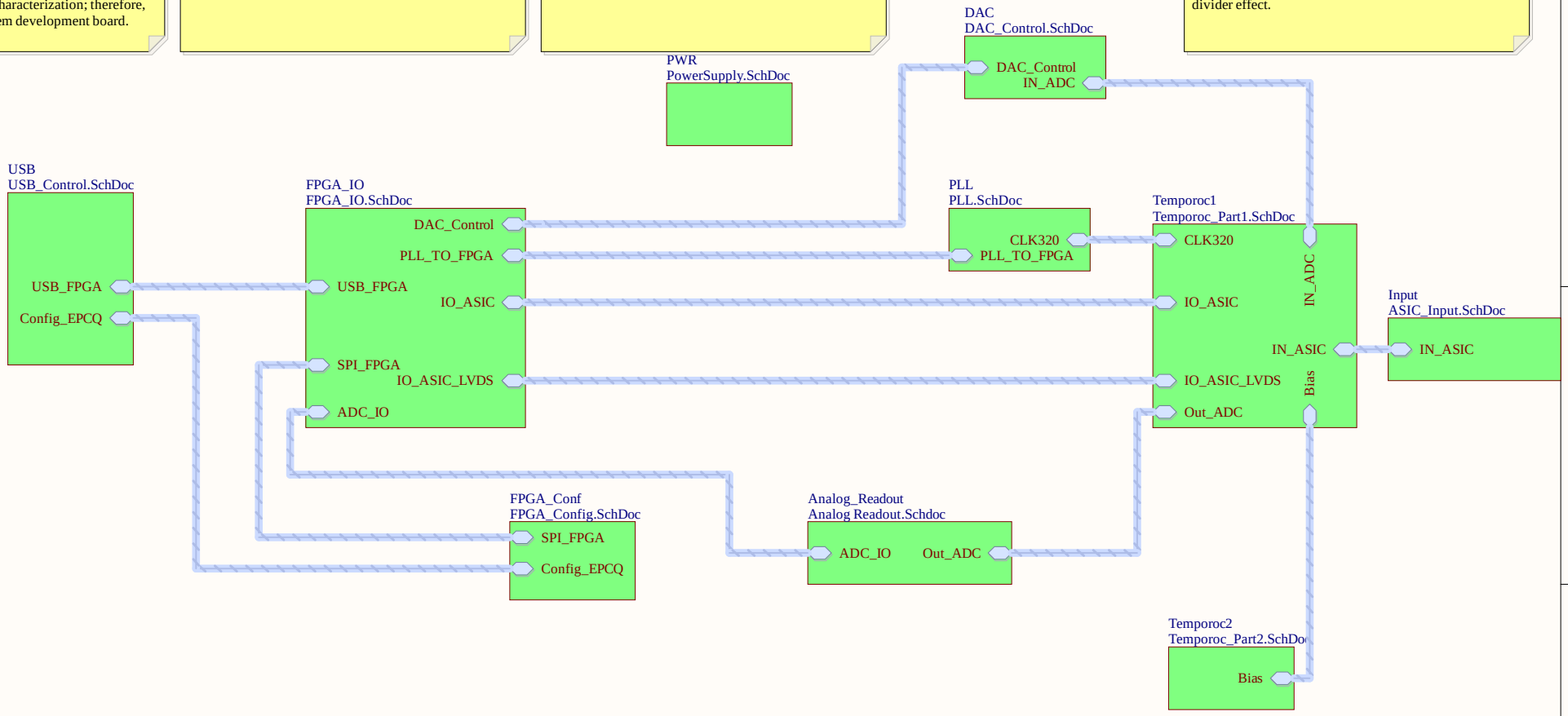
R252: Replace with a 3.3 kOhm resistor (0805 package, 1% tolerance).

R320: Replace with a 10 kOhm resistor (0805 package, 5% tolerance).

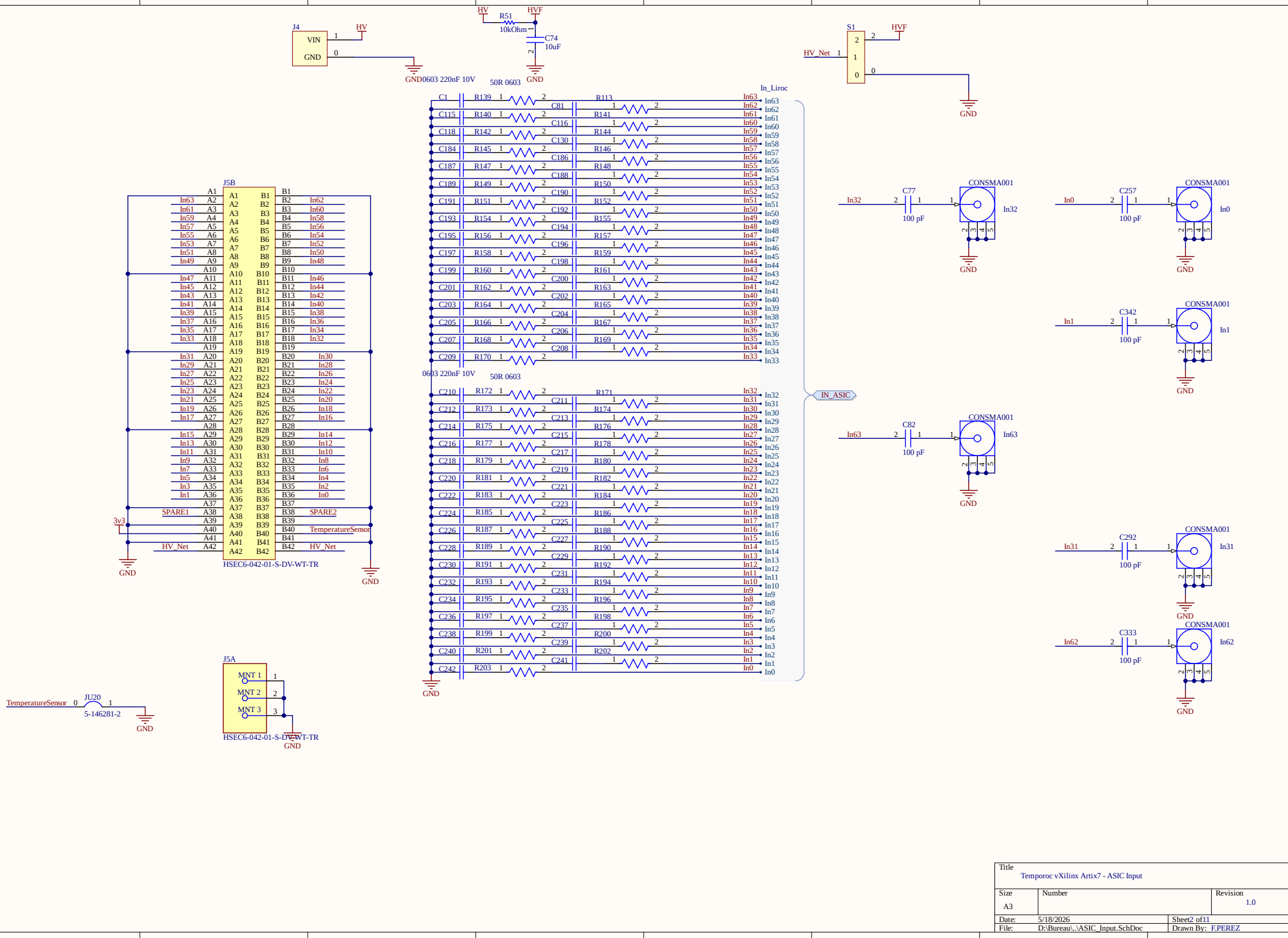
Y3: Rotate the component footprint by 90 degrees.

R286: Change to 10k

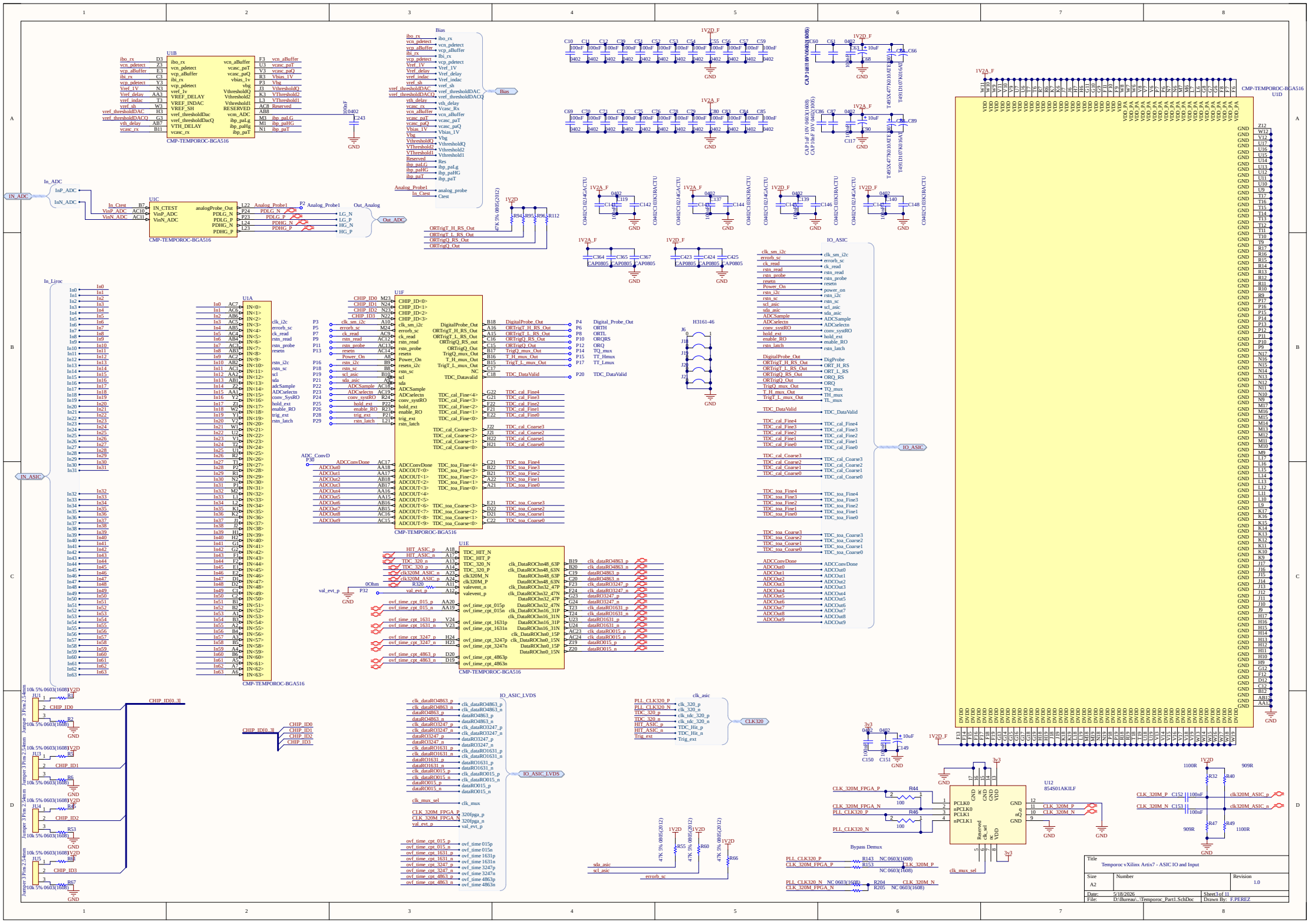
PROGRAM_B Pin: Remove the 10 kOhm resistor on program_b to avoid creating an unintended voltage divider effect.

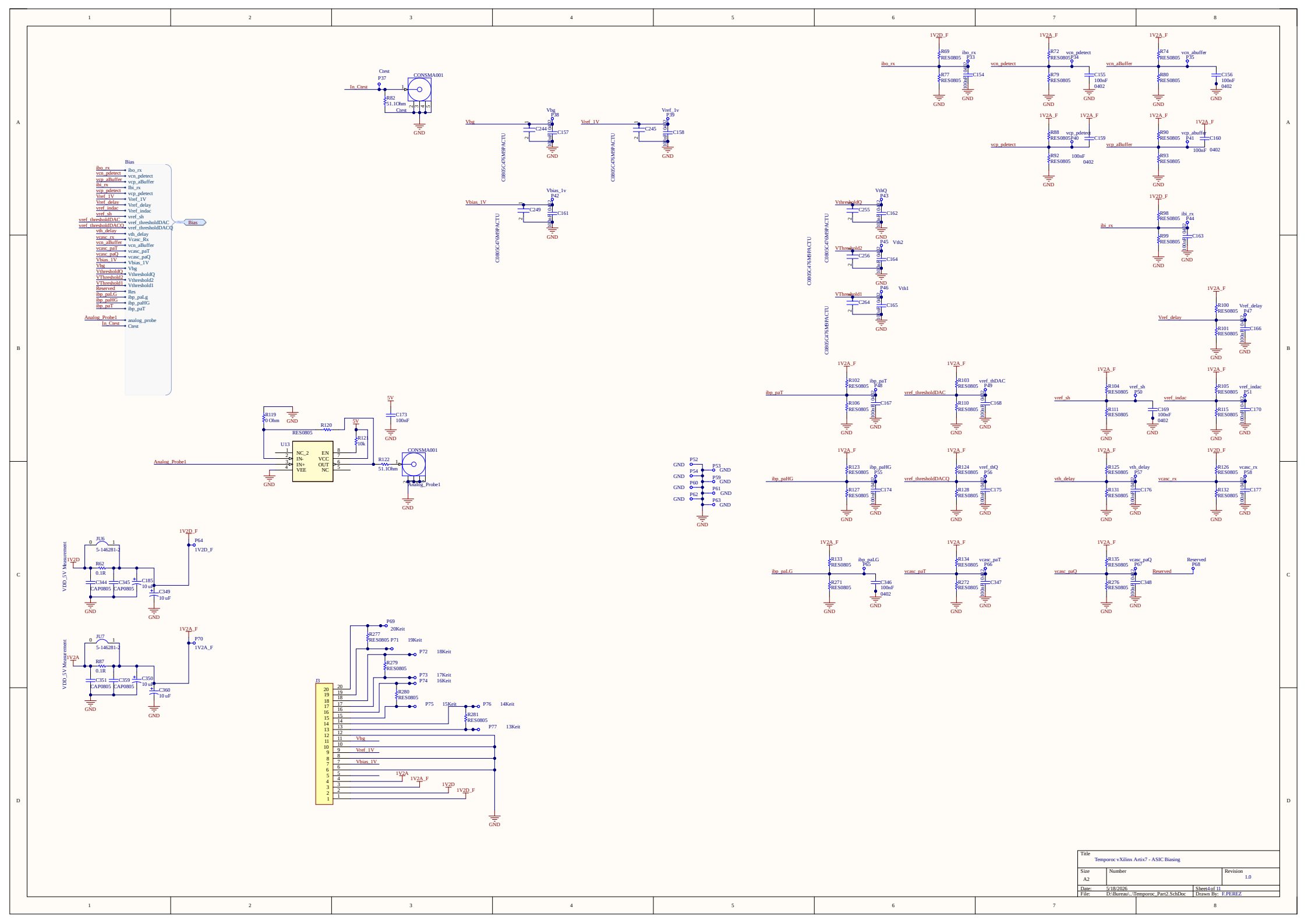


Title	Temporoc vXilinx Artix7 - Top	
Size: A4	Number:	Revision: 1.0
Date: 5/18/2026		Sheet1 of 11
File: D:\Bureau\..\Top Level.SchDoc		Drawn By: F.PEREZ

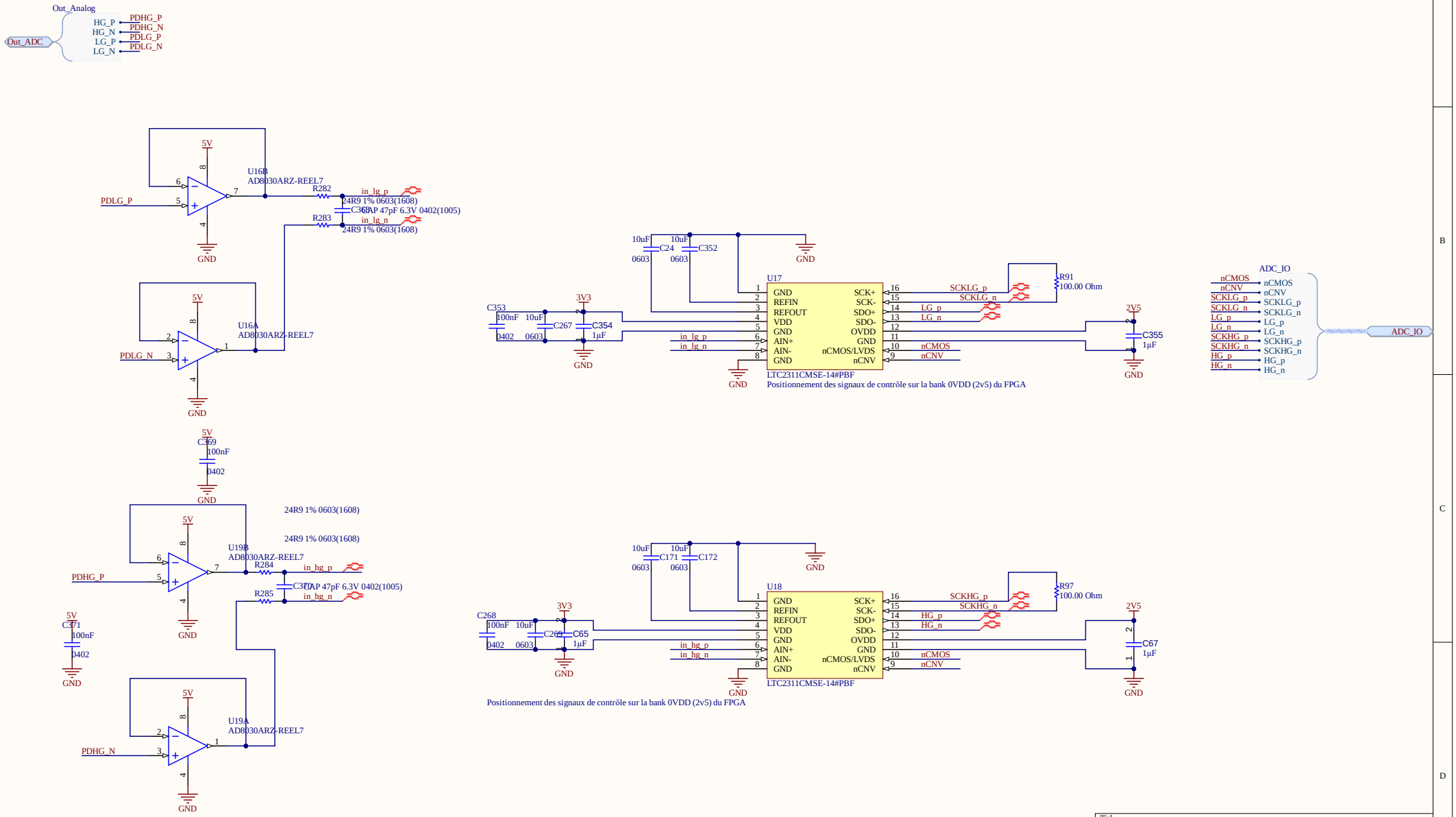


Title	Temporoc vXilinx Artix7 - ASIC Input
Size	A3
Number	
Revision	1.0
Date:	5/18/2026
Sheet	2 of 11
File:	D:\Bureau\..\ASIC_Input.SchDoc
Drawn By:	F.PEREZ

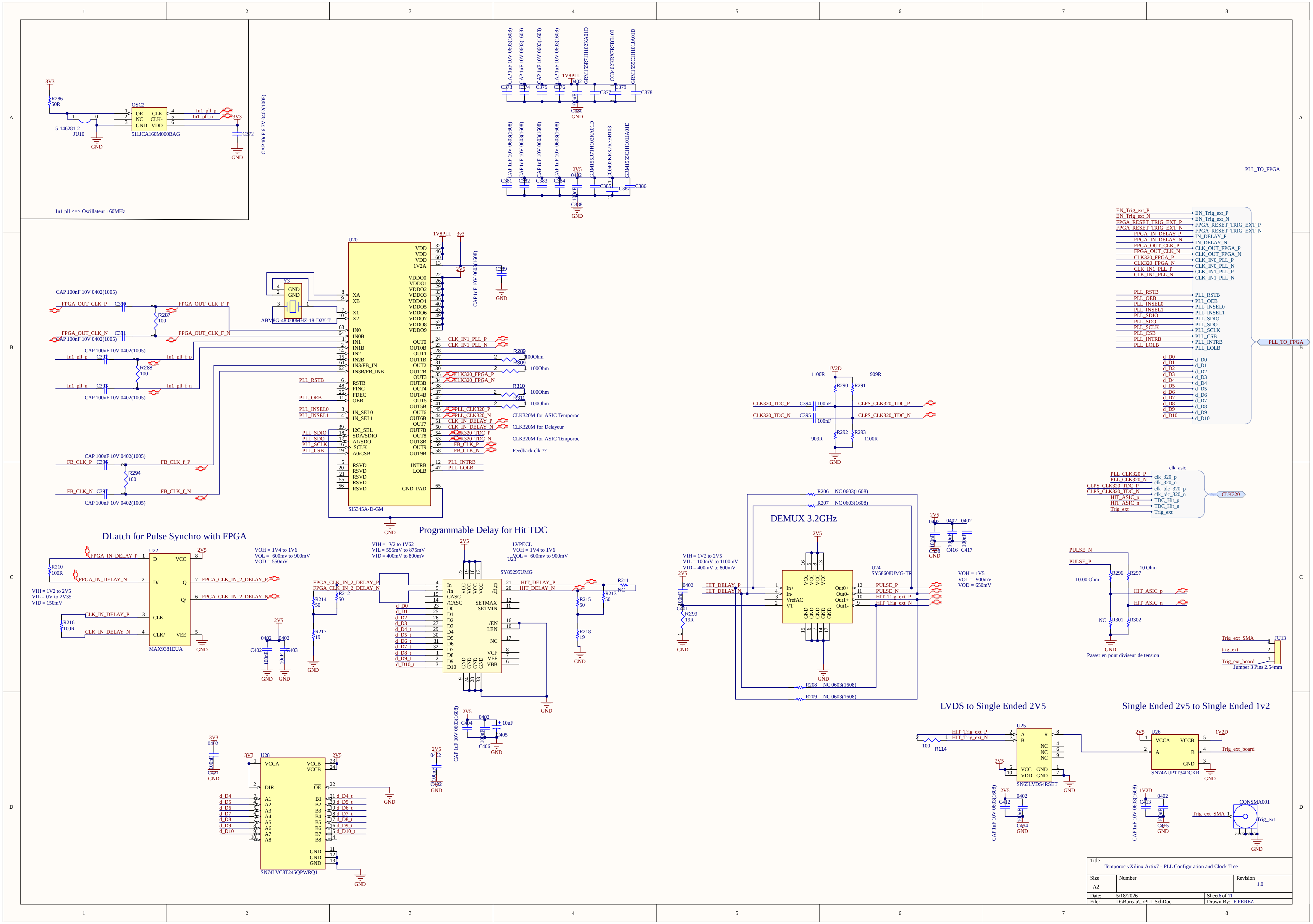

U1B
CMP-TEMPOROC-BGA516
U1C
CMP-TEMPOROC-BGA516
Bias
U1A
CMP-TEMPOROC-BGA516
U1F
CMP-TEMPOROC-BGA516
U1E
CMP-TEMPOROC-BGA516
IO_ASIC
IO_ASIC_LVDS
clk_asic
CLK320
U1D
CMP-TEMPOROC-BGA516
U12
854S01AKILF
H3161-46
Bypass Demux
Title
Temporoc vXilinx Artix7 - ASIC IO and Input
Size
A2
Number
Revision
1.0
Date:
5/18/2026
Sheet3of 11
File:
D:\Bureau\..\Temporoc_Part1.SchDoc
Drawn By:
F.PEREZ



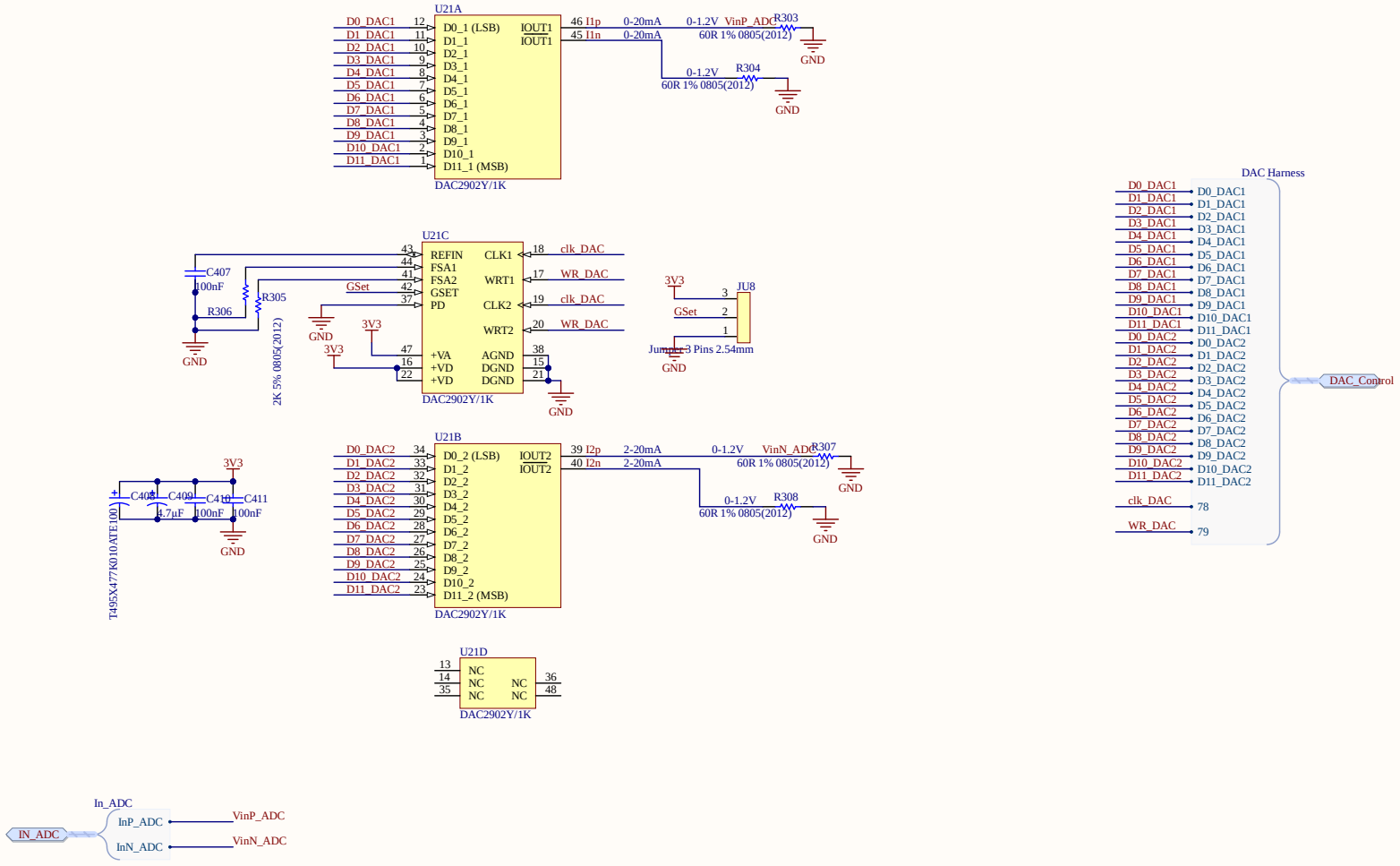
Title	Temporoc vXilinx Artix7 - ASIC Biasing		
Size	Number		Revision
A2			1.0
Date:	5/18/2026	Sheet4of 11	
File:	D:\Bureau\..\Temporoc_Part2.SchDoc	Drawn By:	F.PEREZ



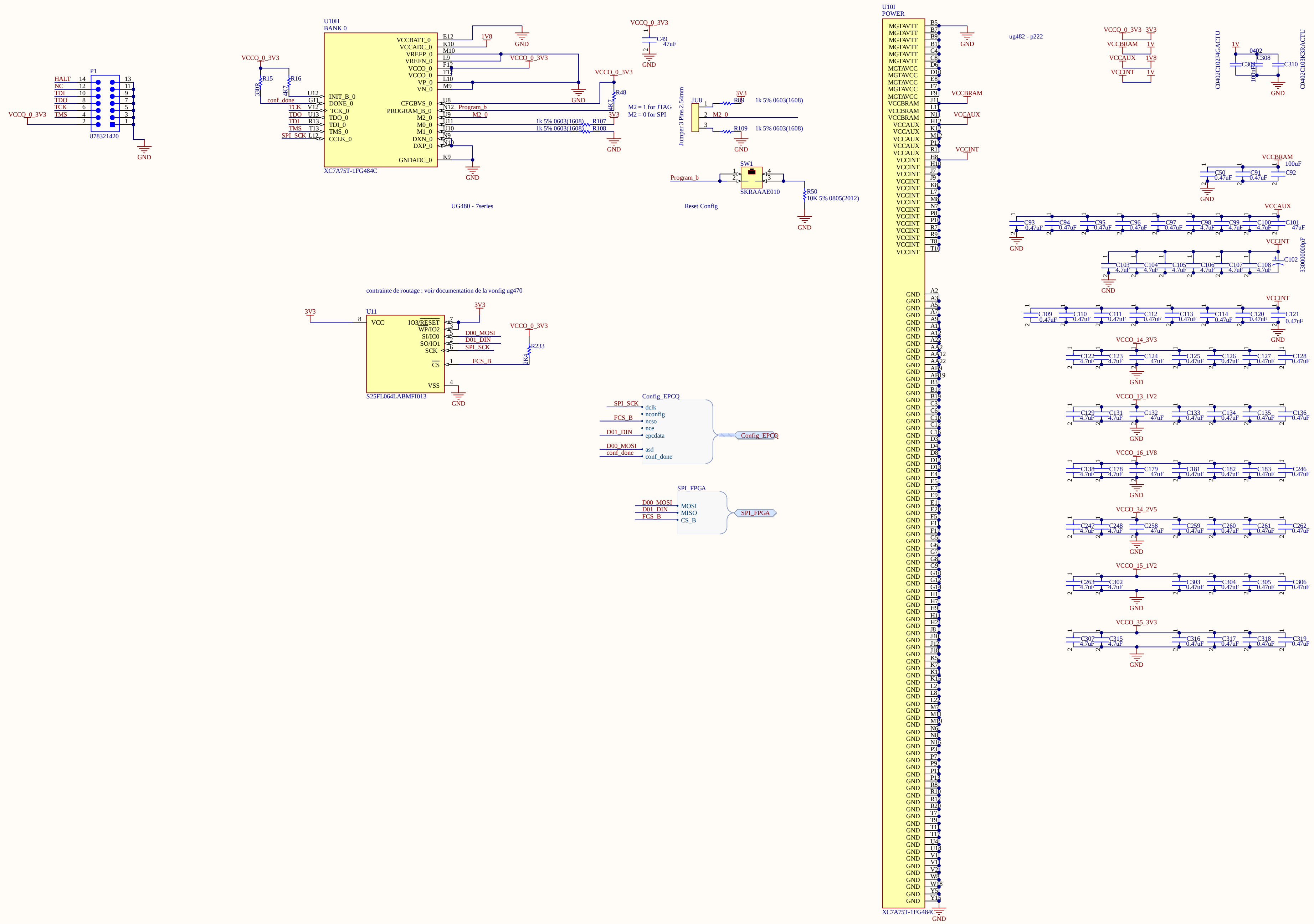
Title	Temporoc vXilinx Artix7 - ASIC External ADC Readout	
Size: A3	Number	Revision: 1.0
Date: 5/18/2026		Sheet5 of11
File: D:\Bureau\..\Analog readout.SchDoc		Drawn By: F.PEREZ



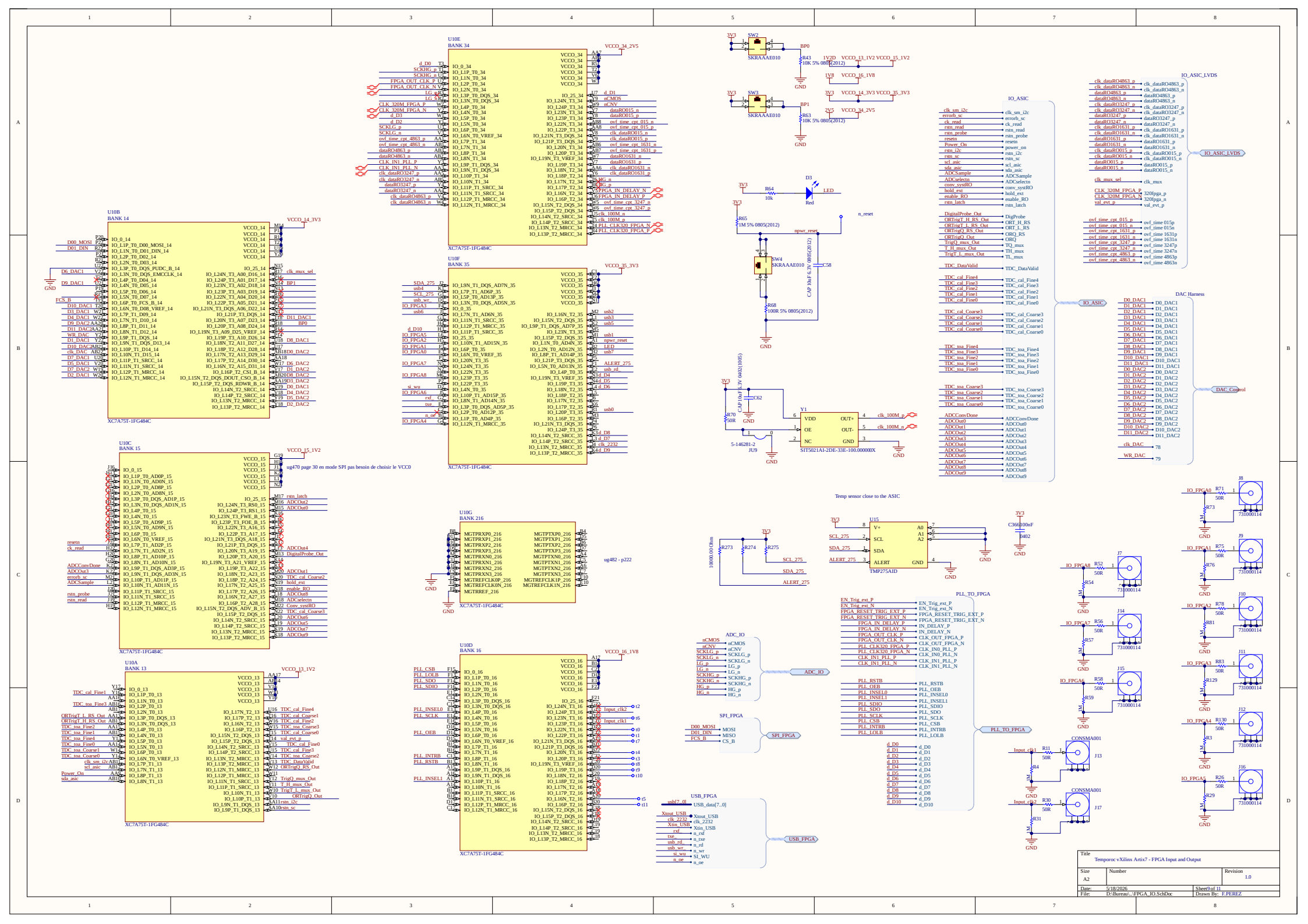
PLL_TO_FPGA
In1 pll <=> Oscillateur 160MHz
CLK320M for ASIC Temporoc
CLK320M for Delayeur
CLK320M for ASIC Temporoc
Feedback clk ??
DLatch for Pulse Synchro with FPGA
Programmable Delay for Hit TDC
DEMUX 3.2GHz
VIH = 1V2 to 2V5
VIL = 0V to 2V35
VID = 150mV
VOH = 1V4 to 1V6
VOL = 600mv to 900mV
VOD = 550mV
VIH = 1V2 to 1V62
VIL = 555mV to 875mV
VID = 400mV to 800mV
LVPECL
VOH = 1V4 to 1V6
VOL = 600mv to 900mV
VIH = 1V2 to 2V5
VIL = 100mV to 1100mV
VID = 400mV to 800mV
VOH = 1V5
VOL = 900mV
VOD = 650mV
Passer en pont diviseur de tension
Jumper 3 Pins 2.54mm
LVDS to Single Ended 2V5
Single Ended 2v5 to Single Ended 1v2
Title
Temporoc vXilinx Artix7 - PLL Configuration and Clock Tree
Size A2
Number
Revision 1.0
Date: 5/18/2026
Sheet 6 of 11
File: D:\Bureau\..\PLL.SchDoc
Drawn By: F.PEREZ

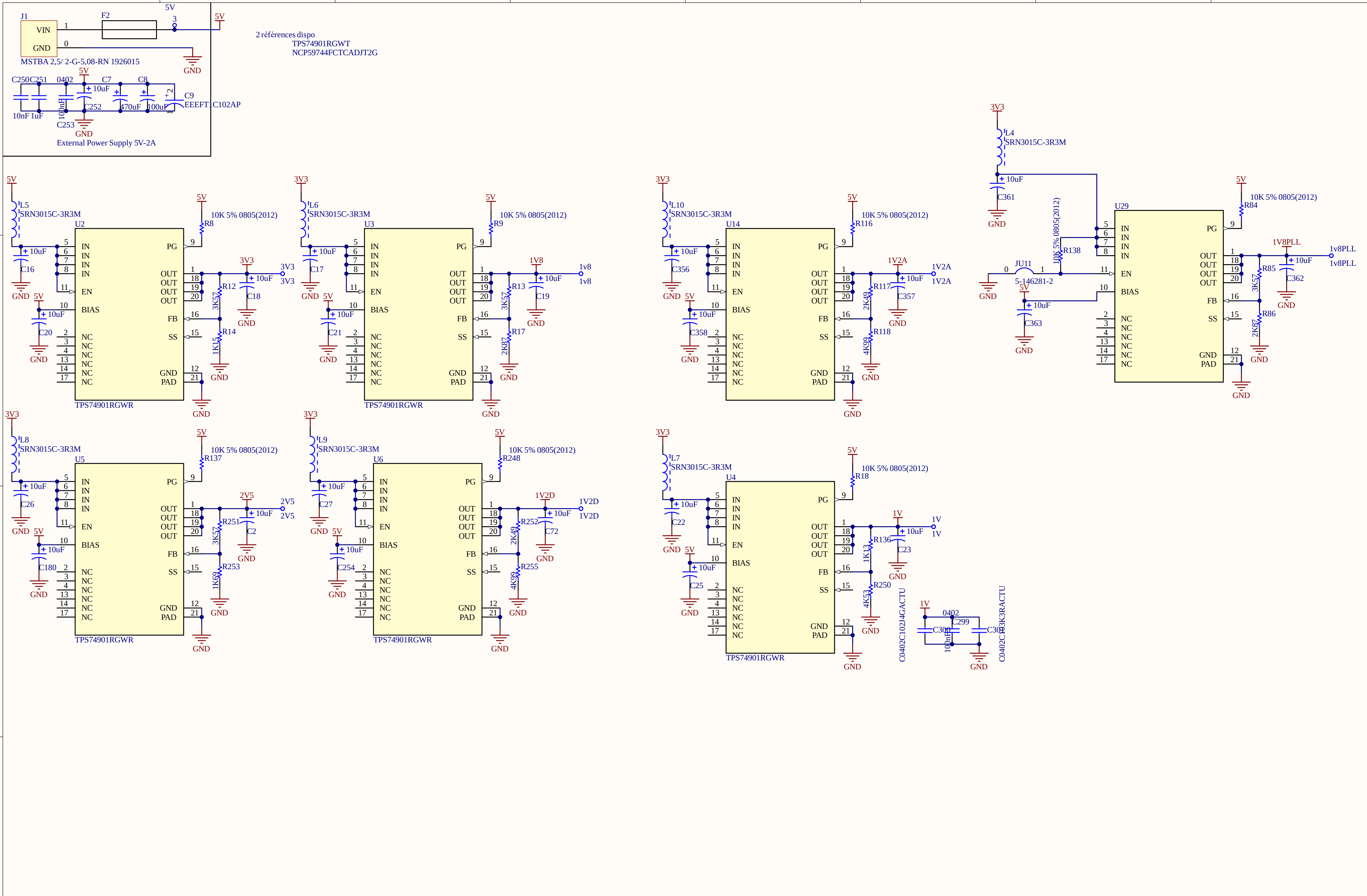


Title	Temporoc vXilinx Artix7 - DAC Control	
Size: A3	Number	Revision: 1.0
Date: 5/18/2026		Sheet7 of11
File: D:\Bureau\..\DAC_Control.SchDoc		Drawn By: F.PEREZ

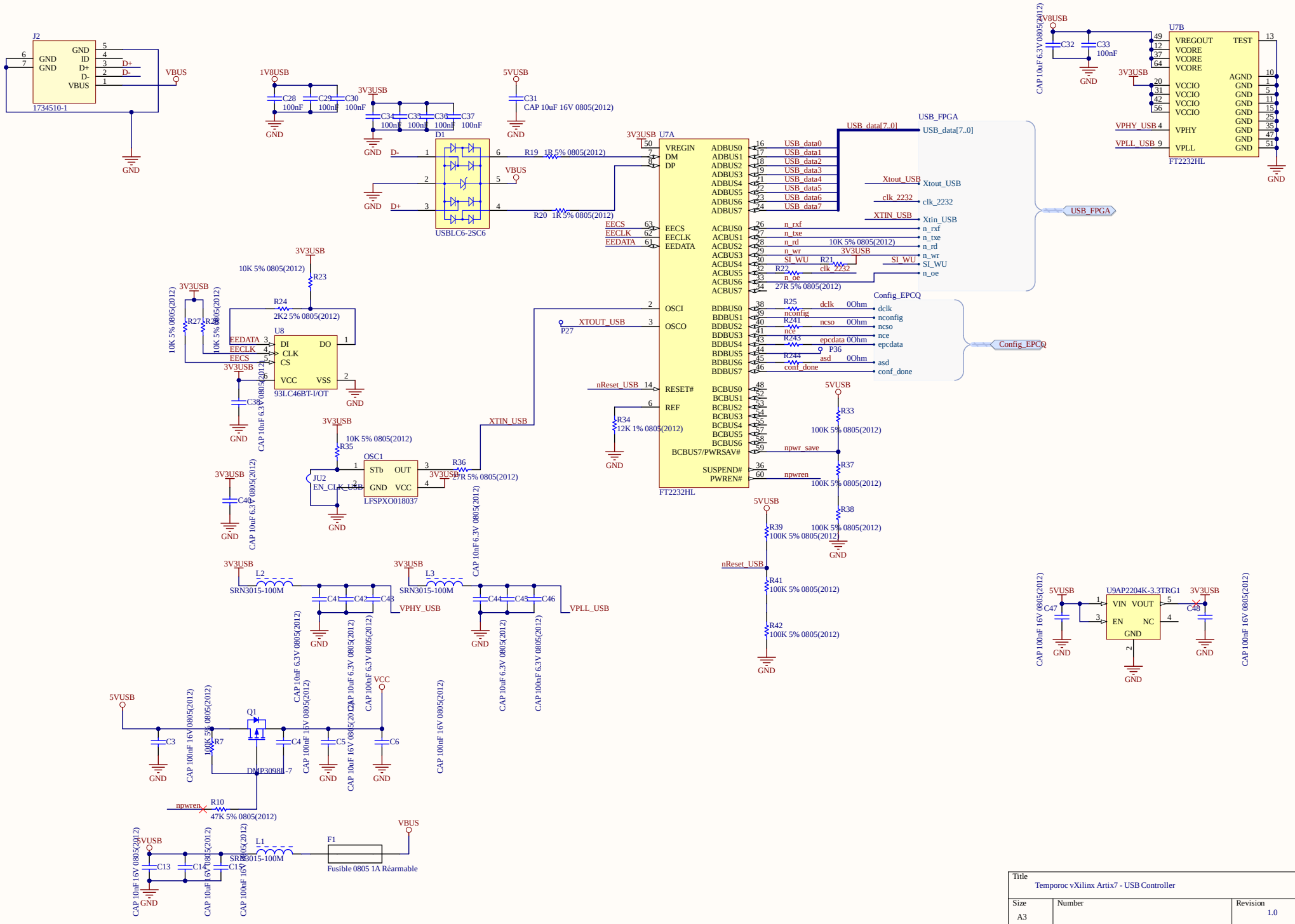


Title		
Temporoc vXilinx Artix7 - FPGA Config		
Size: A2	Number	Revision: 1.0
Date: 5/18/2026		Sheet 8 of 11
File: D:\Bureau\...\FPGA_Config.SchDoc		Drawn By: F.PEREZ

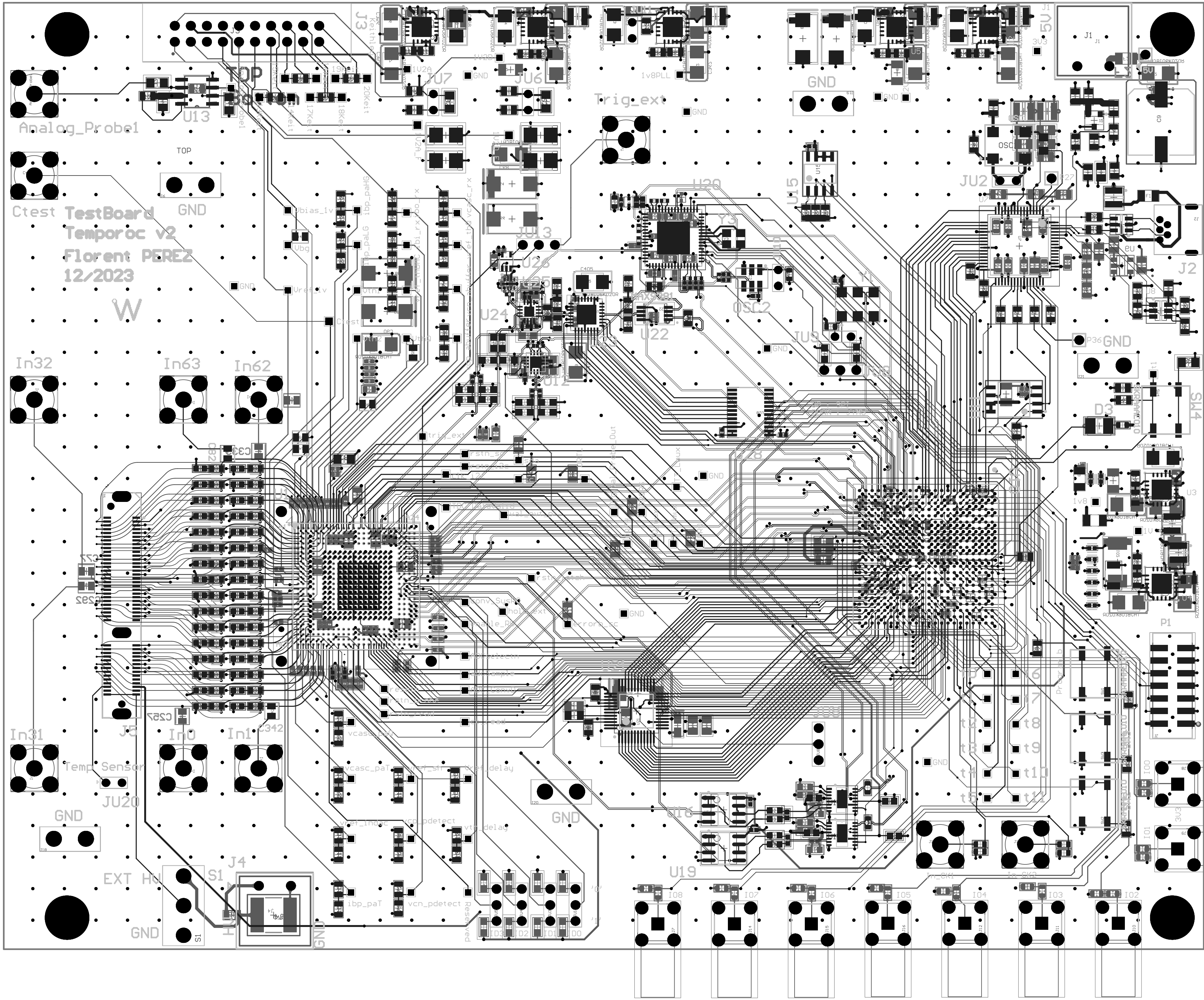

U10E
BANK 34
XC7A75T-1FG484C
VCCO_34_2V5
U10F
BANK 35
VCCO_35_3V3
U10B
BANK 14
VCCO_14_3V3
U10C
BANK 15
VCCO_15_1V2
ug470 page 30 en mode SPI pas besoin de choisir le VCC0
U10A
BANK 13
VCCO_13_1V2
U10G
BANK 216
ug482 - p222
U10D
BANK 16
VCCO_16_1V8
IO_ASIC
IO_ASIC_LVDS
DAC Harness
DAC_Control
PLL_TO_FPGA
ADC_IO
SPI_FPGA
USB_FPGA
Temp sensor close to the ASIC
SKRAAAE010
LED
Red
SIT5021AI-2DE-33E-100.000000X
TMP275AID
5-146281-2
JU9
CONSMA001
Title
Temporoc vXilinx Artix7 - FPGA Input and Output
Size
A2
Number
Revision
1.0
Date:
5/18/2026
Sheet9of 11
File:
D:\Bureau\...\FPGA_IO.SchDoc
Drawn By:
F.PEREZ


J1
VIN
GND
F2
5V
MSTBA 2,5/ 2-G-5,08-RN 1926015
GND
2 références dispo
TPS74901RGWT
NCP59744FCTCADJT2G
C250 C251
0402
C7
C8
C9
10uF
C252
470uF
100uF
EEEFT1C102AP
10nF 1uF
100nF
C253
External Power Supply 5V-2A
L5
SRN3015C-3R3M
U2
10K 5% 0805(2012)
R8
IN
PG
OUT
EN
BIAS
FB
SS
NC
GND
PAD
C16
C20
R12
3K57
C18
R14
1K15
3V3
TPS74901RGWR
L6
U3
R9
C17
C21
R13
C19
R17
2K87
1V8
1v8
L10
U14
R116
C356
C358
R117
2K49
C357
R118
4K99
1V2A
L4
C361
R138
U29
R84
JU11
5-146281-2
C363
R85
C362
R86
1V8PLL
1v8PLL
L8
U5
R137
C26
C180
R251
C2
R253
1K69
2V5
L9
U6
R248
C27
C254
R252
C72
R255
1V2D
L7
U4
R18
C22
C25
R136
1K13
C23
R250
4K53
1V
C300
C299
C301
C0402C102J4GACTU
C0402C103K3RACTU

Title		
Temporoc vXilinx Artix7 - Power supply Management		
Size: A3	Number	Revision: 1.0
Date: 5/18/2026		Sheet 10 of 11
File: D:\Bureau\..\PowerSupply.SchDoc		Drawn By: F.PEREZ



Title	Temporoc vXilinx Artix7 - USB Controller	
Size: A3	Number	Revision: 1.0
Date: 5/18/2026		Sheet1of11
File: D:\Bureau\..\USB_Control.SchDoc		Drawn By: F.PEREZ



TestBoard
Temporoc v2
Florent PEREZ
12/2023
TOP
Bottom
Analog_Probe1
Ctest
GND
Trig_ext
U13
J3
JU7
JU6
JU13
U20
U15
Y3
OSC2
U22
U24
U12
JU2
J2
D3
SW4
P1
5V
In32
In63
In62
In31
In0
In1
Temp Sensor
JU20
J5
EXT HV
S1
J4
U19