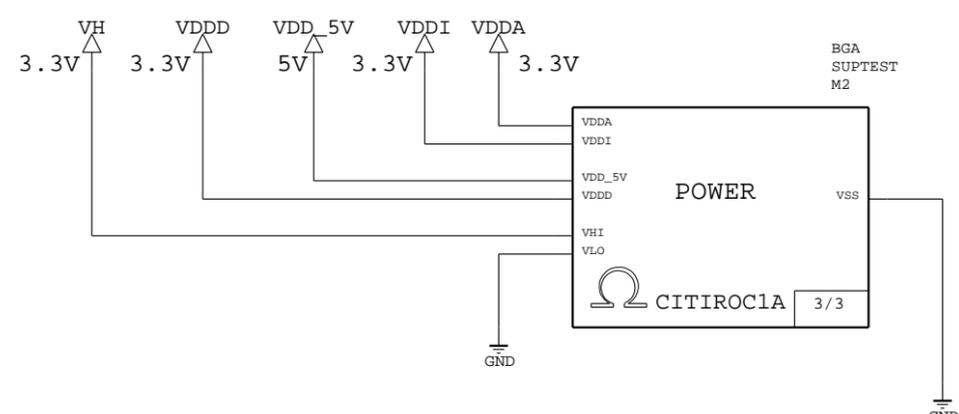
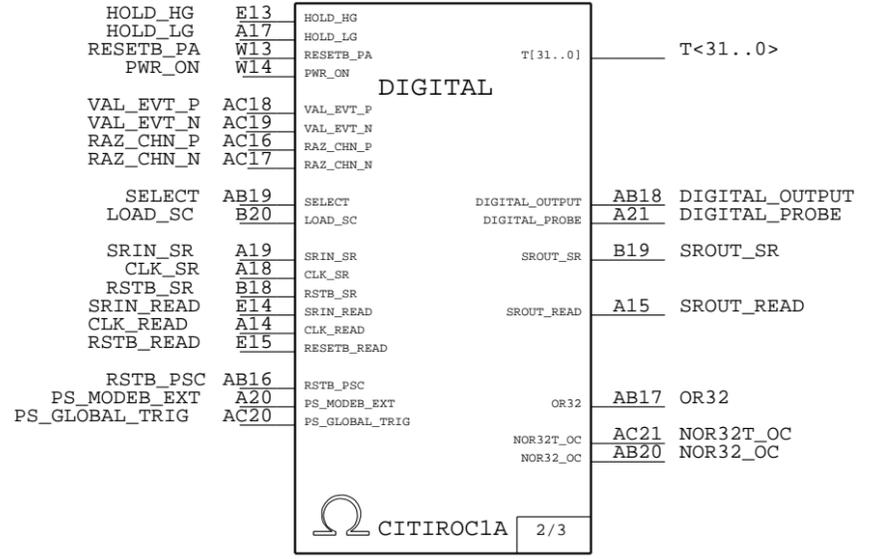
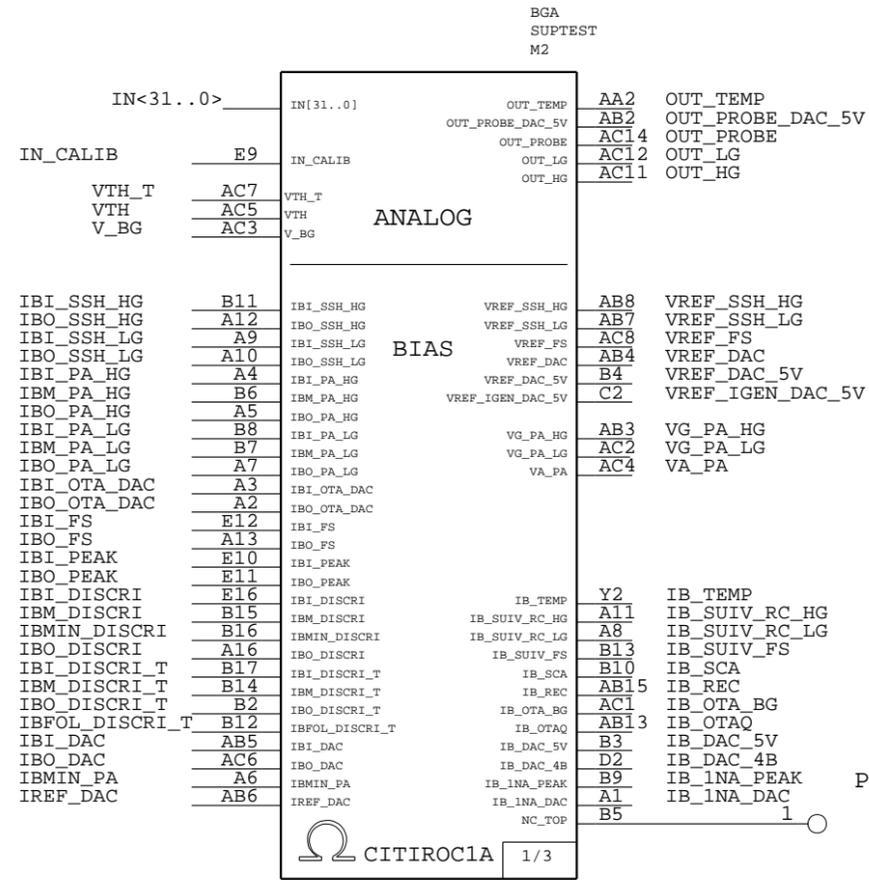
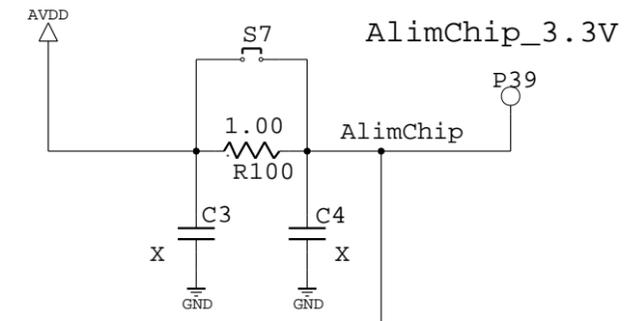


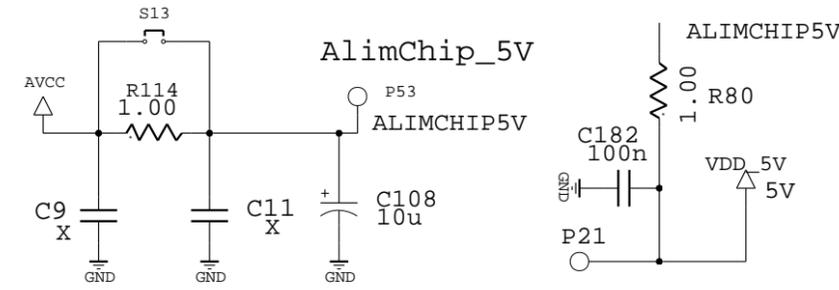
CITIROC



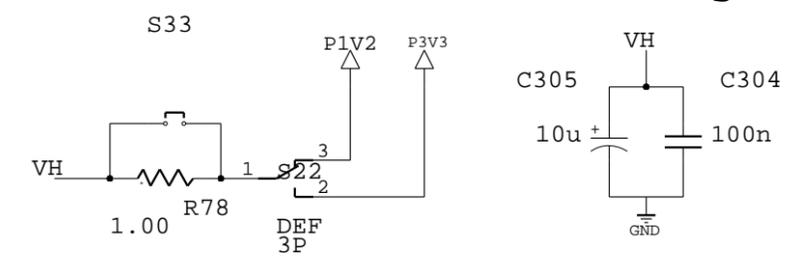
Chip Consumption



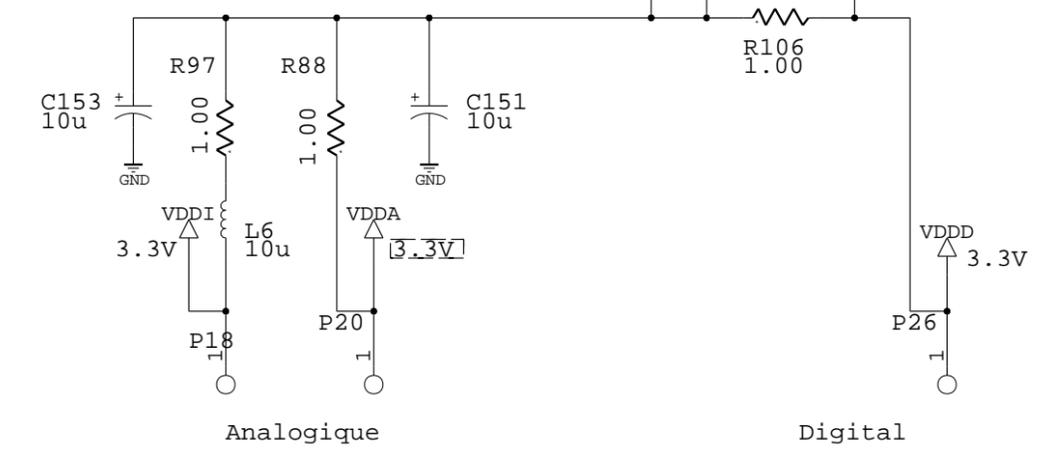
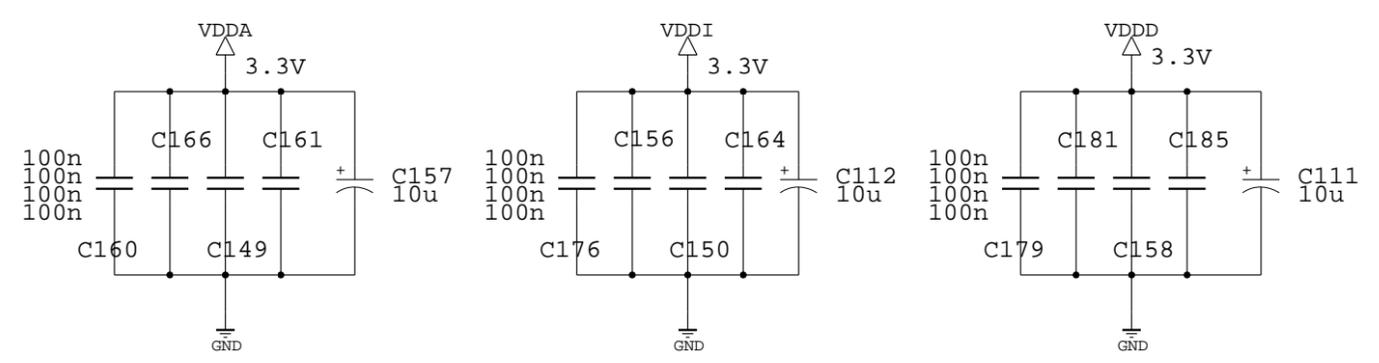
Conso Chip 5V



VH Selection with switch to select Voltage

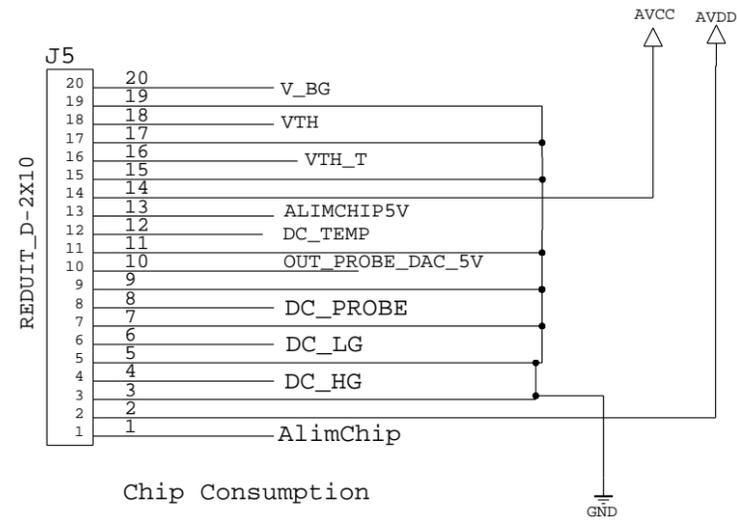


DECOUPLAGE DU VDD (pres du chip)

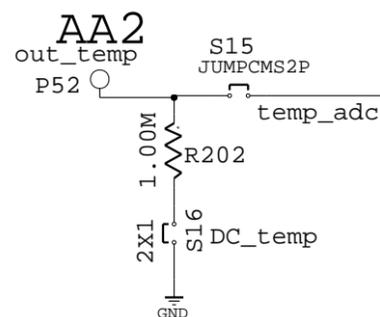
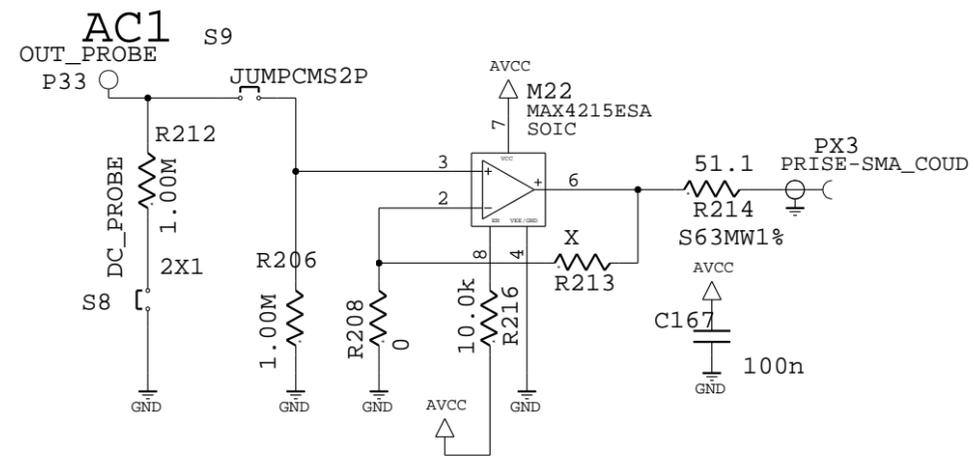


test_citiroc_1a

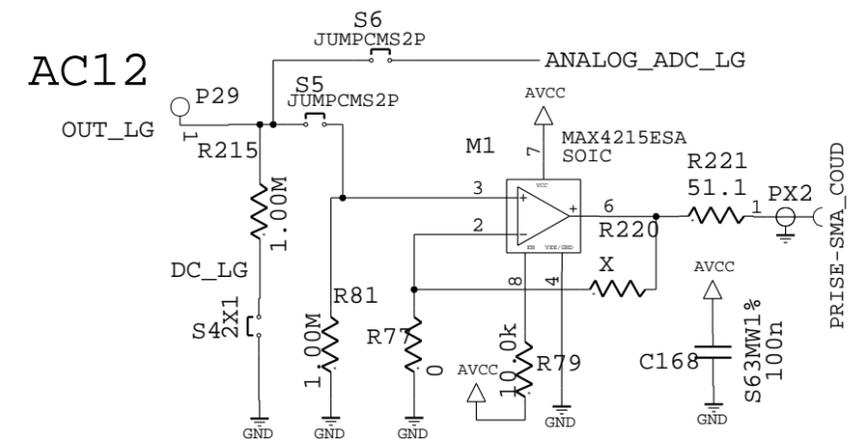
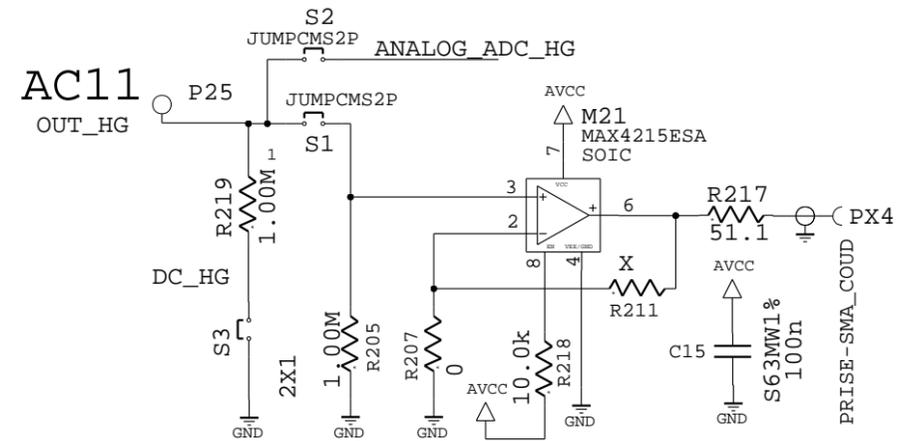
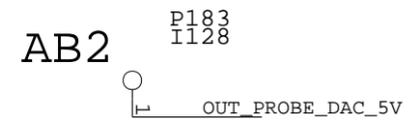
KEITHLEY DMM 2000 - CONNECTOR



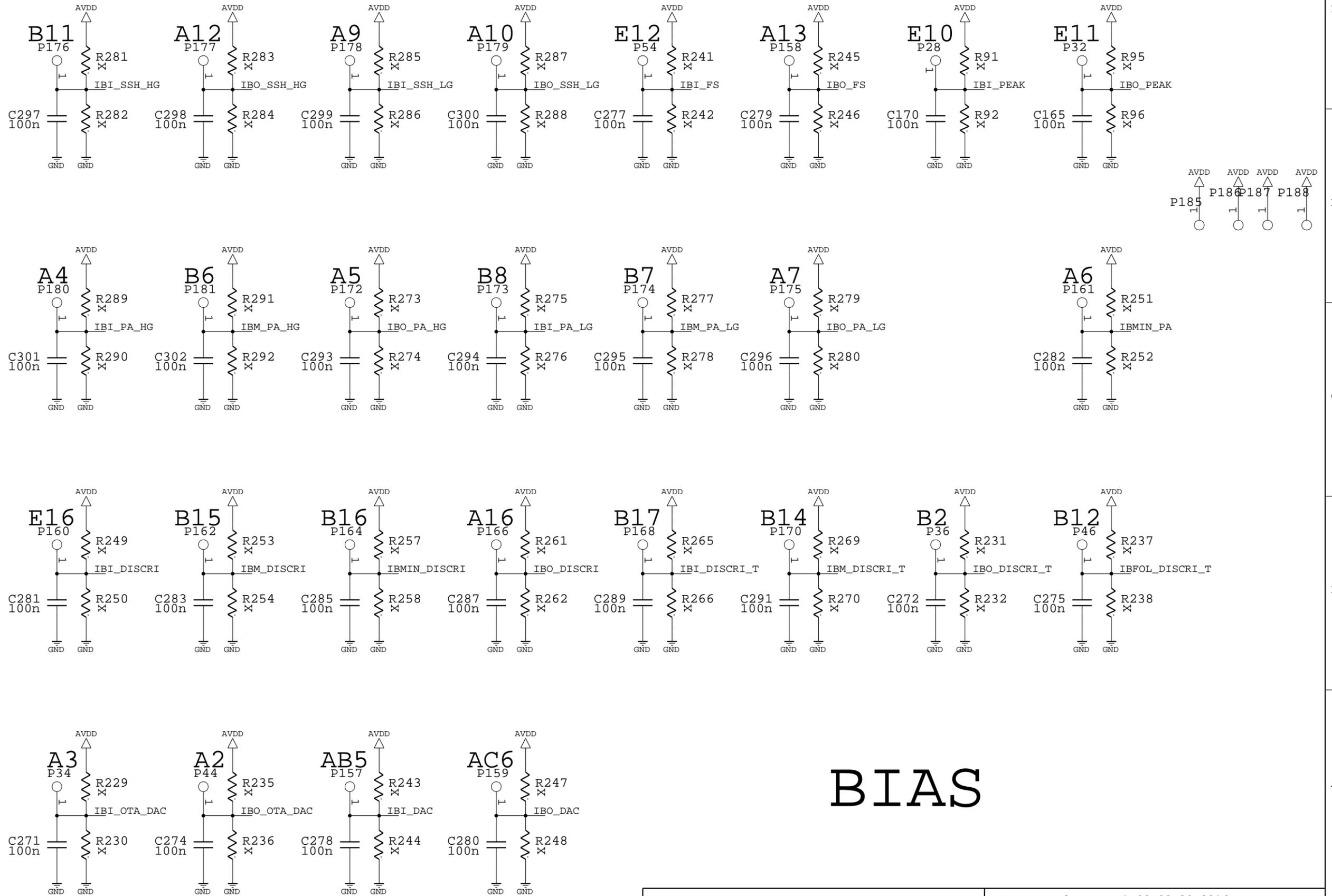
Chip Consumption



ANALOG OUTPUTS

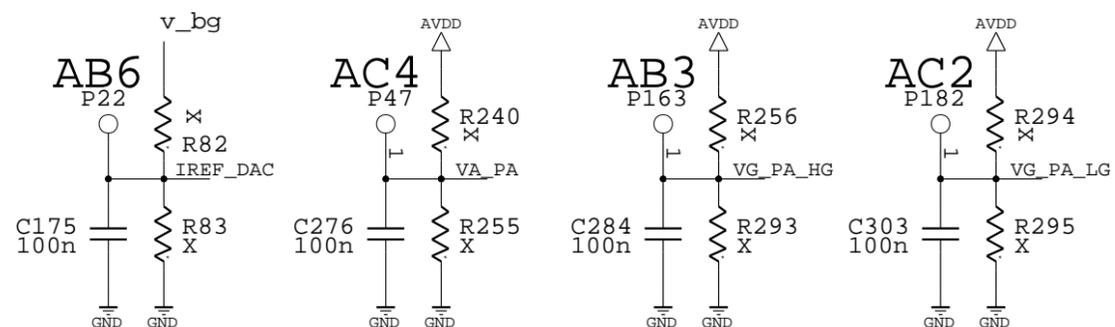
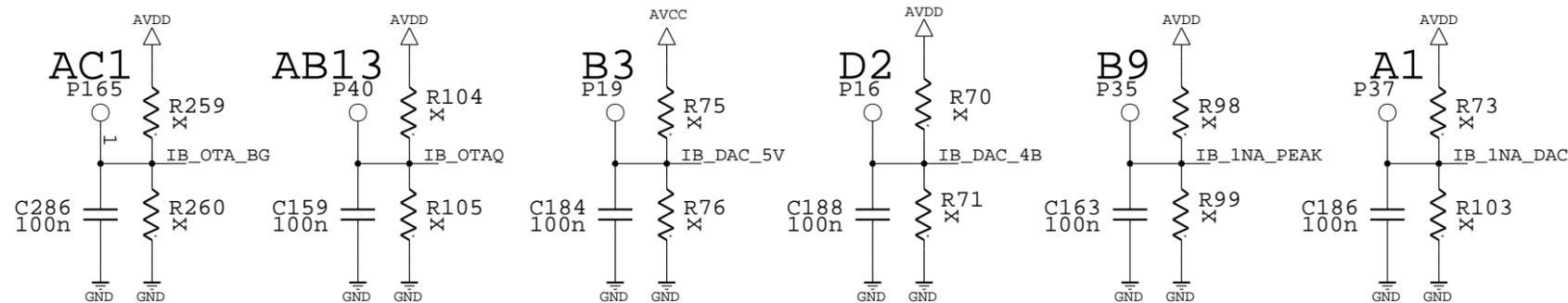
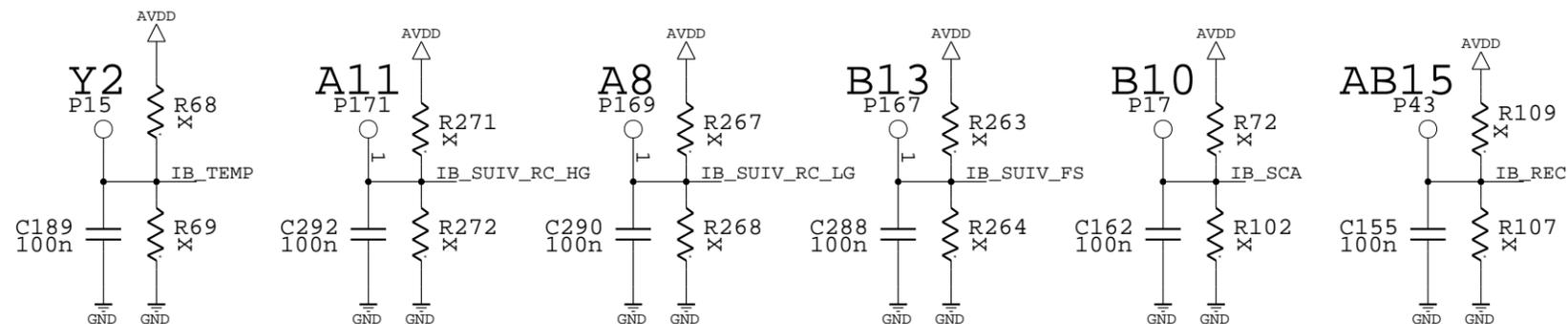
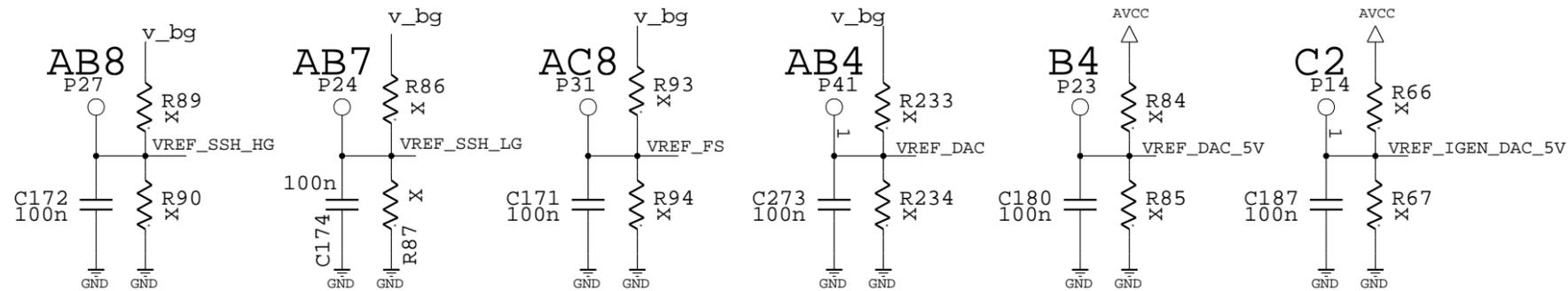


test_citiroc_1a

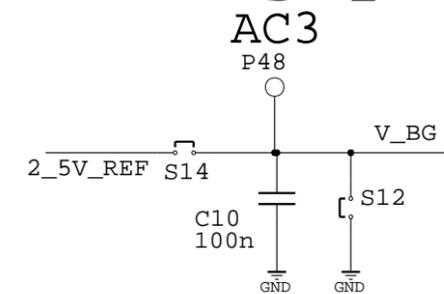


BIAS

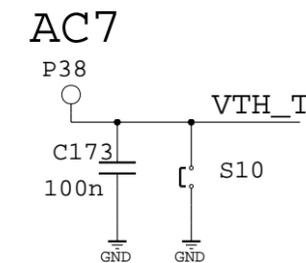
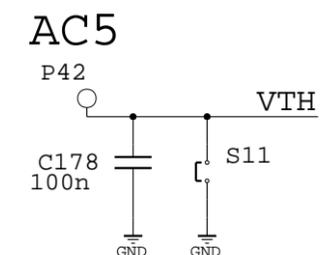
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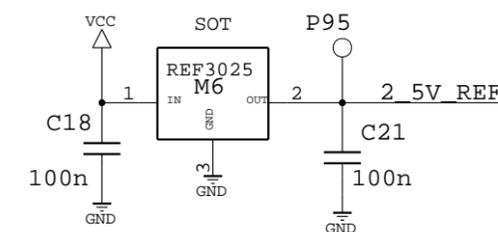
Bandgap



Threshold



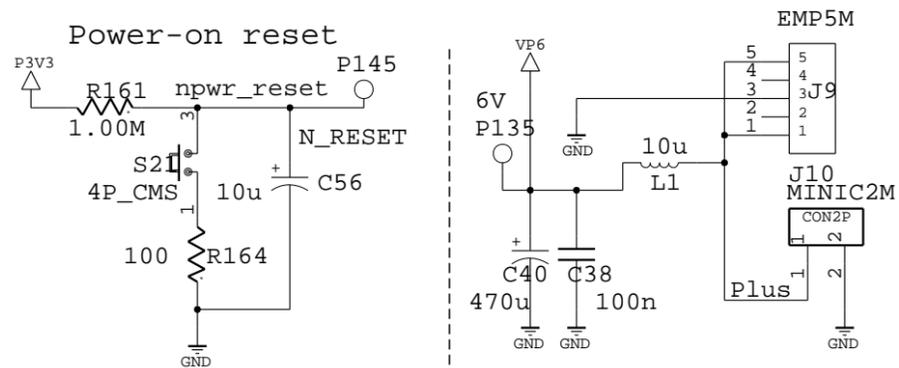
REF. VOLTAGE



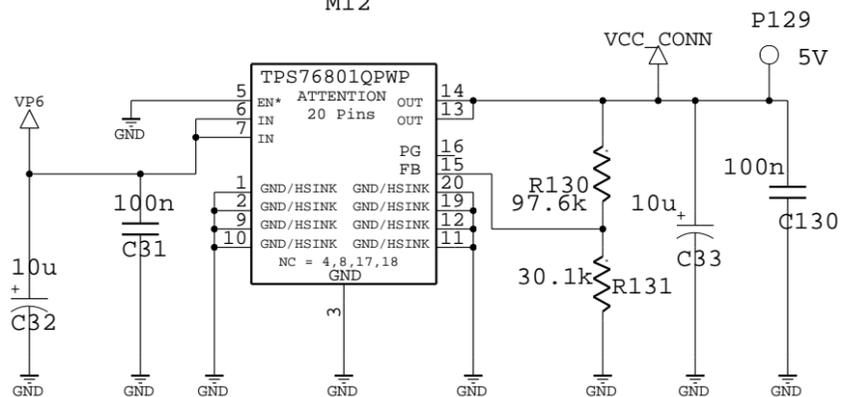
test_citiroc_1a

--- POWER SUPPLY ---

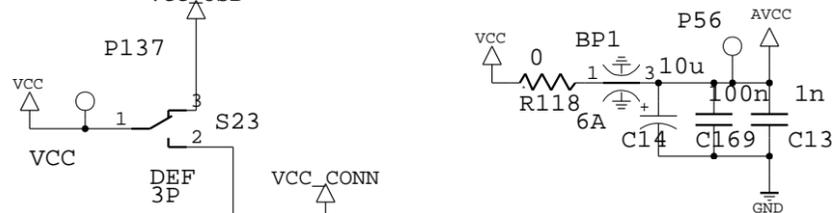
R 0805 (1%) for regulators
 $V_{reg} = 1.1834 * (1 + R1/R2)$ et $R2 = 30.1k$



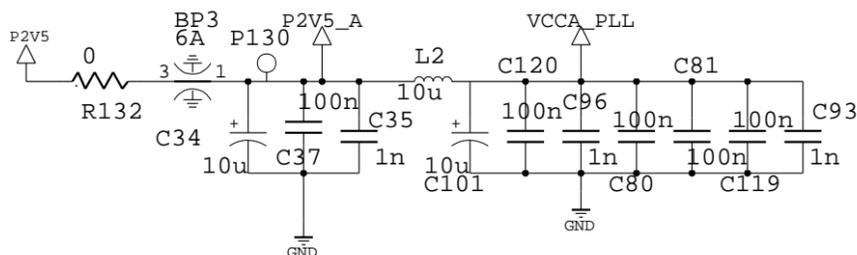
Vcc from power conn.
for Buffers & external ADC



VCC selection
5V for ADC/buffers

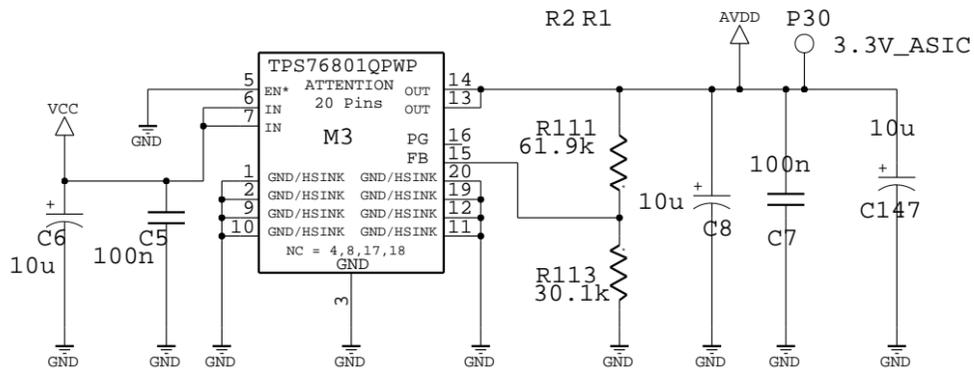


Analog 2V5

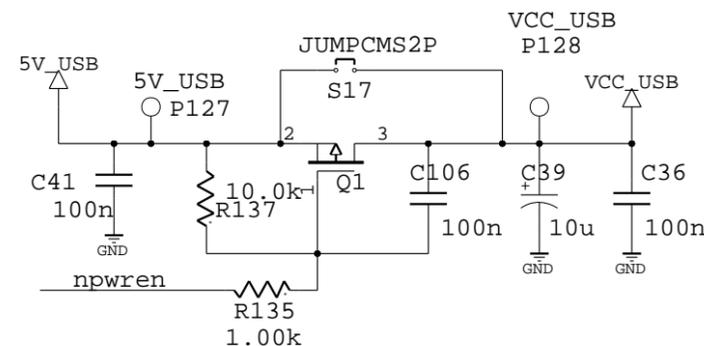


ASIC power supply

ASIC 3.3V

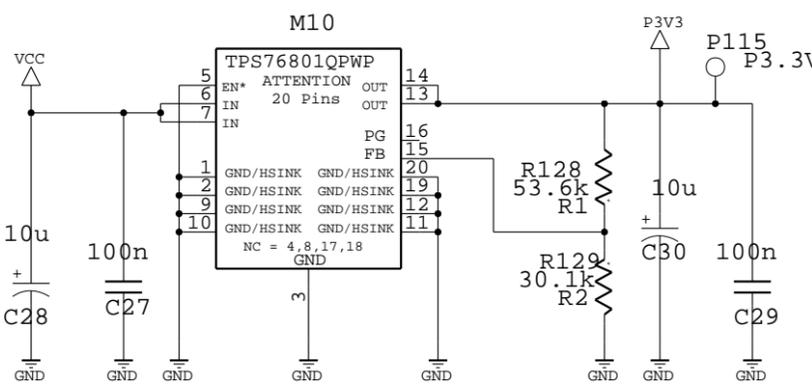


soft power start up
for USB enumeration

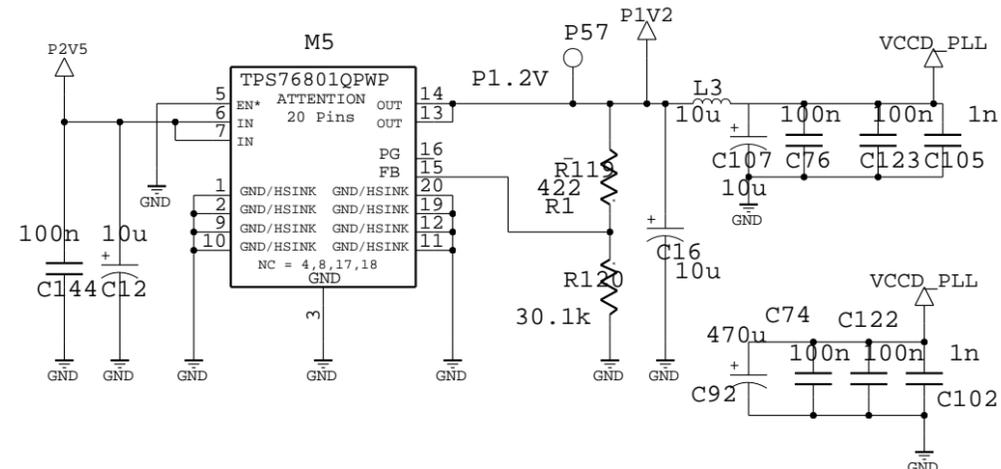


FPGA power supply

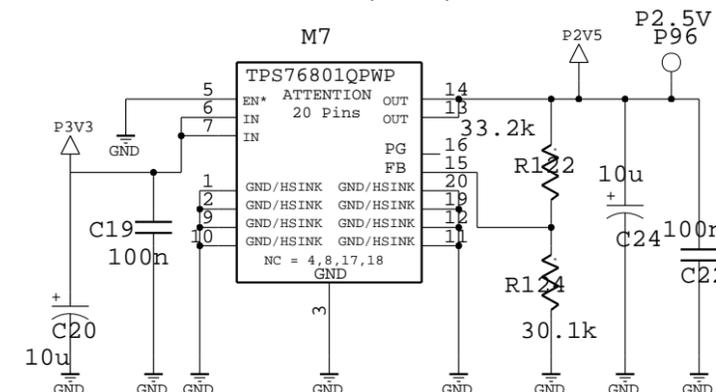
3.3V for banks 1, 2 & 3



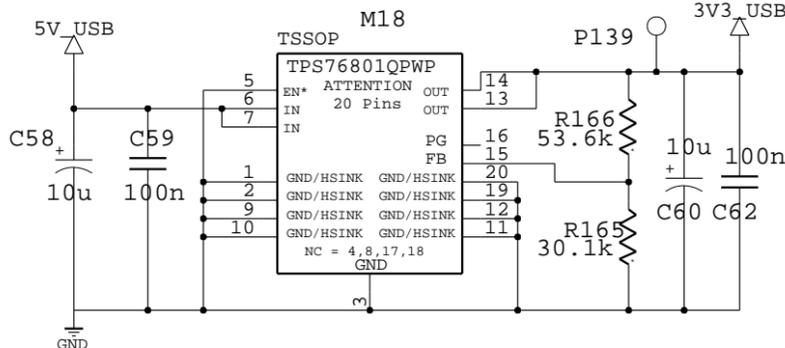
Internal Power Supply



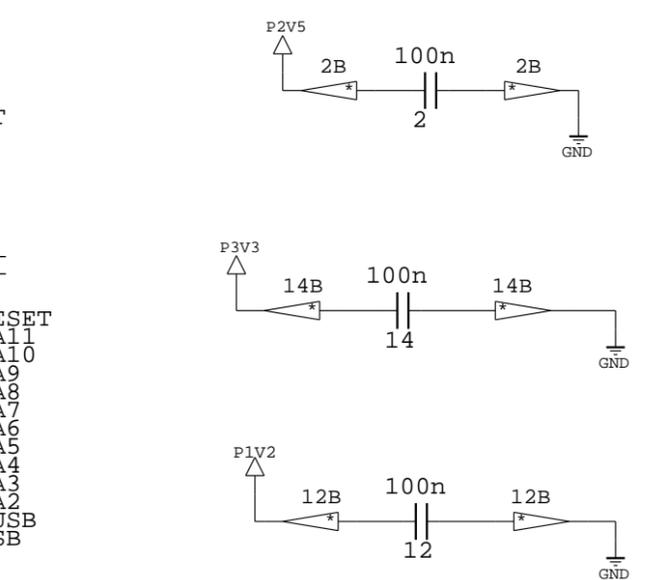
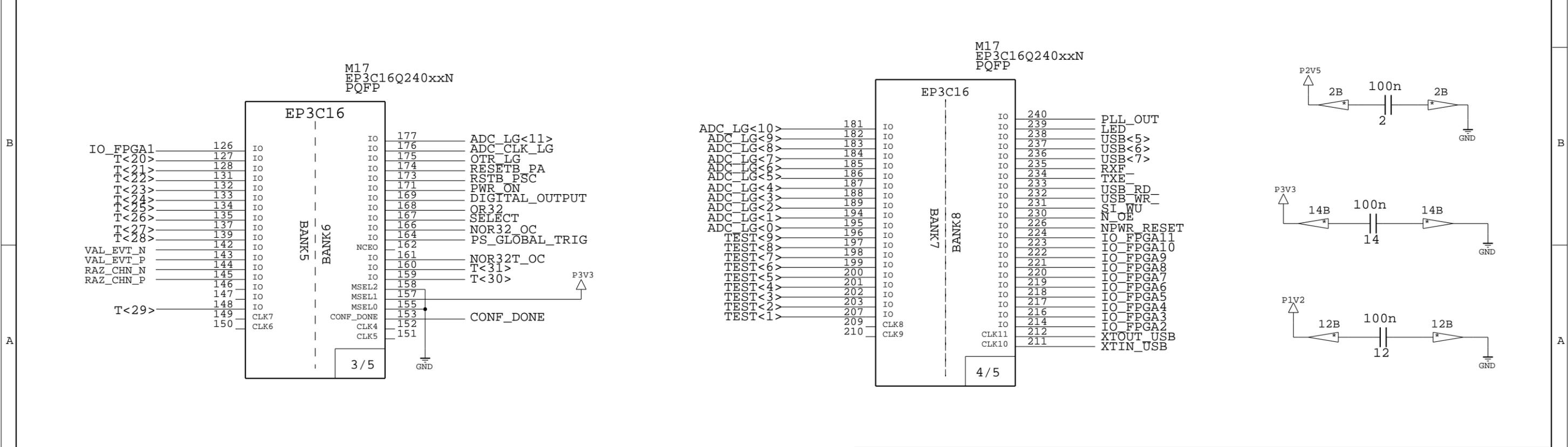
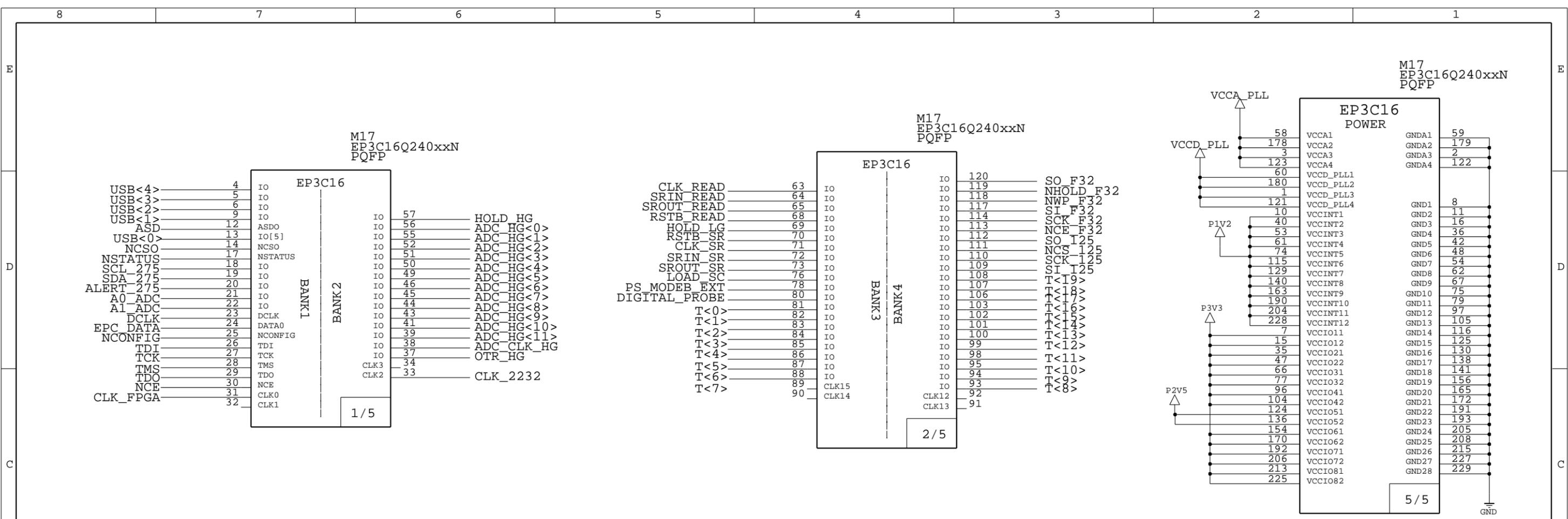
2.5V for bank 4 (LVDS)



3V3 for USB



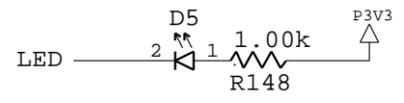
test_citiroc_1a



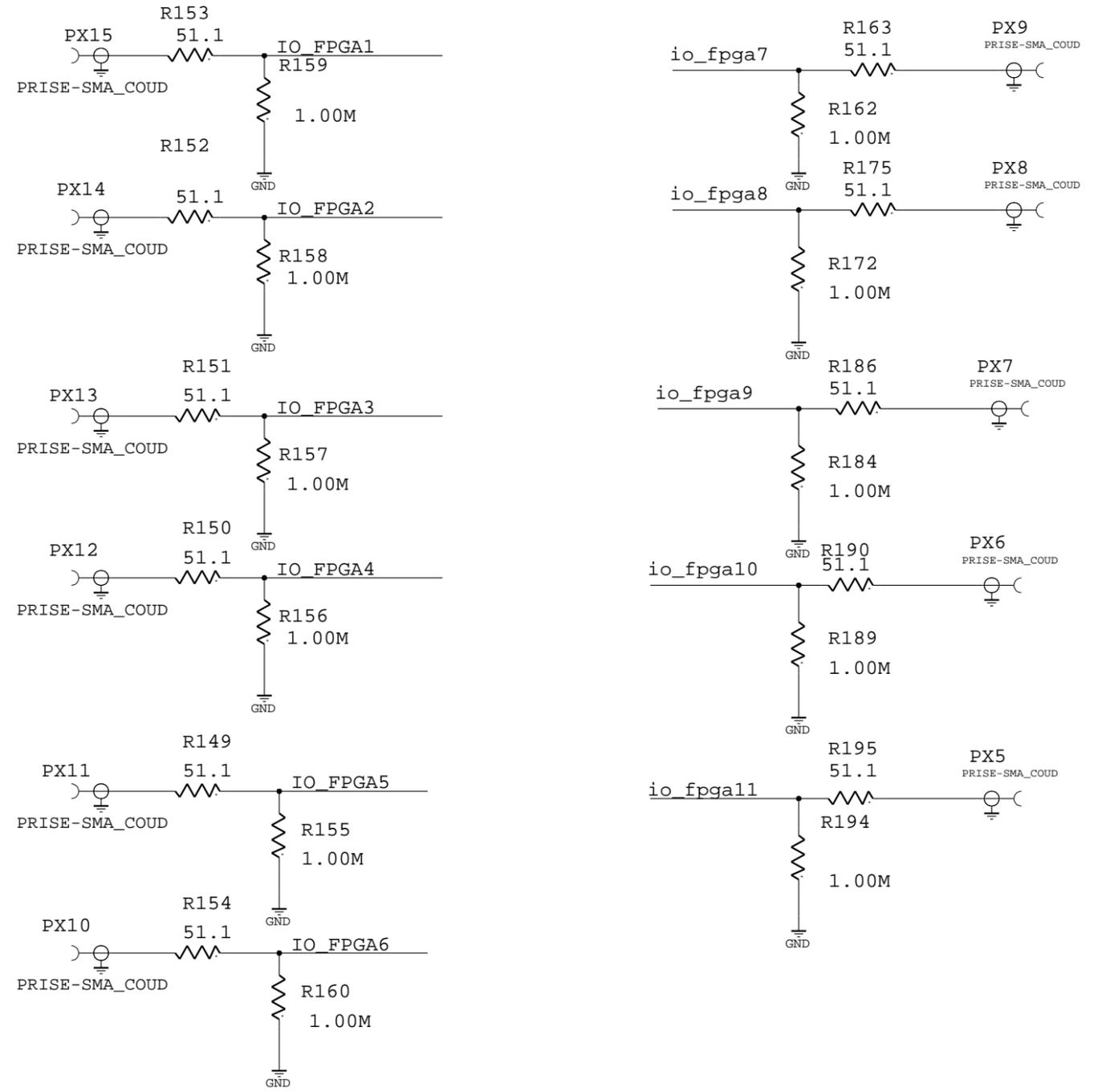
PINS TEST

- TEST<1> —○ P140 T1
- TEST<2> —○ P146 T2
- TEST<3> —○ P141 T3
- TEST<4> —○ P147 T4
- TEST<5> —○ P142 T5
- TEST<6> —○ P148 T6
- TEST<7> —○ P143 T7
- TEST<8> —○ P149 T8
- TEST<9> —○ P144 T9

PLL_OUT —○ P150



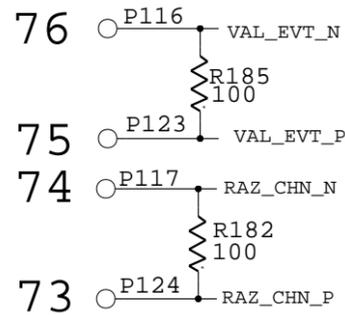
FPGA inputs/outputs



test_citiroc_1a

LVDS INPUTS

ASIC SIDE



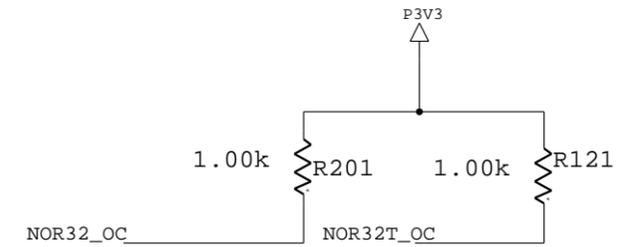
DIGITAL ASIC

T<0>	○ P61	
T<1>	○ P81	
T<2>	○ P100	
T<3>	○ P62	
T<4>	○ P82	
T<5>	○ P101	
T<6>	○ P63	
T<7>	○ P83	
T<8>	○ P102	
T<9>	○ P64	
T<10>	○ P84	
T<11>	○ P103	
T<12>	○ P65	
T<13>	○ P85	
T<14>	○ P104	
T<15>	○ P66	
T<16>	○ P86	
T<17>	○ P105	
T<18>	○ P67	
T<19>	○ P87	
T<20>	○ P106	
T<21>	○ P68	
T<22>	○ P88	
T<23>	○ P107	
T<24>	○ P69	
T<25>	○ P89	
T<26>	○ P108	
T<27>	○ P70	
T<28>	○ P90	
T<29>	○ P109	
T<30>	○ P71	
T<31>	○ P91	

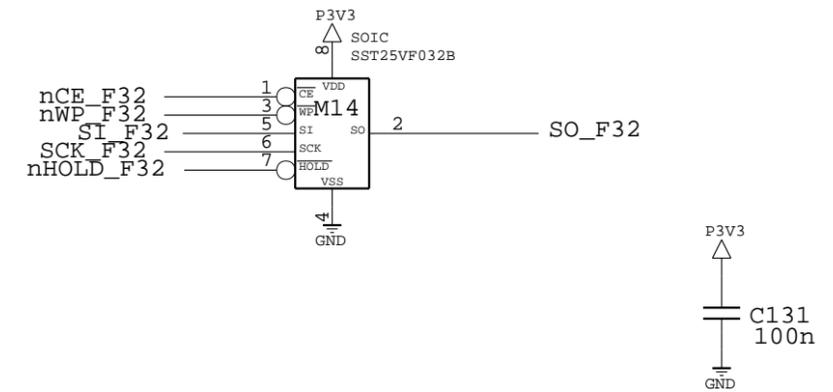
HOLD_HG	○ P58	136
CLK_READ	○ P59	135
SRIN_READ	○ P60	134
SROUT_READ	○ P78	133
RSTB_READ	○ P79	132
HOLD_LG	○ P80	131
RSTB_SR	○ P97	128
CLK_SR	○ P98	127
SRIN_SR	○ P99	126
SROUT_SR	○ P118	125
LOAD_SC	○ P119	124
PS_MODEB_EXT	○ P120	120
DIGITAL_PROBE	○ P121	119

NOR32T_OC	○ P72	83
PS_GLOBAL_TRIG	○ P73	82
NOR32_OC	○ P74	80
SELECT	○ P92	79
OR32	○ P93	78
DIGITAL_OUTPUT	○ P94	77
PWR_ON	○ P110	72
RSTB_PSC	○ P111	71
RESETB_PA	○ P112	70

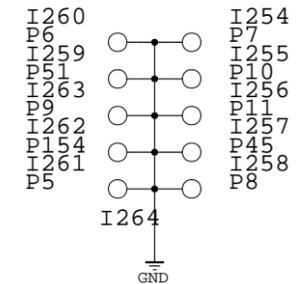
OC OUTPUTS ASIC



External SRAM

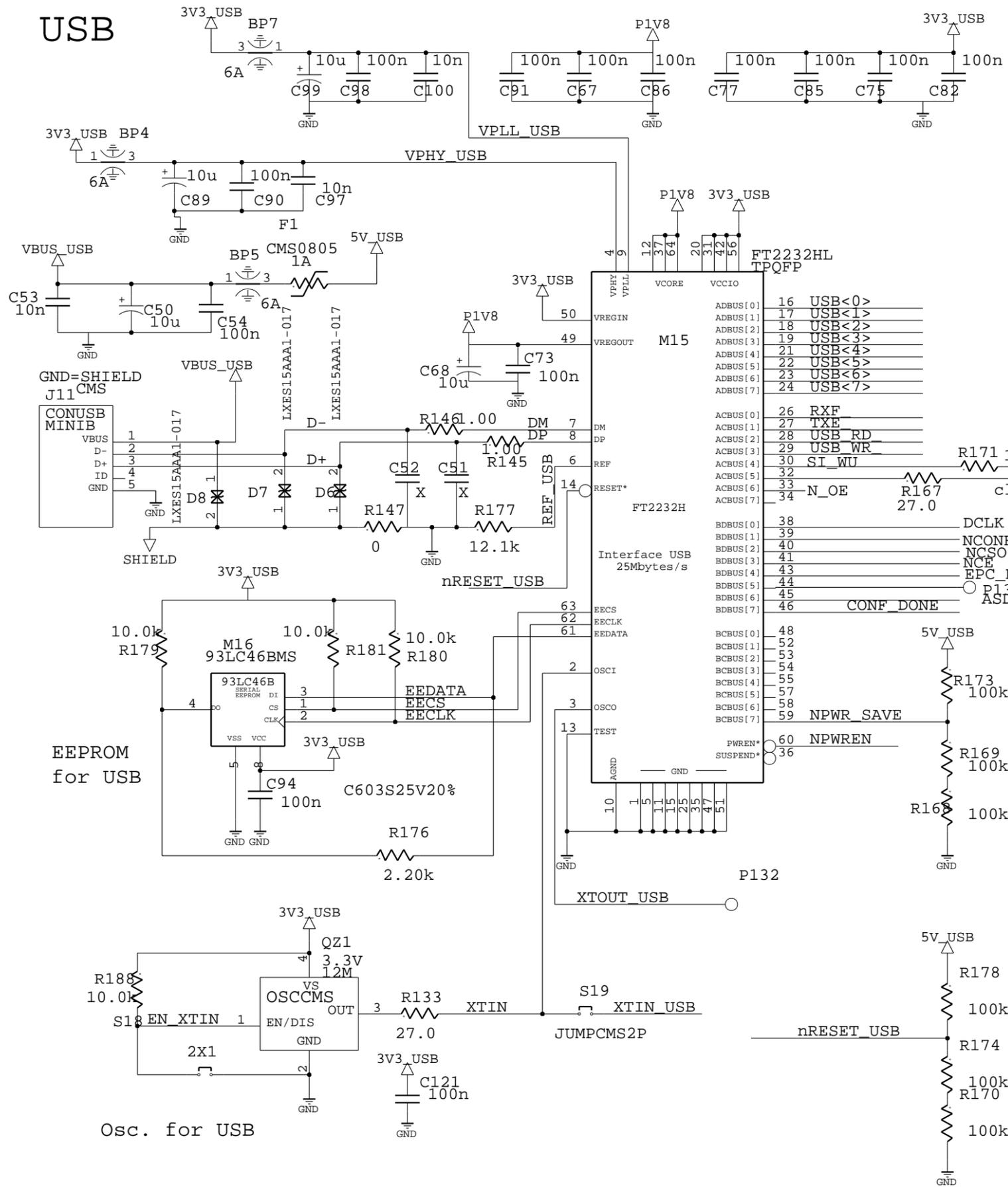


Thru holes ground

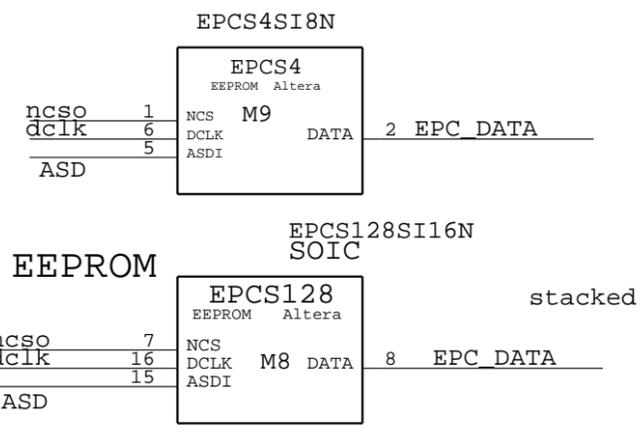
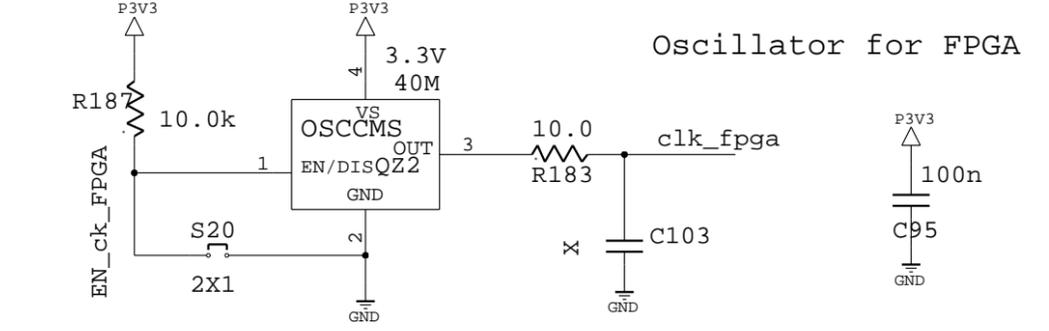


test_citiroc_1a

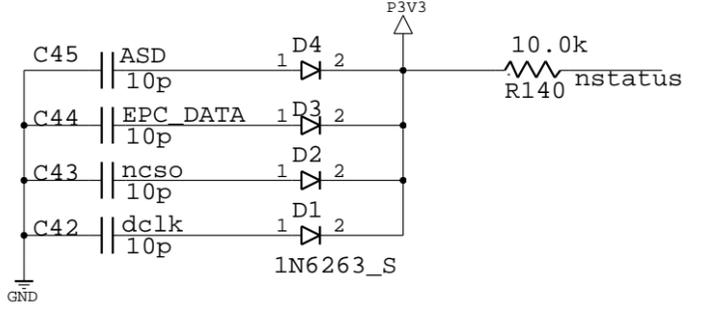
USB



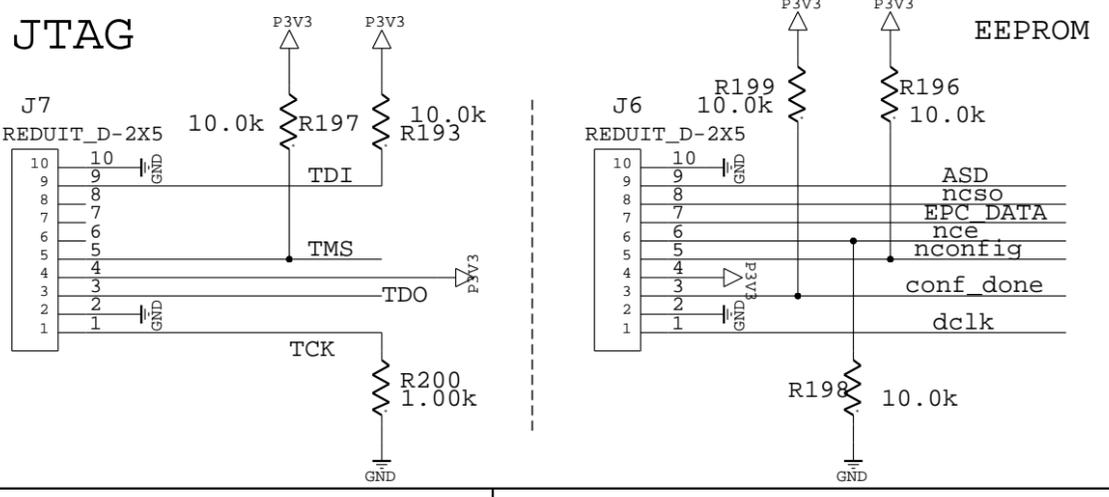
Oscillator for FPGA



FPGA protect

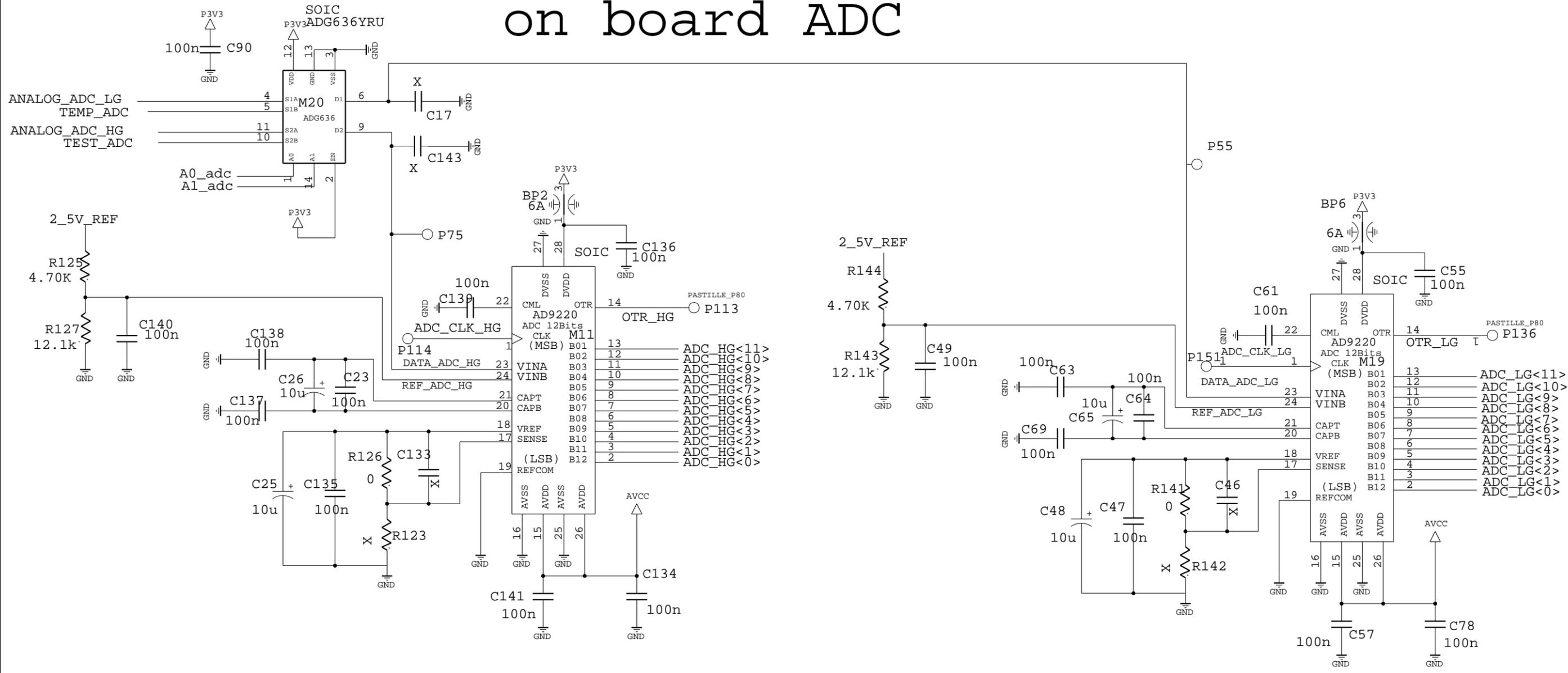


FPGA direct access



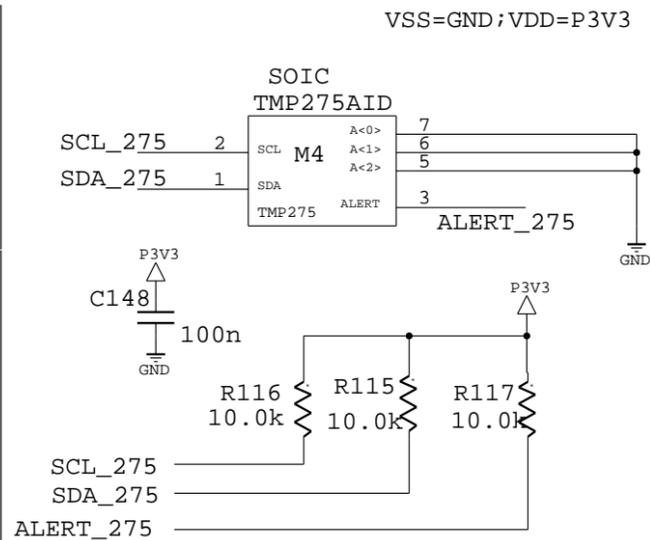
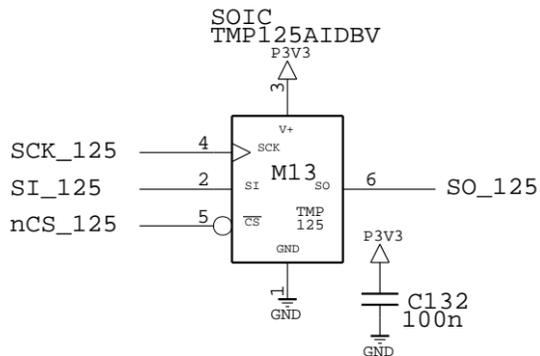
test_citiroc_1a

on board ADC

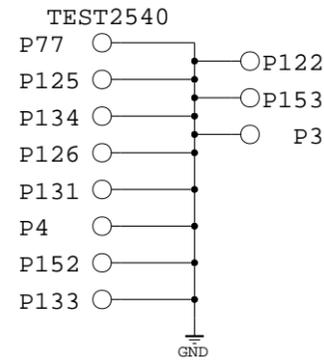


thermal probe

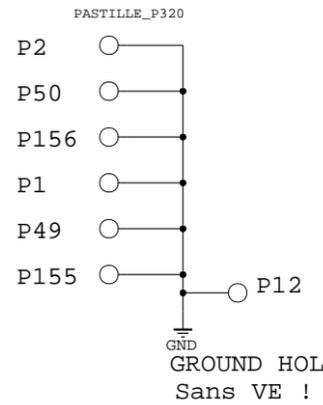
thermal probe



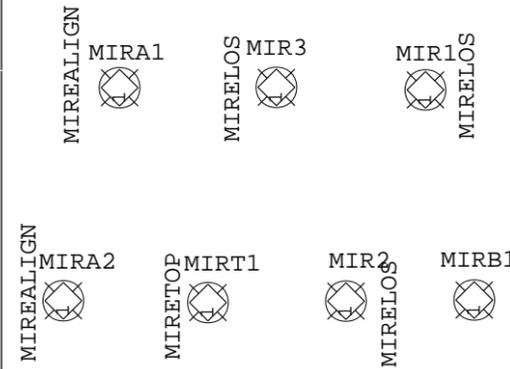
GROUND TEST POINTS



MECANICAL FASTENING HOLES



ALIGNMENT FOR CABLING

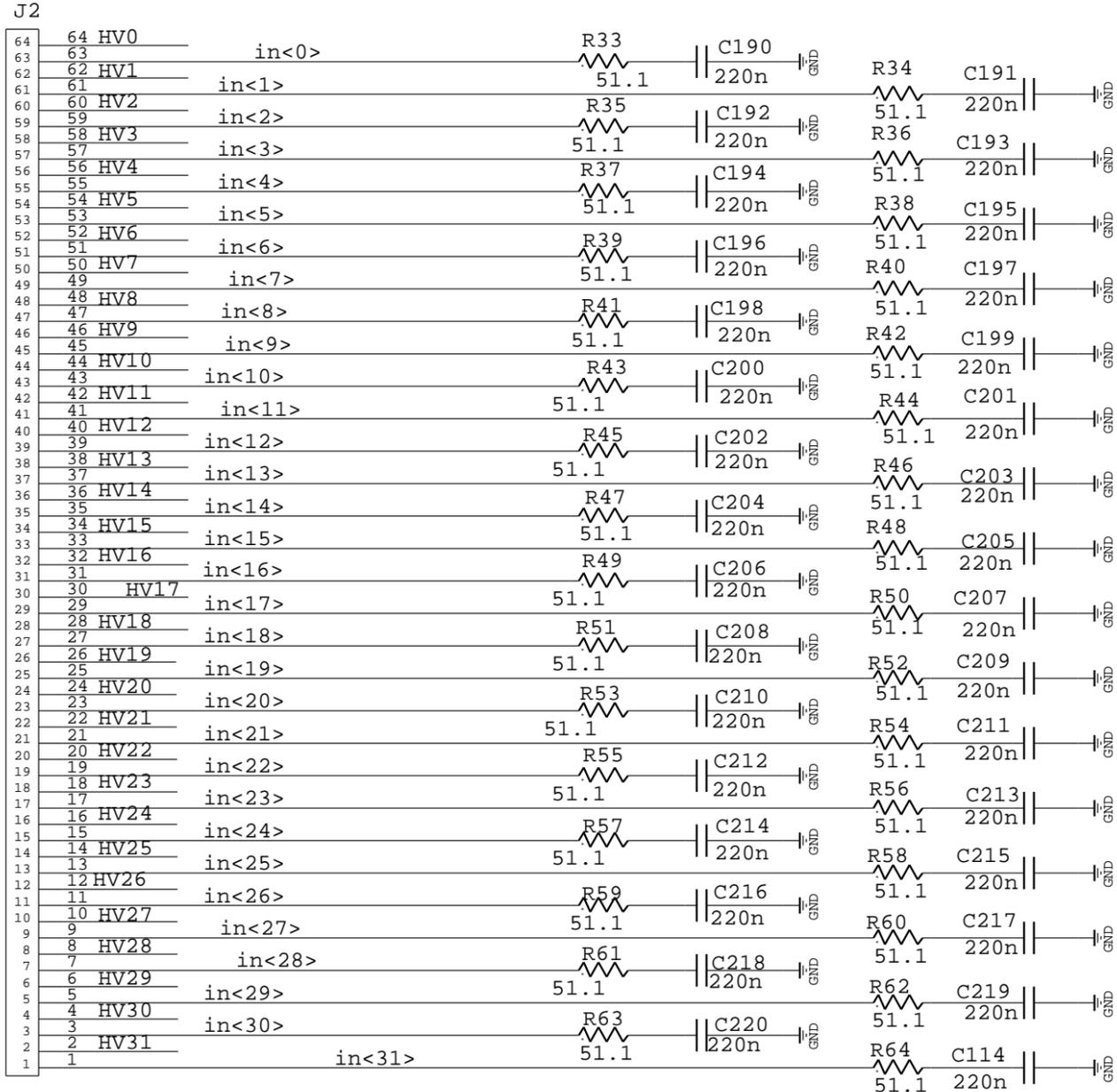


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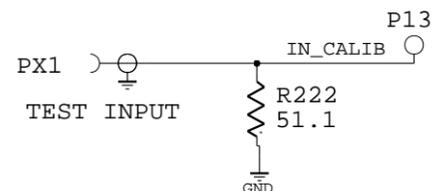
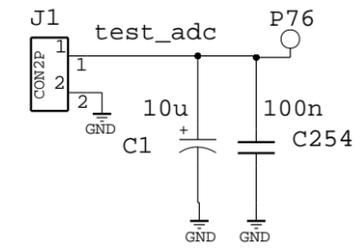
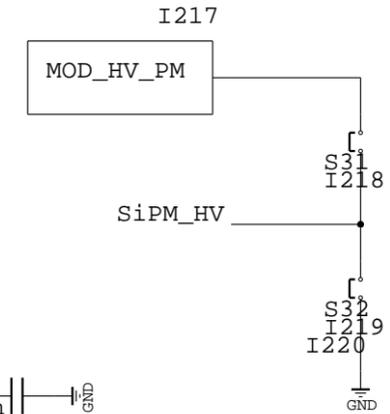
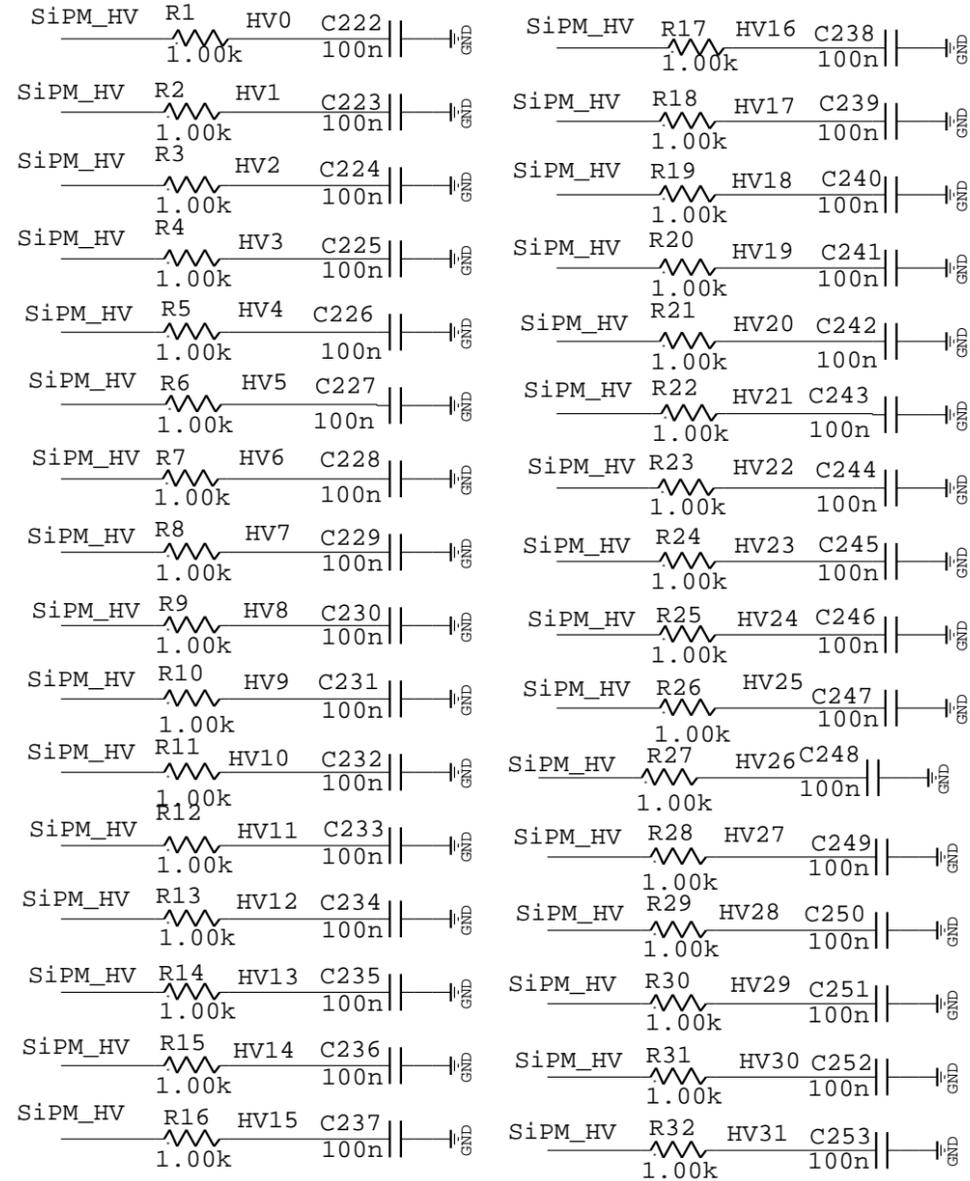
ANALOG INPUTS

Connection to SiPM & HV

SiPM Load

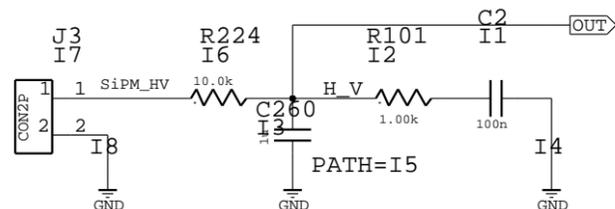


High Voltage filters

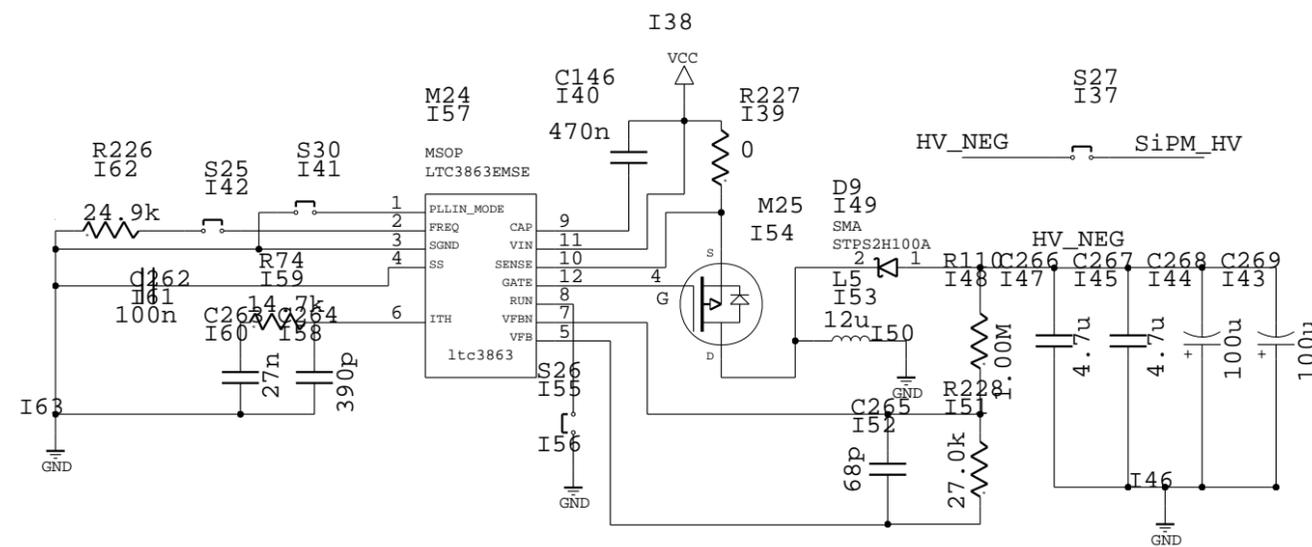
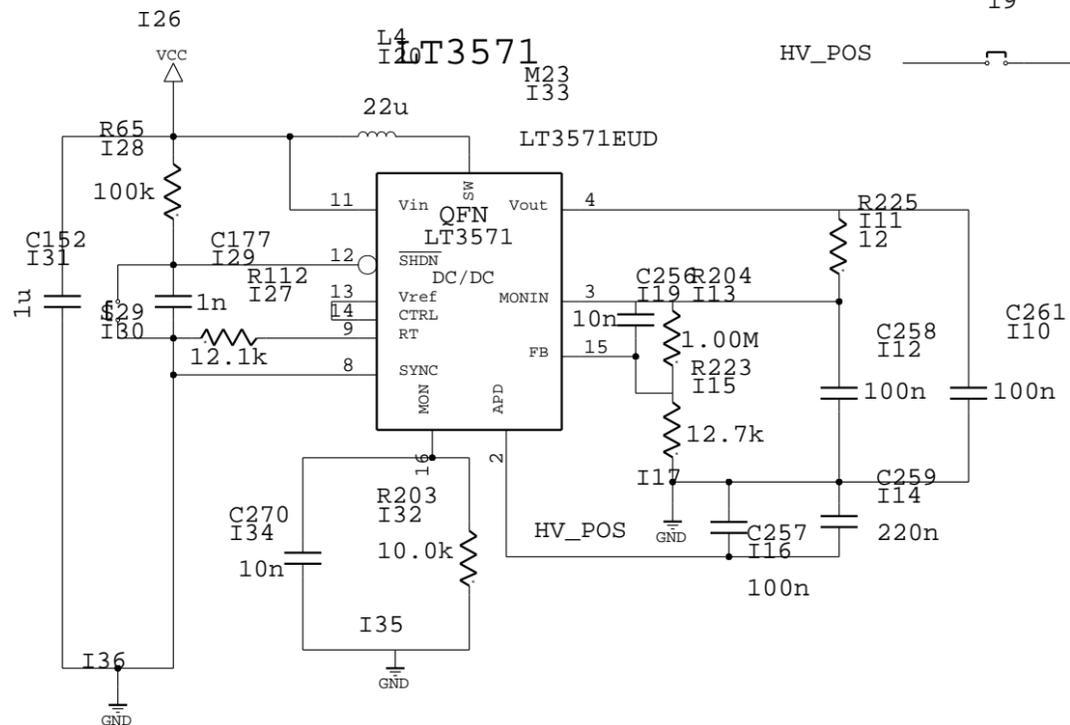
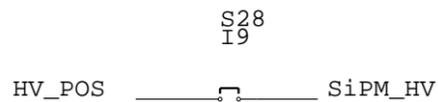
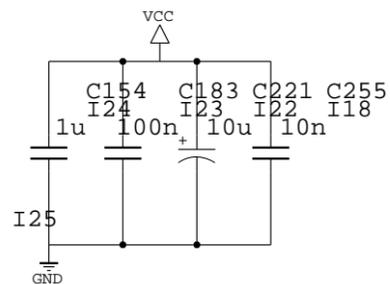


test_citiroc_1a

HV_DECOUPLING



i21 High Voltage



mod_hv_pm

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