Datasheet
GEMROC1 – QFP New Packaging ASIC

GEMROC 1 is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from low **gain detectors (GEMs, Micromegas, …).** GEMROC 1 provides a semi-digital readout with three thresholds tunable from 1 fC to 500 fC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the timestamp from a 24b counter. The three thresholds are set internally by three 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 1 fC input charge. A multiplexed charge measurement up to 500fC is integrated.
The power consumption is 1.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.

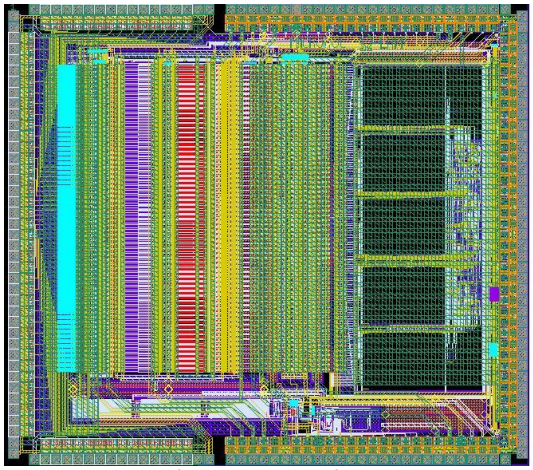

Figure 1 – Gemroc1 layout

Detector Read-Out	Micromegas, GEM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger 1 fC
Timing Resolution	Time stamping 200ns
Dynamic Range	500 fC
Packaging & Dimension	TQFP160
Power Consumption	1.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	Trigger threshold adjustment (10bits), 3*64 trigger masks, multiplexed latched trigger or direct OR64 trigger outputs

They are using Gemroc 1

Industrial application (NDA)

More about Gemroc 1

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1 General description

GEMROC is 64-channel ASIC, designed for reading out 1m^2 MICROMEGAS or GEMs detectors. The front-end and input section have been designed to withstand HV sparks and also to have very low noise performance in order to detect incoming signals down to 2fC.The technology used for designing this ASIC is AMS 0.35um SiGe BiCMOS.

Each channel of the GEMROC chip is made of a very low noise fixed gain charge preamplifier optimised for a detector capacitance of 80 pF, with ability to handle a dynamic range from 1fC to 500fC, two sets of variable shaping time shapers, three comparators and a digital memory block used to store trigger information and event data. Other blocks, like 12-bit DAC, configuration registers, bandgap voltage reference, LVDS receiver are included. All these blocks can be powered on or off (following specific sequences) in order to minimize the static idle power consumption down to nearly zero.

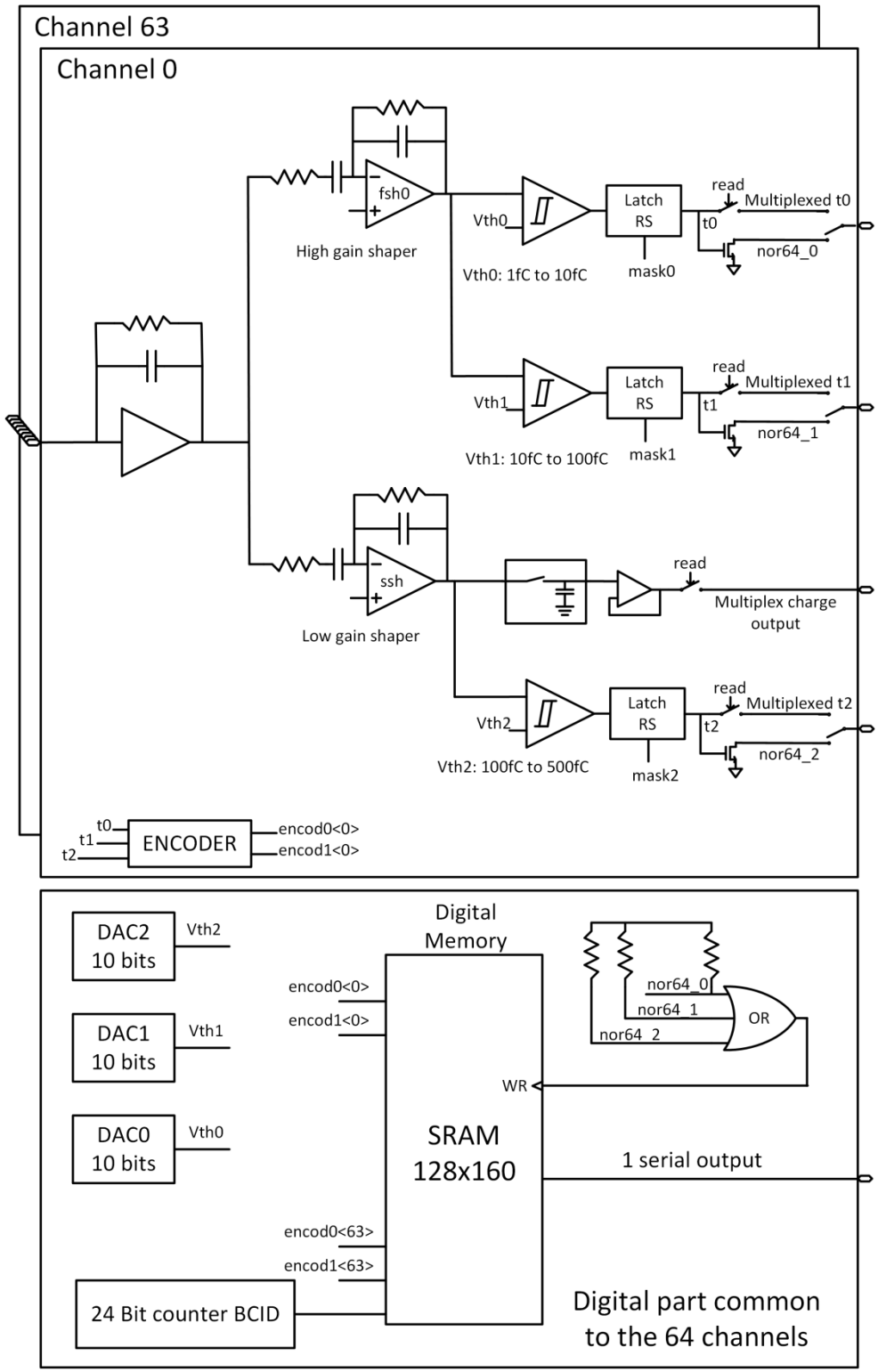


Figure 2 - General ASIC block scheme

2 Maximum ratings

The operating condition of GEMROC1A should not exceed the parameters listed in Table 1.

Parameter	Note	Minimum	Maximum	Unit
Storage temperature range		-40	125	°C
Operating temperature range		-20	110	°C
Power Pin	All power pins	0	3.5	V
Ground Pin	All ground	0	0	V
Analog input		-0.5	VDD+0.3	V
Digital input TTL		-0.5	VDD+0.3	V
Digital input LVDS		-0.5	VDD+0.3	V

Table 1 - Maximum rating operation condition

GEMROC1A electrostatic discharge (ESD) protection is HBM (Human Body Model) compatible on every Pin.

3 ASIC front-end

3.1 Analog channel description

GEMROC1 analog part schematic block is shown Figure 3. From the input, the signal will be amplified by a charge pre-amplifier (denoted as PAC in this document) before sent to High Gain and Low Gain shapers. From High Gain shaper output, the resulting signal will be discriminated with two levels of threshold (Vth0 and Vth1) and two trigger outputs are generated (Ch<n>_trig0 and Ch<n>_trig1). Low Gain Shaper is used to generate a third trigger (threshold = Vth2), denoted as Ch<n>_trig2. Additionally, this shaper can be used for charge measurement, where a track/hold cell with analog output buffer is available for sampling the Low Gain Shaper output.

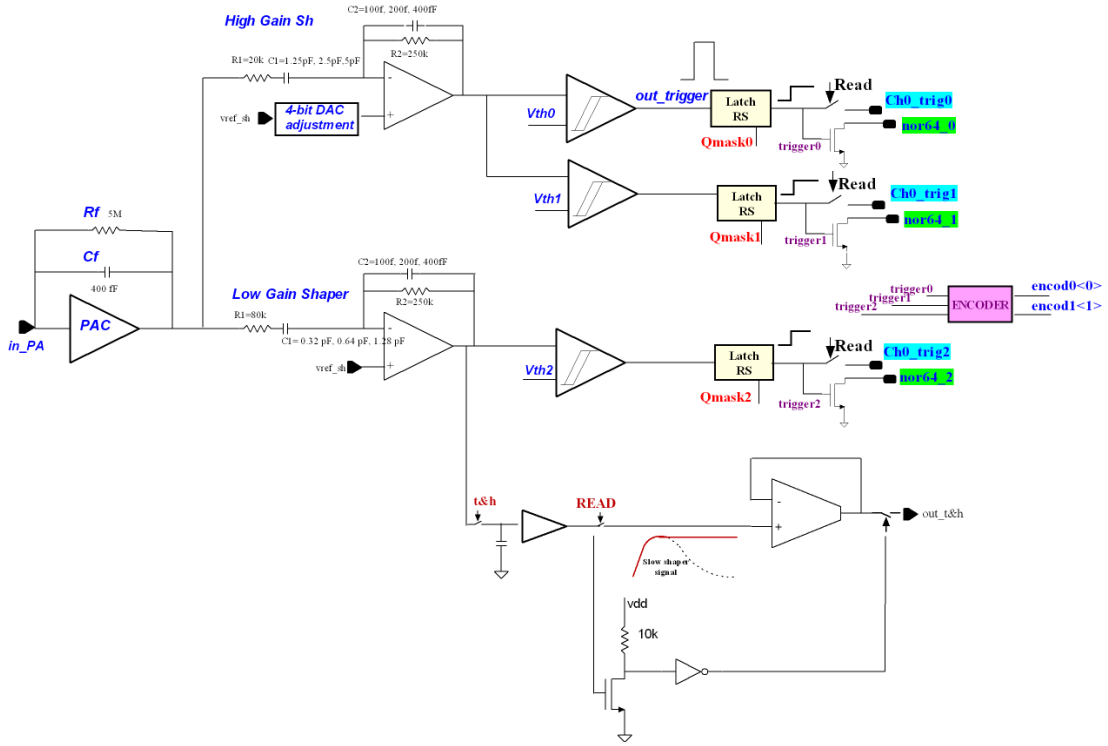


Figure 3 – Gemroc analog part

3.1.1 Preamplifiers Description

Low noise charge preamp optimized for a detector capacitance of 80 pF and a dynamic range up to 500 fC. Fixed feedback network of resistor, Rf=5 MΩ and capacitor, Cf=400 fF are used in the amplification stage.

3.1.2 Shaper description

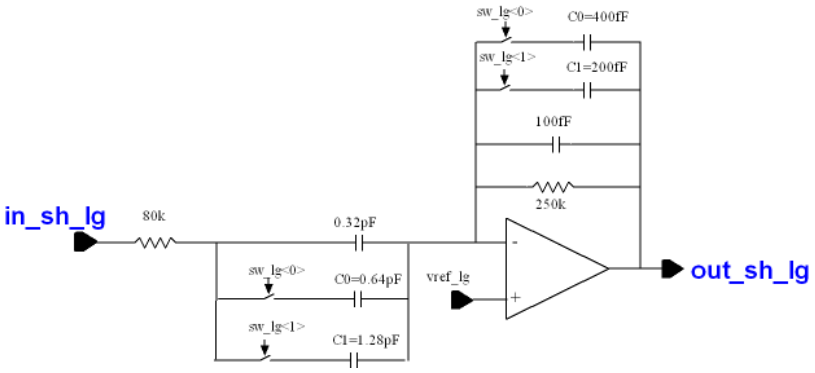


Figure 54 – Low Gain Shaper

A High Gain (HG, gain=4) and a Low Gain (LG, gain=1) CRRC shapers follow the charge preamp.

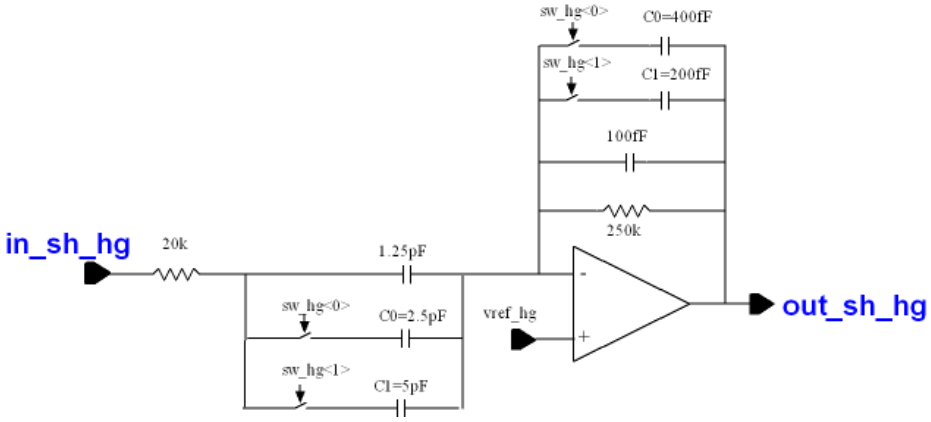


Figure 5 – High Gain Shaper

The time constant can be changed for both using Slow Control parameters (Slow Control bits #69-70 for the Low Gain shaper, Slow Control bit #73-74 for the High Gain shaper) allowing a peaking time of 30ns, 100ns, 150ns or 200 ns as shown on Figure 7.

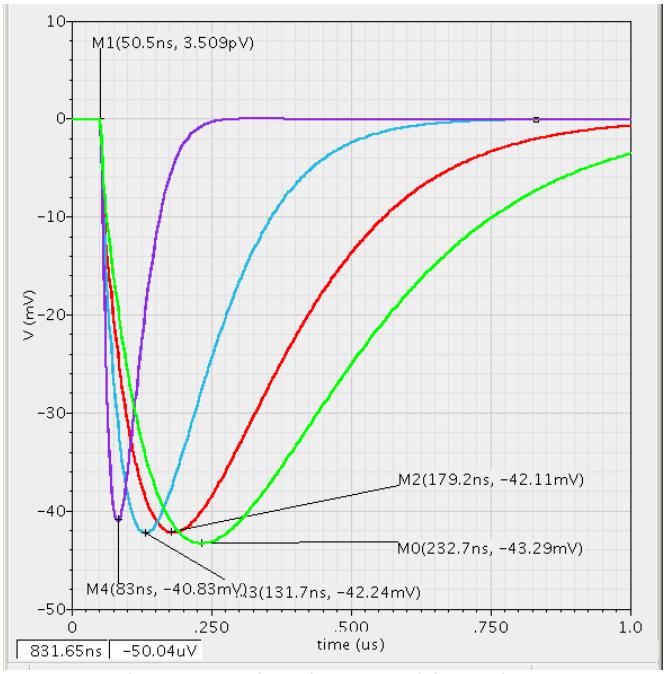


Figure 6 – Step (10mV) response of the HG Shaper

The noise of the PAC followed by the HG shaper (peaking time, tp=200 ns) have been simulated and found equal to 0.25 fC which allows to set the threshold of the discriminator that follow the HG shaper to a very low value such as 2 fC.

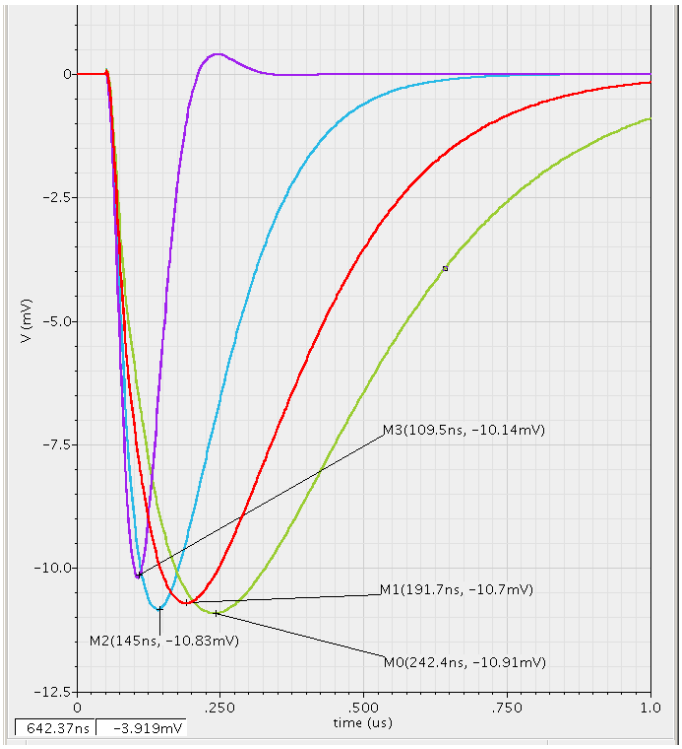


Figure 7 – Step (10mV) response of the LG Shaper

The Low Gain shaper can be also used for charge measurement. Its output is sent to a track and hold buffer to store the charge in a 2 pF capacitor. HOLD signal can be sent from outside (Pin 119 : hold). The output of this track and hold buffer (Pin 129 : out_t&h - refer to Section 7.3) can be read by selecting a channel among the 64 using the read. This output can be daisy chained.

The amplifier of these 2 shapers is slightly different. The transistors of the differential pair of the Low Gain shaper are 10 times bigger than those used in the High Gain shaper. The expected offset with such big transistors is about 350 µV.

For the High Gain shaper, the transistors of the differential pair are rather small and the offset (ASIC wide) can be compensated by trimmable reference voltage (Refer to Section 3.1.3).

3.1.3 4-bit DAC for HG shaper reference voltage trimming

There is a 4-bit DAC per channel to trim the reference voltage of the High Gain shaper and thus compensate its offset. This DAC is made of 4 switched current sources (Slow Control bits #75-330).
With a 14k resistor and a 52nA reference current, the slope is 700µV/DAC unit and the maximum value is 10.9mV. The resulting value is subtracted from the 2.2V base reference voltage.

The reference current can be changed using an external resistor.

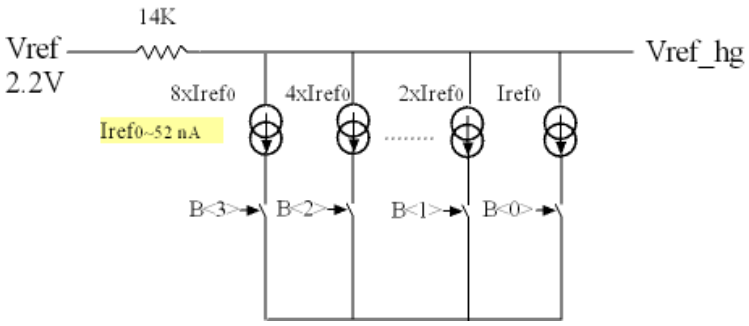


Figure 8 – 4bit_dac schematics

The resulting trimmable reference voltage for HG shaper is as the following:

- LSB : 0.7mV/DAC Unit
- Range : 2.2 V to 2.189V

3.1.4 Discriminators and triple 10bit-DAC

The shapers are followed by 3 discriminators: the High Gain shaper by the Discriminator0 and Discriminator1 and the Low Gain shaper by Discriminator2. Their corresponding thresholds Vth0, Vth1 and Vth2 are set thanks to three sets of 10-bit DACs. By default, Vth0 is set around 2fC, Vth1 around 20fC and Vth3 around 200 fC.

The threshold output calculation is as the following :

Out_dac= Vref_dac + 80K x Iref x(B<0>x2 + B<1>x1+ … +B<8>x1/128 + B<9>x1/256)
with Vref_dac=840 mV and Iref=7.8 µA

The resulting DAC[1] output is the following :

- LSB : 2.43mV/DAC Unit
- Range : 840 mV to 2.9V

Bb<0>, Bb<1> … Bb<9> are set using the Slow Control parameters:

- Slow Control bits #542-551 : for Bb<0>, Bb<1> … Bb<9> settings of DAC0 (Vth0)
- Slow Control bits #552-561 : for Bb<0>, Bb<1> … Bb<9> settings of DAC1 (Vth1)
- Slow Control bits #562-571 : for Bb<0>, Bb<1> … Bb<9> settings of DAC2 (Vth2)

[1] DAC dynamic range optimisation: Iref to be divided by 2. Add external 200k between Pin 73 and V_BG.
→ LSB : 1.37 mV/DAC Unit; Range : 940mV to 2.34V.

3.2 Trigger Interface

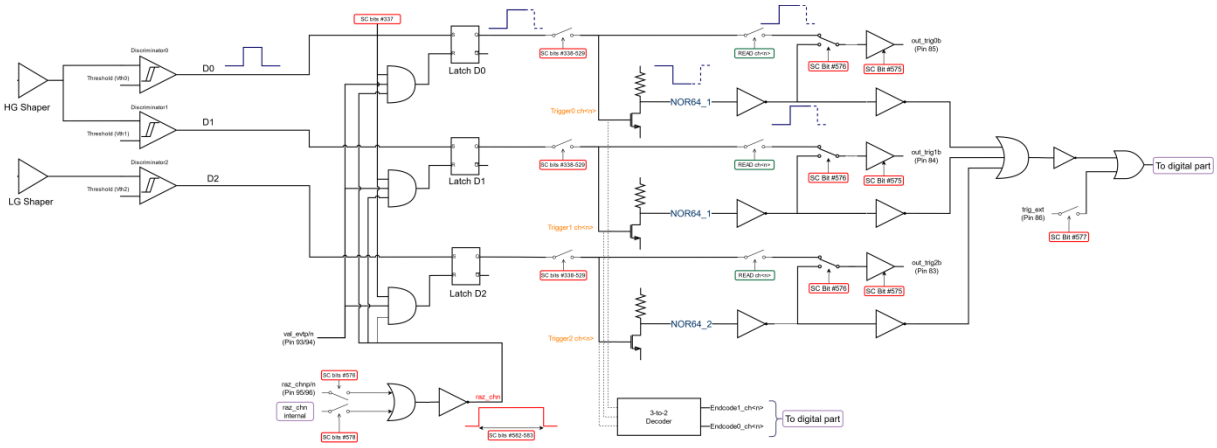


Figure 9 – Trigger interface

Figure 9 illustrates various options available for the triggers, before it reaches the digital side of the ASIC. Although the trigger information is sent (through a 3-to-2 decoder) to the digital block for data acquisition and readout, there are few options available to users for controlling and observing the triggers.

Firstly there are 3 outputs (Open Collector) which users can use for trigger observation, either as a NOR gate of all triggers or multiplexed triggers (Accessible through Read register):

- Pin 83, out_trig2 : Output for Trigger2
- Pin 84, out_trig1 : Output for Trigger1
- Pin 83, out_trig0 : Output for Trigger0

The usage of these outputs can be controlled using the following Slow Control bits:

- Slow Control bit #572, trig2b (nor64_2) : Trigger2 NOR enable to digital block
- Slow Control bit #573, trig1b (nor64_1) : Trigger1 NOR enable to digital block
- Slow Control bit #574, trig0b (nor64_0) : Trigger0 NOR enable to digital block
- Slow Control bit #575, EN_trig_out : Trigger Open Collector outputs enable
- Slow Control bit #576, disc_or_or :Trigger Open Collector outputs selection (Trigger NOR or Read register, Section 7.3)

Additionally, there is an input which can be used as external trigger for bypassing the internal triggers and send it to digital part. The input and associated Slow Control bit are the following:

- Pin 86, trig_ext : External trigger input
- Slow Control bit #577, trig_ext validation : Internal or external triggers to digital block

The triggers can be masked using either Slow Control bits or specific inputs:

- Pin 93-94, val_evtp/n : Fast masking (ASIC wide), LVDS input
- Slow Control bits #338-529, Mask discri0,1,2 ch0-63 : Channel-per-channel and for each trigger available

Additionally, the triggers can be set into latched mode and reset once latched the trigger using the following inputs and Slow Control bits:

- Pin 95-96, raz_chnp/n : LVDS input for external latch reset ("raz_chn")
- Slow Control bit #337 , rs_or _discri : Discriminators latch
- Slow Control bit #578, raz_chn_int validation : Internal "raz_chn" enable to analog block
- Slow Control bit #579, raz_chn_ext : External "raz_chn" enable to analog block
- Slow Control bits #582-583, Sel_raz1,0 : Internal "raz_chn" width

The operation of the trigger latch is described in the following section.

3.2.1 Trigger Latch ***reset ("raz_chn") operation***

For each channel, the 3 discriminators outputs (D0, D1, D2) needs to latched during the acquisition phase (initiated by Pin 92 : StartAcq – Refer to section 0). After the data acquisition and readout phase, the trigger latch is release by a reset signal (denoted as "raz_chn") generated by the digital part of this ASIC.

This reset has variable width which is recommended to be set by matching the chosen peaking time of HG shaper (refer to section 3.1.2). The purpose of this recommendation is in order to have optimum reset width and also to avoid "re-triggering" phenomena. Re-triggering due to shorter latch release reset is illustrated in Figure 11. Latched discriminator output is denoted with "RS output"-purple plot, and the latch release reset is denoted with "raz_chn"-cyan plot. The latch release reset has been purposely chosen at 75 ns, shorter than 200ns chosen peaking time for HG shaper.

The latch release reset width selection is set through the Slow Control parameters (Slow Control bits #582-583, sel_raz0 &1) and the resulting width is listed in the following table.

Slow Control bits #582, Sel_raz1	Slow Control bits #583, Sel_raz0	Raz width
0	0	75 ns
0	1	250 ns
1	0	500 ns
1	1	1 µs

Figure 10 – Trigger latch reset width selection

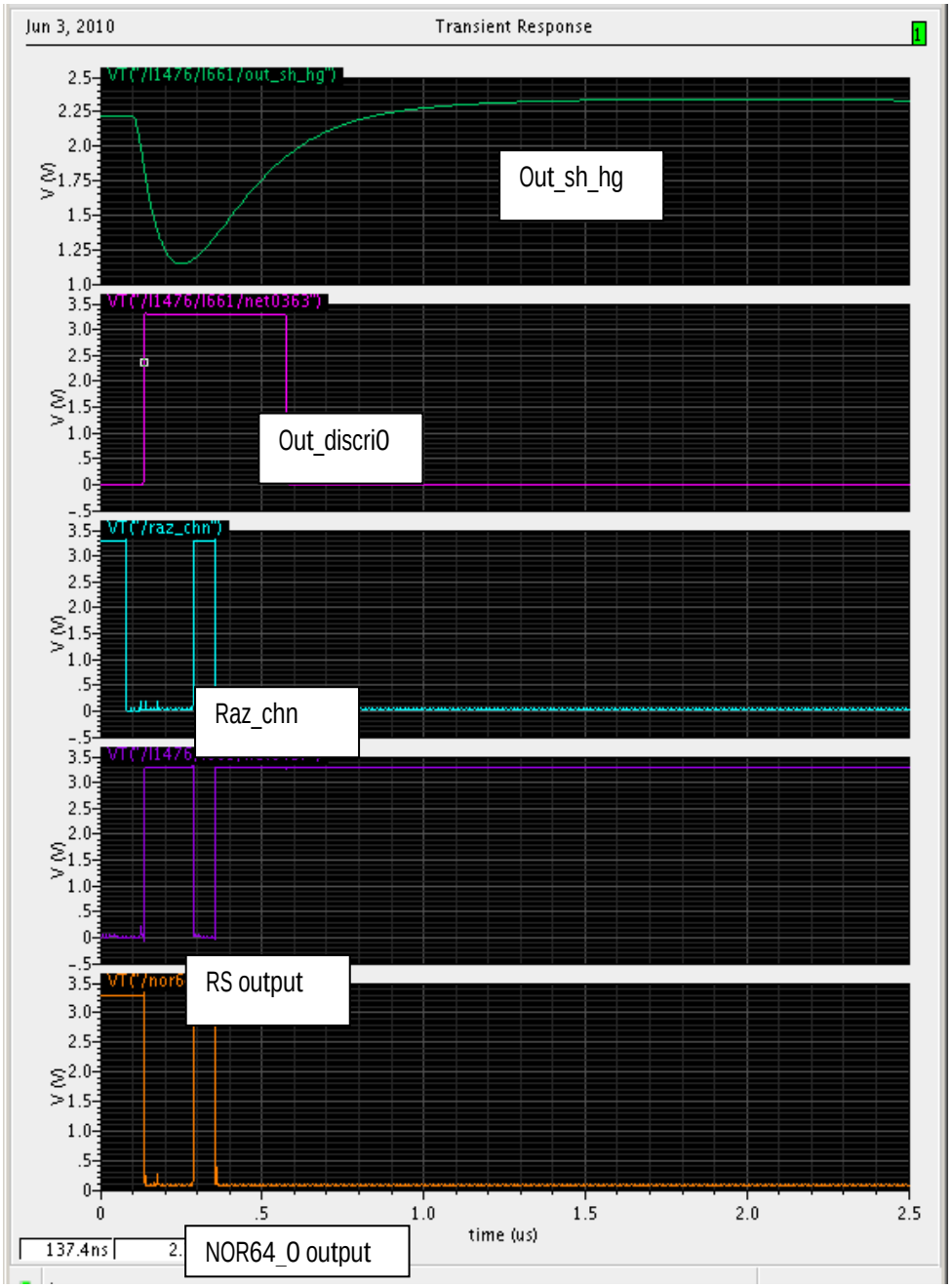


Figure 11 – Simulation of trigger latch reset "raz_chn" width shorter than HG shaper shaping time

Additionally, this internally generated latch release reset can be bypassed with external input and the following Slow Control parameters:

- Pin 95-96, raz_chnp/n : LVDS input for external latch reset ("raz_chn")
- Slow Control bit #578, raz_chn_int validation : Internal "raz_chn" enable to analog block
- Slow Control bit #579, raz_chn_ext : External "raz_chn" enable to analog block

3.2.2 Trigger decoding

A 3-to-2 encoder is used to deliver trigger encoded data for each channel: encod0 and encod1 are stored in the digital memory which during data acquisition phase.

Discriminator2 (D2)	Discriminator1 (D1)	Discriminator0 (D0)	enc <1>	enc <0>
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Figure 12 – Trigger information encoded for data acquisition

4 ASIC backend

This ASIC integrates a memory of 160 bits with 128 of depth in order to store encode trigger data (2*2bits for each channel), event id (BCID - 24-bit) and also Slow Control header (8-bit). The readout is initiated by a command from a data acquisition system (DAQ or FPGA). The data are sent out via redundant Open Collector lines.

In order to use the digital backend in order to readout the digital memory (RAM) embedded in this ASIC, the trigger latches are required to be in latched mode. This can be set through "rs_or_discri" or Slow Control bit #337 :

Slow Control bit #337, "rs_or_discri" = '1'

Simplified block schematic of the backend is shown in the following figure. This part is driven by two clocks :

- Fast Clock for state machines : 40MHz
- Slow Clock for readout : 1 or 5 MHz

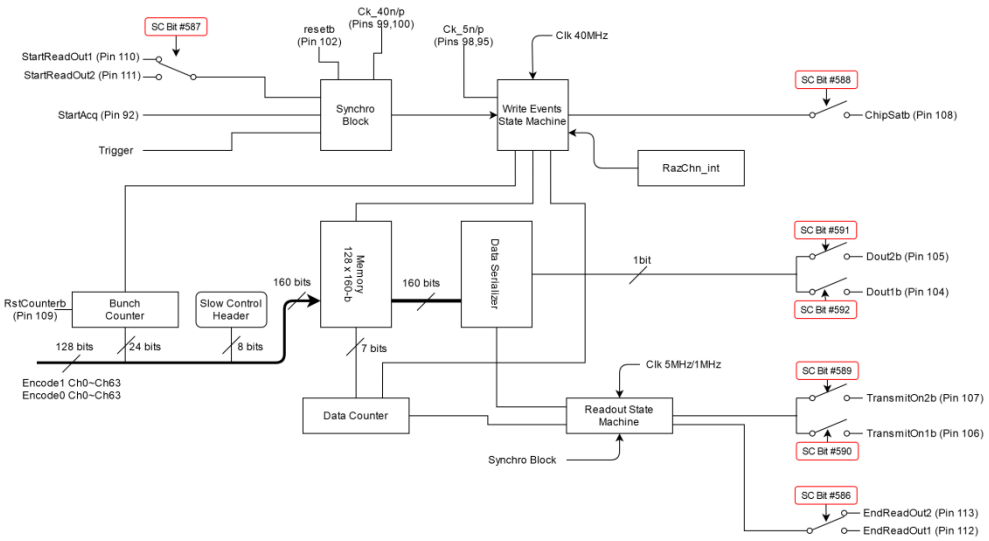


Figure 13 – Simplified schematics of GEMROC backend

ASIC data frames which are sent out serially through the data transmission pins (Pins 104-105 : Dout1b/2b) are shown in the following figure.

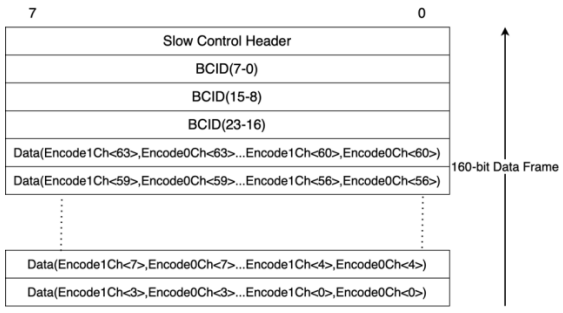


Figure 14 - GEMROC data frames

4.1.1 Digital backend connections

GEMROC data readout lines are designed to be daisy chained (Figure 15) on a printed board. The main signals for data readout are the following:

- StartAcq (pin92) : it is generated by the DAQ to start the acquisition ('1': acquisition enabled, '0': acquisition disabled)
- ChipSatb (pin 108) : this is an open collector signal generated by the chip when one of the digital memory is full (ChipSatb='0') or when the acquisition is finished
- StartReadOut1 and 2 (pins 110 and 111) : this signal is generated by the DAQ to start the Readout sequence.

There are two lines for redundancy on the printed circuit board :

- EndReadout 1 and 2 (pins 112 and 113) : this signal (duplicated for redundancy) is generated by the chip to indicate when the readout is finished
- Dout1b and 2b (pins 104 and 105) : open collector signals (duplicated for redundancy) to deliver the encoded data memorized in the digital memory
- TransmitOn1b and 2b (pins 157 and 158) : open collector signals (duplicated for redundancy) generated by the ASIC to indicate when the data out (Dout1 or 2) are transmitted to the DAQ.

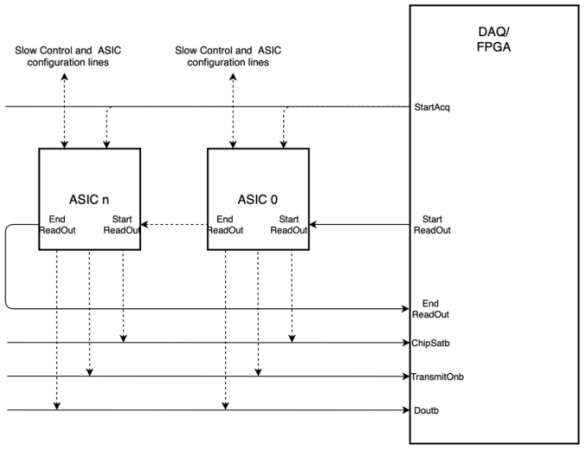


Figure 15 - GEMROC daisy chain data readout (excluding redundant lines)

The pins required for the backend connection are listed in the following table.

Pin Name	Pin Location	Type	Description
Ck_40n/p	99,100	LVDS	40MHz clock for event writing state machine
Ck_5n/p	97,98	LVDS	5MHz/1MHz clock for data transmission serializer
resetb	102	LVCMOS	Backend reset except bunch (event) counter. Active Low
RstCounterb	109	LVCMOS	Bunch (event) counter reset. Active Low
StartAcq	92	LVCMOS	Start data acquisition signal from DAQ. Active High
ChipSatb	108	Open Collector	Flag for memory full. Active Low
StartReadOut1/2	110,111	LVCMOS	Start data readout signal from DAQ. Active High
EndReadout 1/2	112,113	LVCMOS	End of data readout signal from ASIC. Active High
Dout1b/2b	104,105	Open Collector	Readout data transmission. Active Low
TransmitOn1b/2b	106,107	Open Collector	Data Transmission flag. Active Low

Table 2 - GEMROC backend connections

4.1.2 Redundancy of backend I/Os

To ensure the reliability of the lines used in the daisy chain, the Doutb, Transmitonb, StartReadOut and EndReadOut signals are send out using two separate Open Collector buffers on dedicated pins. The selection of which signal to be daisy chained is done through Slow Control parameters. The following figure illustrates the redundancy with the usage of dual buffer outputs.

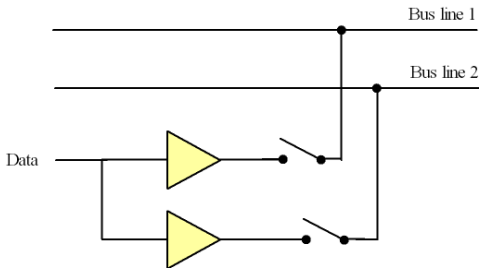


Figure 16 – Extra open collector buffer buffers for redundancy

The following Slow Control bits are used to select the redundant digital I/Os:

Slow Control bit #	Slow Control bit Name	Descriptions
586	Sel endreadout 1 or 2	Selection between EndReadout1/2 pins: '1' : EndReadout1 (Pin 112) '0' : EndReadout2 (Pin 113)
587	Sel startreadout 1 or 2	Selection between StartReadout1/2 pins: '1' : StartReadout1 (Pin 110) '0' : StartReadout2 (Pin 111)
588	EN_OC chipsatb	Enable Open Collector driver on ChipSatb (Pin 108): 1' : Enable Open Collector driver '0' : Disable Open Collector driver
589	EN_OC transmiton2b	Enable Open Collector driver on TransmitOn2b (Pin 107): 1' : Enable Open Collector driver '0' : Disable Open Collector driver
590	EN_OC transmiton1b	Enable Open Collector driver on TransmitOn1b (Pin 106): 1' : Enable Open Collector driver '0' : Disable Open Collector driver
591	EN_OC dout2b	Enable Open Collector driver on Dout2b (Pin 105): 1' : Enable Open Collector driver '0' : Disable Open Collector driver
592	EN_OC dout1b	Enable Open Collector driver on Dout1b (Pin 104): 1' : Enable Open Collector driver '0' : Disable Open Collector driver

Table 3 - Slow Control bits for GEMROC backend I/Os redundancy control

Contrary to the Open Collector I/Os which are shared bus, StartReadout1/2 and EndReadOut1/2 are point to point signals which can be daisy chained.

In the event of ASIC malfunctioning, a bypass for StartReadout1/2 or EndReadOut1/2 can be done on the printed board using external switches or resistors. The selection of the redundancy line has to be done made using the Slow Control parameters as shown in Table 3.

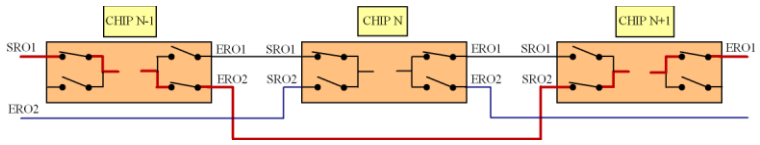


Figure 17 - StartReadout and EndReadout bypass

4.1.3 Data acquisition and readout timing diagram

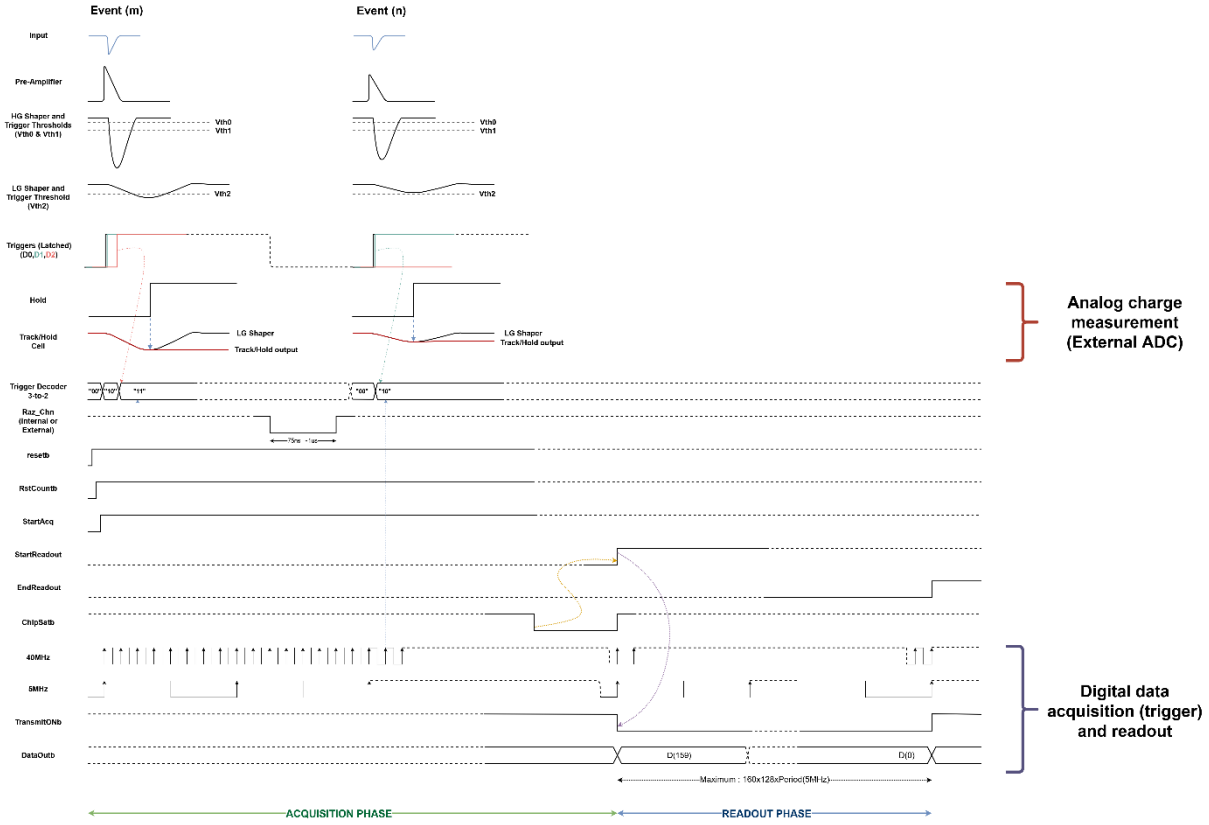


Figure 18 - GEMROC timing diagram, from data acquisition to readout phase

The timing diagram illustrated in Figure 18, is for a typical multi-event readout of a single ASIC. Encoded trigger information from the events will be stored in embedded memory of the ASIC (up to 128 events). Ideally, the data acquisition phase is performed prior the readout phase.

It should be noted that in daisy chained and shared data bus readout setup; the timing diagram would differ on the readout phase. It will depend on the time window allocated for data acquisition and also readout sequences.

5 ASIC power pulsing feature

The ASIC could be sequentially turned off in order to save power consumption using "power pulsing" feature. This ASIC is separated in several blocks and it could be powered down using dedicated pins. The current drawn by various blocks in this ASIC is reported in Table 4. Total power consumption of this ASIC is about 137mW (3.3V power supply).

Pre-amplifier	1.1mA
HG or LG shaper	1.13mA
Discriminator	0.12mA
Trigger Threshold DAC	0.52mA
Band Gap voltage reference	1.2mA
Data transmission, gates, etc..	2.4 mA
Readout block	0.4mA (0 if 40MHz clock OFF)
TOTAL	6.9 mA

Table 4 - Power consumption

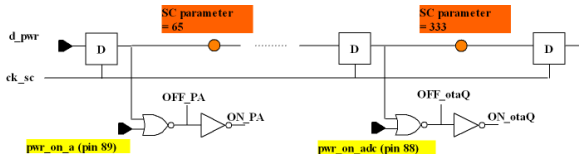


Figure 19 – Power pulsing logic

Thanks to the Slow Control parameters and dedicated ASIC input pins, users can select cells/sections to be power pulsed:

Slow Control bit #	Slow Control bit Name	Description	Power Pulsing Pin
65	on/off pa	Power pulsing stage for pre-amplifier	Pin 89 : pwr_on_a
67	on/off sh_hg	Power pulsing stage for high gain shaper (refer to Table 6)	Pin 89 : pwr_on_a
68	on/off sh_lg	Power pulsing stage for high gain shaper (refer to Table 6)	Pin 89 : pwr_on_a
71	on/off widlar	Power pulsing stage for charge measurement buffer	Pin 88 : pwr_on_adc
331	on/off dac_4bit	Power pulsing stage for 4-bit DAC HG shaper reference trimming	Pin 89 : pwr_on_a
333	on/off otaq	Power pulsing stage for analog output (Shapers and Track/Hold) buffers	Pin 88 : pwr_on_adc
334	on/off discri0	Power pulsing stage for Discriminator0 (refer to Table 7)	Pin 89 : pwr_on_a
335	on/off discri2	Power pulsing stage for Discriminator2 (refer to Table 7)	Pin 89 : pwr_on_a
336	on/off discri1	Power pulsing stage for Discriminator1 (refer to Table 7)	Pin 89 : pwr_on_a
538,539	En_pp_bandgap, On/off bg	Power pulsing stage for band gap voltage reference	Pin 87 : pwr_on_dac
540,541	En_pp_dac, On/off dac	Power pulsing stage for band gap voltage reference	Pin 87 : pwr_on_dac
580	Sc_on 5MHz and 40MHz	Power pulsing stage for LVDS receiver	Pin 90 : pwr_on_d

Table 5 - Slow Control bits with associated power pulsing input

The pins listed in 'Power Pulsing Pin' of Table 5, are used to power on or off various blocks in this ASIC when the associated Slow Control bits are set correctly. The listed blocks will be turned ON if the pins input are set high and OFF when these inputs are at low level. This is true for most blocks in the ASIC except for HG and LG shapers and the associated discriminators (Discriminator0,1 &2).

For the usage of HG and LG shapers in conjunction with power pulsing input (Pin 89 : pwr_on_a), the following Slow Control bits (SC bits #67-68) have to set accordingly :

Pin 89 : pwr_on_a	SC Bit #67	SC Bit #68	Descriptions
I/O	'0'	'0'	Power pulsing on HG shaper; LG shaper OFF
I/O	'0'	'1'	Power pulsing on HG & LG shapers
X	'1'	'0'	HG shaper ON; LG shaper OFF & power pulsing not available
X	'1'	'1'	HG & LG shapers ON; Power pulsing not available

Table 6 - Power pulsing option for HG and LG shapers

Additionally, powering ON or OFF Discriminators 0, 1 and 2 by using power pulsing input (Pin 89 : pwr_on_a) need to be done according the associated Slow Control bits (SC bits #334-336) settings as listed in the following table:

Pin 89 : pwr_on_a	SC Bit #334	SC Bit #335	SC Bit #336	Descriptions
I/O	'0'	'0'	'0'	Power pulsing on Discriminator0; Discriminator1 and 2 are OFF
I/O	'0'	'0'	'1'	Power pulsing on Discriminator0 and 1; Discriminator2 is OFF
I/O	'0'	'1'	'0'	Power pulsing on Discriminator0 and 2; Discriminator1 is OFF
I/O	'0'	'1'	'1'	Power pulsing on Discriminator0,1 and 2
X	'1'	'0'	'0'	Discriminator0 is ON; Discriminator1 and 2 are OFF & Power pulsing not available
X	'1'	'0'	'1'	Discriminator0 and 1 are ON; Discriminator2 is OFF & Power pulsing not available
X	'1'	'1'	'0'	Discriminator0 and 2 are ON; Discriminator1 is OFF & Power pulsing not available
X	'1'	'1'	'1'	Discriminator0,1 and 2 are ON; Power pulsing not available

Table 7- Power pulsing option for Discriminator 0, 1 and 2

It should be noted that HG shaper output is sent to Discriminator0 and 1, and LG shaper output is sent solely to Discriminator2. Given that the shapers can be powered on or off independently, therefore it not advisable to have a combination such as LG shaper is turned OFF and its associated discriminator, Discriminator2 turned ON through Slow Control bits or power pulsing features.

The timing of various power pulsing inputs and digital signals are shown in the following figure. It is advised to turn on the analog section first before powering on the digital part (minimum 25us later). Reset of the digital can be released in 200ns after the ASIC is powered ON and finally the data acquisition signal can start in 1us later.

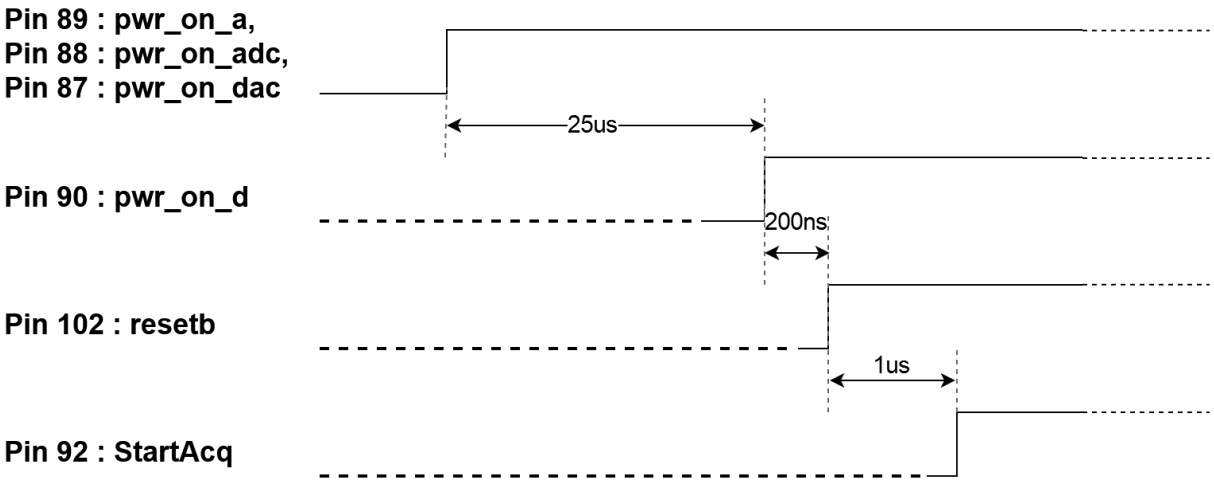


Figure 20 – Power pulsing timing

Turning down sequence with be exactly the opposite as the powering on, by starting on turning down the digital part first and next the analog part. The timing for powering down sequence is exactly similar as the powering on sequence.

6 ASIC charge injection feature

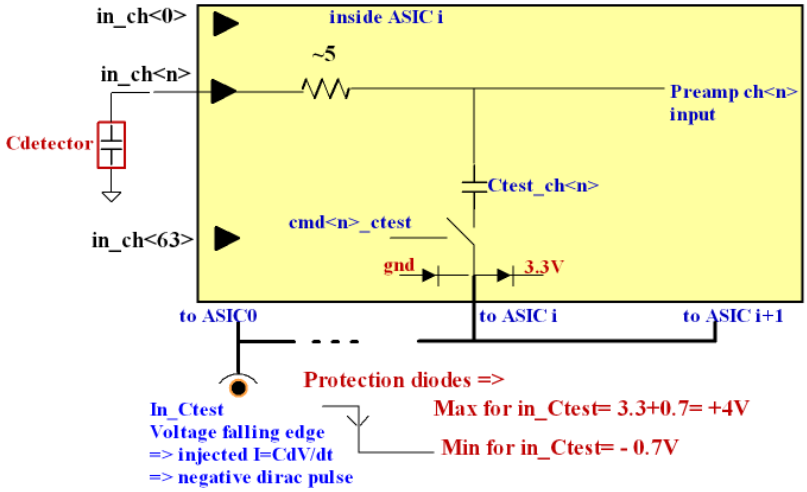


Figure 21 – Charge injection using Ctest input

Each channel can be calibrated using the charge injection input (Pin 59 : Ctest) which is common to all 64 channels. A voltage pulse (negative polarity) has to be sent on this input. There are 64 charge injection capacitors which have been designed to be equal to **500 fF** ±20%, which can be selected through the following Slow Control bits :

- Slow Control bits #1-64, ctest_ch0-63 : Charge injection for Channel 0 - 63

7 ASIC programmable parameters

7.1 Slow Control (SC) and Read registers access

There are two sets of shift register, sharing the same I/Os (selectable through Pin 114 : select), used for configuring this ASIC:

- Slow Control registers for configuring the analog components of this ASIC : 592 bits
- Read registers for reading out analog/trigger outputs (LG shaper Track/Hold cell, Discriminators 0,1 & 2) of this ASIC : 64 bits

The shared I/Os will be set according to the selection input (through Pin 114, select):

- Pin 117, sr_in : Registers input
- Pin 116, sr_ck : Registers clock
- Pin 115, sr_rstb : Registers low level reset
- Pin 115, sr_out: Register output
- Pin 114 , select : Registers I/Os selection , '1' for Slow Control registers; '0' for Read registers

The following figure illustrates the I/Os selection of each registers based in the selection input level.

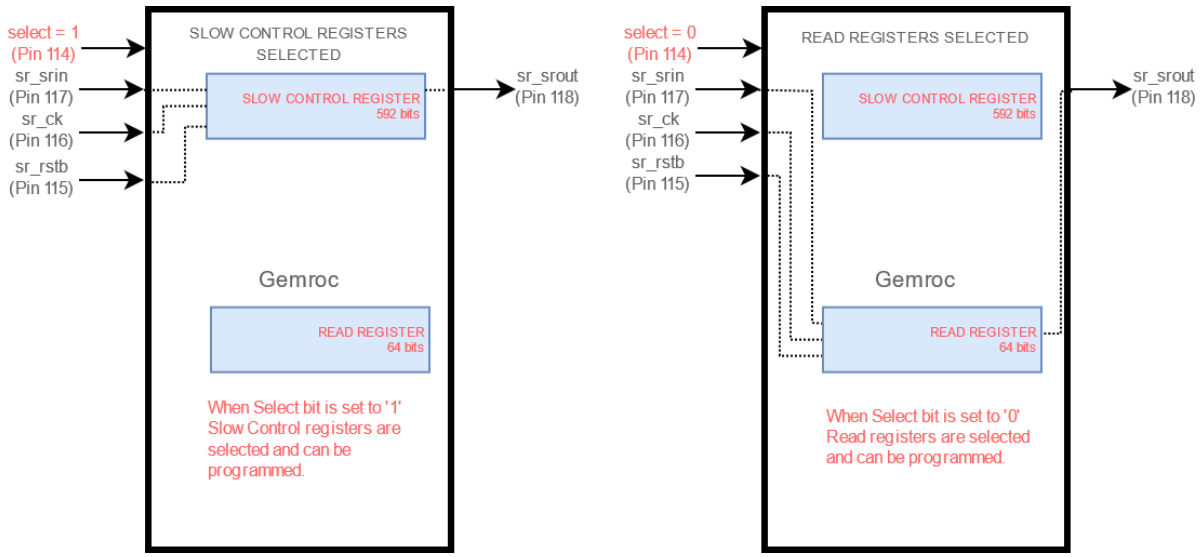


Figure 22 - Selection of Slow Control and Read registers

7.2 Slow Control register parameters

Operating the Slow Control registers is similar as shifting data in shift registers. The I/Os are described in Section 7.1, the data or parameters available are listed in Table 8 and the timing diagram is illustrated in Figure 23.

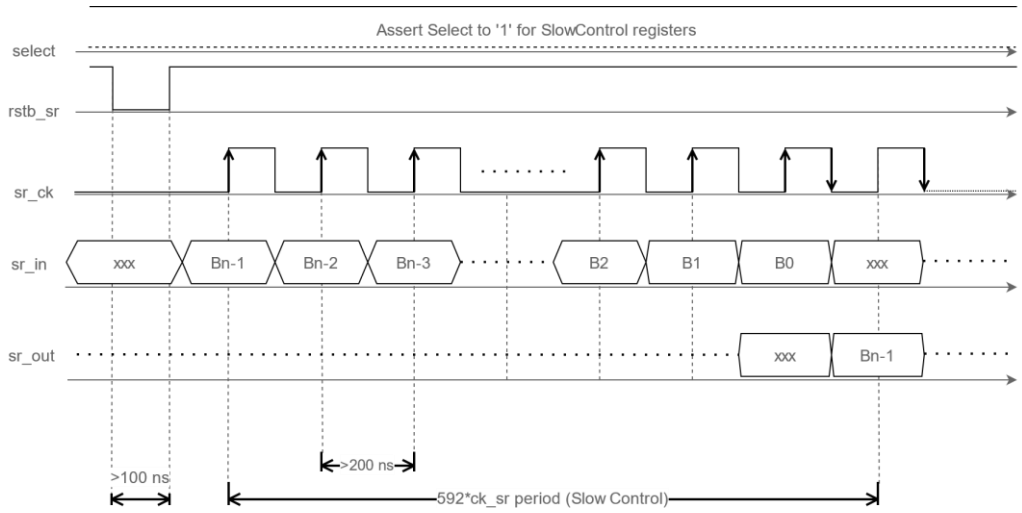


Figure 23 - GEMROC Slow Control registers timing diagram

The Slow Control parameters are listed in the following table:

CELL	BIT#	Slow Control Name	Description	DEFAULT VALUE
One_channel0	1	(Srin_sc=d_test ->) ctest_ch0 -	Charge injection for Channel 0: **'0' : Charge injection Enable** **'1' : Charge injection Disable**	off
One_channel1	2	ctest_ch1	Charge injection for Channel 1: **'0' : Charge injection Enable** **'1' : Charge injection Disable**	off
...	...			
One_channel63	64	ctest_ch63=q_test=d_pwr	Charge injection for Channel 63: **'0' : Charge injection Enable** **'1' : Charge injection Disable**	0 (off)
BIAS	65	on/off_pa for pp (+ pwr_on_a)	Power pulsing stage for pre-amp: **'0' : Power Pulsing enable** **'1'** : Power ON and Power Pulsing disable	0=OFF
	66	en_gbst (enable gain boost)	Enable pre-amp gain boost : **'0' : disable gain boost** **'1' : enable gain boost**	1=> on
	67	On/off sh_hg for power pulsing (+pwr_on_a)	Power pulsing stage for HG shaper: **'0'** : Power Pulsing enable **'1' : Power ON and Power Pulsing disable**	0 => off
	68	On/off sh_lg (depends on ON/FF sh_hg)	Power pulsing stage for HG shaper (refer to Table 6): **'0' : Power OFF/Power Pulsing disable** **'1' : Power ON /Power Pulsing enable**	0 => off
	69	sw_lg<1>	LG shaper peaking time selection: **"00" :** 30 ns **"01" : 100 ns** **"10" : 150 ns** **"11" : 200 ns**	1 => on
	70	sw_lg<0>		0 (off)
	71	On/off widlar for pp (+pwr_on_adc)	Power pulsing stage for Track/Hold output buffer: **'0' : Power Pulsing enable** **'1' : Power ON and Power Pulsing disable**	0 (off)
	72	valid_sh_hg (=q of the FF)	Selection for HG or LG shaper Read register (refer to Table 9): **'0' : LG output** **'1' : HG output**	0 (off)
		valid_sh_lg for READ register (qb of the FF)		1 (on)
	73	sw_hg<1>	HG shaper peaking time selection:	1 => on

	74	sw_hg<0> = q1_sc_bias=d_4bit_dac	**"00" : 30 ns** **"01" : 100 ns** **"10" : 150 ns** **"11" : 200 ns**	0=> off
One_channel0 4 bits dac	75	B0	Bit<0> of 4-bit DAC HG shaper reference for Channel 0 : **'0' :** Inactive **'1' : Active**	0 (off)
One_channel0	76	B1	Bit<1> of 4-bit DAC HG shaper reference for Channel 0 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel0	77	B2	Bit<2> of 4-bit DAC HG shaper reference for Channel 0 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel0	78	B3	Bit<3> of 4-bit DAC HG shaper reference for Channel 0 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel1 4 bits dac	79	B0	Bit<0> of 4-bit DAC HG shaper reference for Channel 1 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel1	80	B1	Bit<1> of 4-bit DAC HG shaper reference for Channel 1 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel1	81	B2	Bit<2> of 4-bit DAC HG shaper reference for Channel 1 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel1	82	B3	Bit<3> of 4-bit DAC HG shaper reference for Channel 1 : **'0' : Inactive** **'1' : Active**	0 (off)
…				
One_channel63 4bits dac	327	B0	Bit<0> of 4-bit DAC HG shaper reference for Channel 63 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel63	328	B1	Bit<1> of 4-bit DAC HG shaper reference for Channel 63 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel63	329	B2	Bit<2> of 4-bit DAC HG shaper reference for Channel 63 : **'0' : Inactive** **'1' : Active**	0 (off)
One_channel63	330	B3 = q_4bit_dac=d_pwr_4bitdac	Bit<3> of 4-bit DAC HG shaper reference for Channel 63 : **'0' : Inactive** **'1' : Active**	0 (off)
BIAS	331	On/off dac_4bit for pp (+pwr_on_a)	Power pulsing stage for 4-bit DAC HG shaper reference trimming: **'0' : Power Pulsing enable** **'1' : Power ON and Power Pulsing disable**	0 (off)
	332	en_otaq	Enable output and Power ON for Shapers analog buffer: **'0' : Output Disable and Power OFF** **'1' : Output Enable and Power ON(Power Pulsing)**	0 (off)
	333	On/off otaQ for pp (+pwr_on_adc)	Power pulsing stage for analog output (Shapers and Track/Hold) buffers: **'0' : Power Pulsing enable** **'1' : Power ON and Power Pulsing disable**	0 (off)
	334	on/off discri0 for pp (+pwr_on_a)	Power pulsing stage for Discriminator0 (refer to Table 7): **'0' : Power Pulsing enable** **'1' : Power ON and Power Pulsing** disable	0 (off)
	335	on/offdiscri2 depends on discri0	Power pulsing stage for Discriminator2 (refer to Table 7): **'0' : Power OFF/Power Pulsing disable** **'1' : Power ON /Power Pulsing enable**	0 (off)
	336	on/off discri1 depends on discri0	Power pulsing stage for Discriminator1 (refer to Table 7): **'0' : Power OFF/Power Pulsing disable** **'1' : Power ON /Power Pulsing enable**	0 (off)
	337	q2_sc_bias=d_mask=rs_or_discri	Discriminators latch: **0' : Latch disable** **'1' : Latch enable**	1
One_channel0	338	Mask discri0 ch0	Discriminator0 of Channel 0 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel0	339	Mask discr1 ch0	Discriminator1 of Channel 0 mask: **0' : Mask enable**	1 (no mask)

			'1' : Mask disable	
One_channel0	340	Mask discri2=qmask ch0	Discriminator2 of Channel 0 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel1	341	mask0 ch1	Discriminator0 of Channel 1 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel1	342	mask1 ch1	Discriminator1 of Channel 1 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel1	343	mask2=qmask ch1	Discriminator2 of Channel 1 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
…	…	…		
One_channel63	527	mask0 ch63	Discriminator0 of Channel 63 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel63	528	mask1 ch63	Discriminator1 of Channel 63 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
One_channel63	529	mask2 ch63=qmask	Discriminator2 of Channel 63 mask: **0' : Mask enable** **'1' : Mask disable**	1 (no mask)
TOP LEVEL	530	header<0>	Slow Control header<0> for data readout	1
	531	header<1>	Slow Control header<1> for data readout	1
	532	header<2>	Slow Control header<2> for data readout	1
	533	header<3>	Slow Control header<3> for data readout	1
	534	header<4>	Slow Control header<4> for data readout	1
	535	header<5>	Slow Control header<5> for data readout	1
	536	header<6>	Slow Control header<6> for data readout	1
	537	header<7> = srin_triple dac	Slow Control header<7> for data readout	1
Triple DAC :	538	En_pp_bandgap	Power ON or OFF bandgap : **'0' : BandGap OFF** **'1' : Bandgap ON (Power Pulsing)**	1
Bias DAC	539	On/off bg	Power pulsing bandgap : **'0' : Power pulsing enable** **'1' : Power pulsing disable**	0
	540	En_pp_dac	Power ON or OFF trigger threshold DAC : **'0' : DAC OFF** **'1' : DAC ON (Power Pulsing)**	1
	541	On/off dac	Power pulsing trigger threshold DAC : **'0' : Power pulsing enable** **'1' : Power pulsing disable**	0
DAC0 (for Vth0)	542	Bb0<0> ! MSB and low active !	Bit<9> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1 (off)
	543	Bb0<1>	Bit<8> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1 (off)
	544	Bb0<2>	Bit<7> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	545	Bb0<3>	Bit<6> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	546	Bb0<4>	Bit<5> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	547	Bb0<5>	Bit<4> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	548	Bb0<6>	Bit<3> of 10-bit DAC Discriminator0 threshold : **'0' : Active**	1

			'1' : Inactive	
	549	Bb0<7>	Bit<2> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	550	Bb0<8>	Bit<1> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1
	551	Bb0<9>	Bit<0> of 10-bit DAC Discriminator0 threshold : **'0' : Active** **'1' : Inactive**	1 (off)
DAC1 (for Vth1)	552	Bb1<0>	Bit<9> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	553	Bb1<1>	Bit<8> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	554	Bb1<2>	Bit<7> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	555	Bb1<3>	Bit<6> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' :** Inactive	1
	556	Bb1<4>	Bit<5> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	557	Bb1<5>	Bit<4> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	558	Bb1<6>	Bit<3> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	559	Bb1<7>	Bit<2> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	560	Bb1<8>	Bit<1> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1
	561	Bb1<9>	Bit<0> of 10-bit DAC Discriminator1 threshold : **'0' : Active** **'1' : Inactive**	1 (off)
DAC2 (for Vth2)	562	Bb2<0>	Bit<9> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	563	Bb2<1>	Bit<8> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' :** Inactive	1
	564	Bb2<2>	Bit<7> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	565	Bb2<3>	Bit<6> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	566	Bb2<4>	Bit<5> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	567	Bb2<5>	Bit<4> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	568	Bb2<6>	Bit<3> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	569	Bb2<7>	Bit<2> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	570	Bb2<8>	Bit<1> of 10-bit DAC Discriminator2 threshold : **'0' : Active** **'1' : Inactive**	1
	571	Bb2<9> =q_dac	Bit<0> of 10-bit DAC Discriminator2 threshold : **'0' : Active**	1 (off)

			'1' : Inactive	
Trigger cell	572	trig2b (nor64_2)	Trigger2 NOR enable to digital block: **'0' : disable trigger** **'1' : enable trigger**	1 (=valid ON)
	573	trig1b (nor64_1)	Trigger1 NOR enable to digital block: **'0' : disable trigger** **'1' : enable trigger**	1 (=valid ON)
	574	trig0b (nor64_0)	Trigger0 NOR enable to digital block: **'0' : disable trigger** **'1' : enable trigger**	1 (=valid ON)
	575	EN_trig_out	Trigger Open Collector outputs enable: **'0' : disable all outputs** **'1' : enable all outputs**	1 (=valid ON)
	576	disc_or_or	Trigger Open Collector outputs selection: **'0' : trigger multiplexers readout (refer to Section** 7.3 and Table 9) **'1' :** Triggers OR	1 (=or)
	577	trig_ext validation	Internal or external triggers to digital block: **'0' : external triggers** **'1' : internal triggers**	1
	578	raz_chn_int validation	Internal **"raz_chn" enable to analog block:** **'0' : disable** **'1' : enable**	1
	579	raz_chn_ext validation=qt_sc	**External "raz_chn" enable to analog block:** **'0' : disable** **'1' : enable**	0
TOP LEVEL	580	Sc_on 5MHz and 40MHz (+lvds_on5 and lvds_on40)	Power pulsing stage for LVDS receiver : **'0' : Power pulsing** **'1' :** Power ON, Power pulsing disabled	0 (off)
	581	Ck_mux: choice between sroand sro_pod, ck5 and ck5_pod, ck40 and ck40_pod	Start ReadOut, Clocks to digital selection : **'0' : Input through Power On Digital*** module **'1' : Direct input**	1=> sro,ck5,ck40 validated (pod bypassed)
	582	Sel_raz1 (raz_chn width)	**Internal "raz_chn" width :** **"00" : 75ns** **"01" : 250ns** **"10" : 500ns** **"11" : 1us**	1 (on)
	583	Sel_raz0 (mux raz_chn width)		1 (on)
	584	NC		1
	585	NC		1
	586	Sel endreadout 1 or 2	Selection for EndReadOut : **'0' :** EndReadOut2 **'1' : EndReadOut1**	1 (endreadout1)
	587	Sel startreadout 1 or 2	Selection for StartReadOut : **'0' : StartReadOut2** **'1' : StartReadOut1**	1 (startreadout1)
	588	EN_OC chipsatb	Selection for ChipSat Open Collector output buffer : **'0' : Disable output buffer** **'1' : Enable output buffer**	1
	589	EN_OC transmiton2b	Selection for TransmitOn2b Open Collector output buffer : **'0' : Disable output buffer** **'1' : Enable output buffer**	1
	590	EN_OC transmiton1b	Selection for TransmitOn1b Open Collector output buffer : **'0' : Disable output buffer** **'1' : Enable output buffer**	1
	591	EN_OC dout2b	Selection for Dout2b Open Collector output buffer : **'0' : Disable output buffer** **'1' : Enable** output buffer	1
	592	EN_OC dout1b	Selection for Dout1b Open Collector output buffer : **'0' : Disable output buffer** **'1' : Enable output buffer** *Last register of Slow Control clocked with falling edge of sr_ck, refer to timing diagram Figure 23	1
	592b	*Q_sc = Srout_sc (d clocked on ckb)*		1

Table 8 – Slow Control register parameters

*Power on digital module will manage the clocks (5MHz and 40MHz) received by the ASIC by turning of the LVDS receivers until "power_on_d" input is received (refer to section 0) and data acquisition is initiated (refer to section 4).

7.3 Read register

As the Read registers share the same I/Os and operation as the Slow Control registers, users will need to shift in data into shift registers as well. The I/Os are described in Section 7.1, sub-address available are listed in Table 9 and the timing diagram is illustrated in Figure 24.

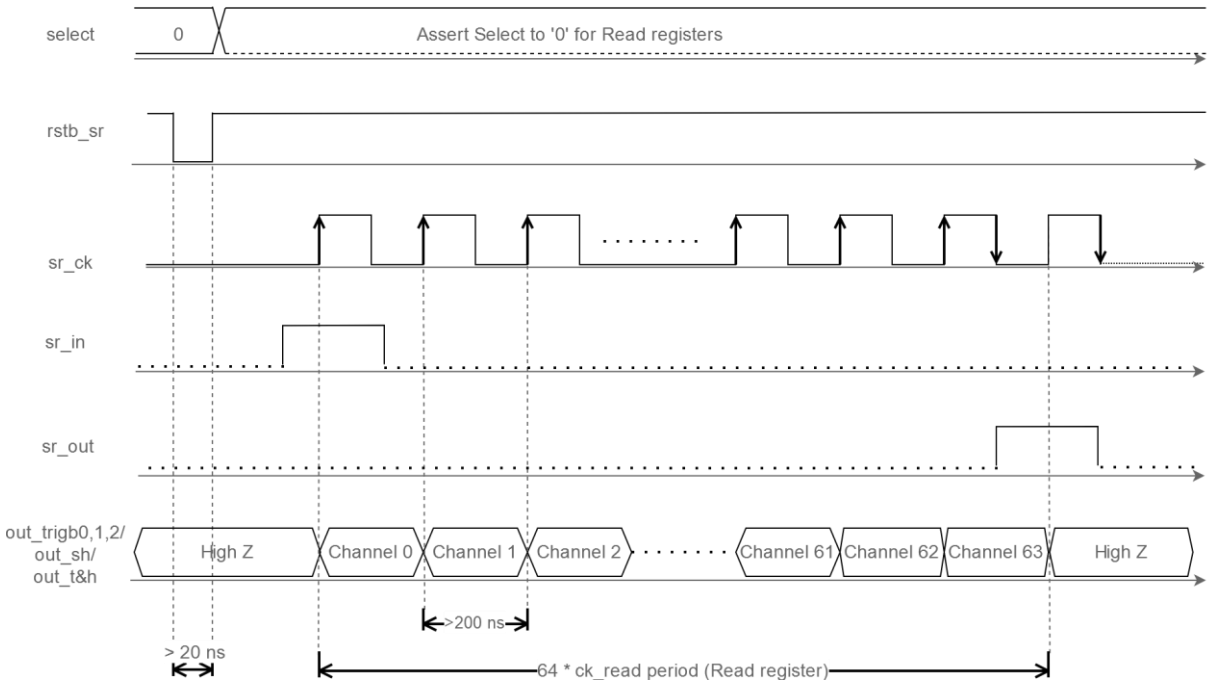


Figure 24 - GEMROC Read registers timing diagram

Pin Name	Pin	Comment	Output type	Sub address
out_trig0b	85	Output trigger 0 (HG Shaper, threshold:Vth0)	Trigger	0-63
out_trig1b	84	Output trigger 1 (HG Shaper, threshold:Vth1)	Trigger	0-63
out_trig2b	83	Output trigger 2 (LG Shaper, threshold:Vth2)	Trigger	0-63
out_sh	128	Output for LG or HG shaper (refer to SC Bits #72)	Analog	0-63
out_t&h	129	Output for LG shaper Track and Hold cell	Analog	0-63

Table 9 - Read registers and association output

8 ASIC Performances

8.1 DAC linearity

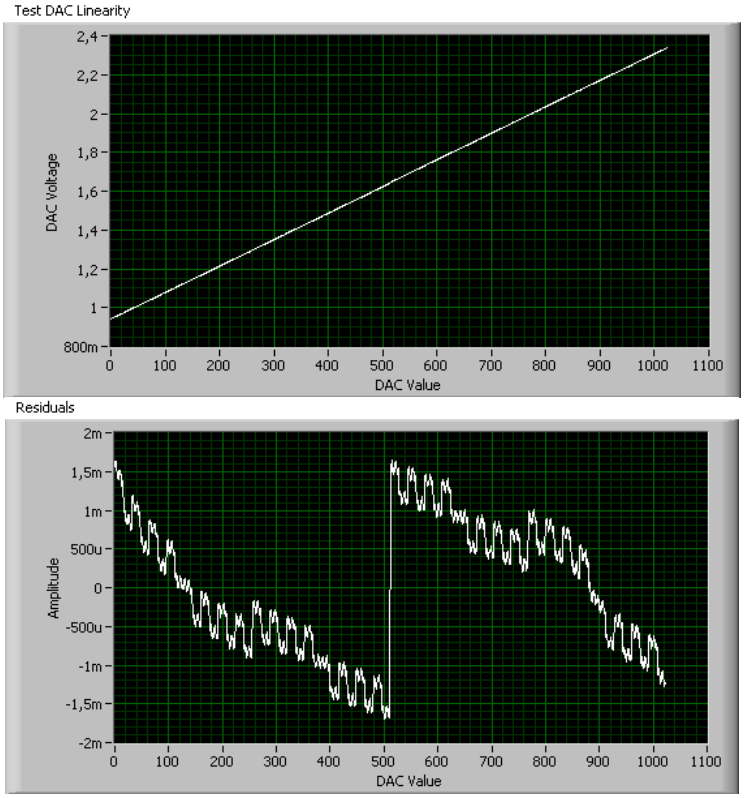


Figure 25 – 10-bit DAC linearity

The measurement done in this section is for 10-bit DAC used for setting the trigger threshold. The performances of these DACs as the following:

- Range : 0.95V - 2.35V
- LSB: 1.37mV/DACU

8.2 DC Measurements

In this section, the DC measurements were mostly done for HG and LG shapers.

8.2.1 DC Uniformity of the HG Shaper

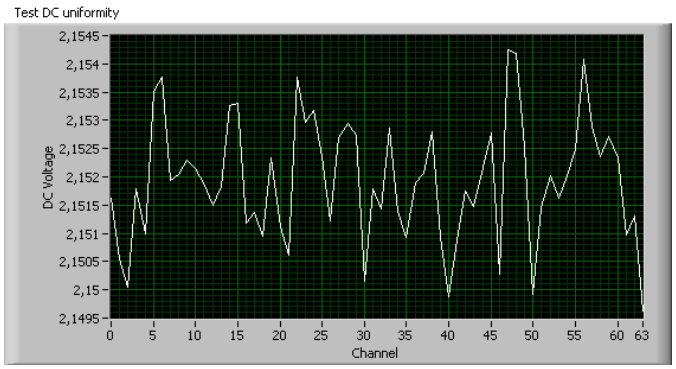


Figure 26 - HG shaper DC measurement without reference voltage trimming

The DC measurements were performed for 64 channels of HG shapers (without reference voltage trimming, Figure 26) and the results are listed in the following:

- Average : 2.15194V
- Min value : 2.14963V
- Max value : 2.15424V
- Standard deviation : 1.088mV

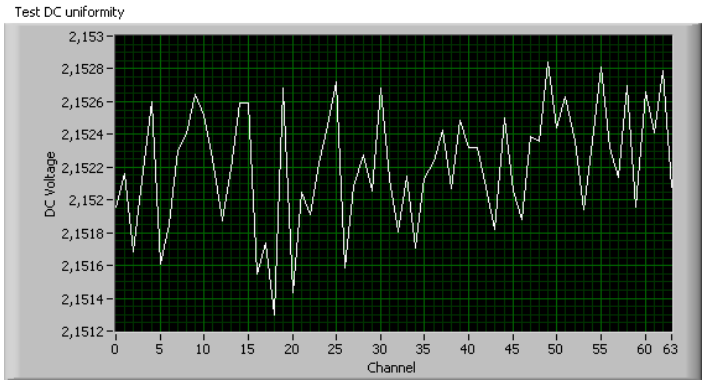


Figure 27 - HG shaper DC measurement after correction

The offset presents between all channels, can be corrected using the 4-bit DAC available for trimming the HG shaper reference voltage. The results of the DC measurement (Figure 27) after HG shaper reference voltage trimming are listed in the following :

- Average : 2.15221V
- Min value : 2.1513V
- Max value : 2.15284V
- Standard deviation : 360.71µV

8.2.2 DC Uniformity of the LG Shaper

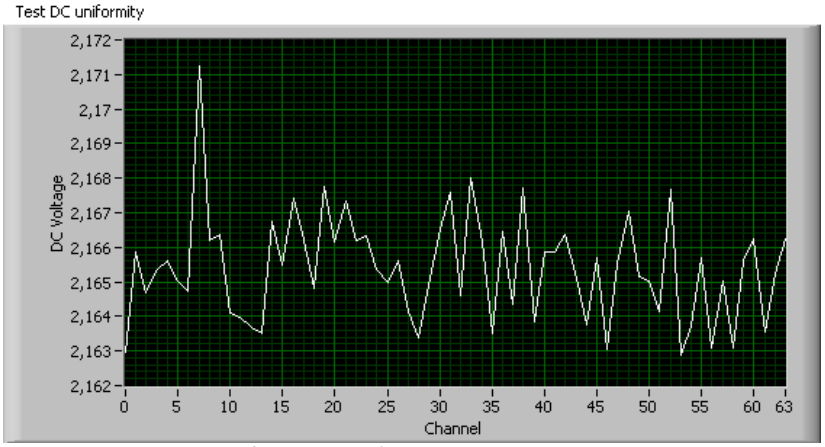


Figure 28 - LG shaper DC measurement

Similar DC measurements were performed for 64 channels of LG shapers and the results are listed as the following :

- Average : 2.1654 V
- Min value : 2.16289V
- Max value : 2.17125V
- Standard deviation : 1,54015mV

9 Amplitude and transient measurements

The transient and amplitude measurements were performed for HG shaper and for various detector capacitances (20pF and 88 pF). For each detector capacitance, the 10fC and 100fC of equivalent charges were injected. The results are reported in Table 10 and Table 11.

HG shaper with detector capacitance = 20pF

Shaping time Selection (SC bits #73-74)	Input Charge = 10 fC		Input Charge = 100 fC		Measure noise (RMS)
	Measured Amplitude	Measured Peaking time	Measured Amplitude	Measured Peaking time	
"00" : 30 ns	-72 mV	65 ns	-771 mV	60 ns	1.58 mV
"01" : 100 ns	-93 mV	103 ns	-971 mV	103 ns	1.6 mV
"10" : 150 ns	-100 mV	152 ns	-1.041 V	152 ns	1.61 mV
"11" : 200 ns	-103 mV	202 ns	1.07V	202 ns	1.61 mV

Table 10 - HG shaper amplitude and peaking time measurements for 20pF detector capacitance.

HG shaper with detector capacitance = 88 pF

Shaping time Selection (SC bits #73-74)	Input Charge = 10 fC		Input Charge = 100 fC		Measure noise (RMS)
	Measured Amplitude	Measured Peaking time	Measured Amplitude	Measured Peaking time	
"00" : 30 ns	-67 mV	79 ns	-700 mV	72 ns	3.3 mV
"01" : 100 ns	-94 mV	121 ns	-970 mV	121 ns	136 mV
"10" : 150 ns	-101 mV	168 ns	-1.05 V	168 ns	3.55 mV
"11" : 200 ns	-105 mV	215 ns	1.09V	215 ns	3.46 mV

Table 11 - HG shaper amplitude and peaking time measurements for 88pF detector capacitance.

10 S-curves of HG shaper

S-curve is a trigger characterization measurement where the response of trigger is quantified based on the various threshold level applied. Therefore, the probability of having a trigger output (denoted as Trigger Efficiency) can be plotted versus the threshold sweep for a given discriminator. This measurement has been performed with and without charge injection. Without charge injection, the baseline threshold for 64-channel can be extracted in order to verify the non-uniformity on all channels. Additionally, noise envelope and equivalent output noise can be also extracted for each channel.

With charge injection, two information can be extracted: minimum input charge of the ASIC and also the linearity of HG shaper against various input charge.

10.1 Baseline S-curve without and with HG reference trimming

In order to take into account noise contribution of a detector, 20pF capacitors are included at the input. S-curve measurement has been performed without charge injection. The baseline S-curve for all channels without and with the HG reference voltage trimming is illustrated in Figure 29 and Figure 30 respectively.

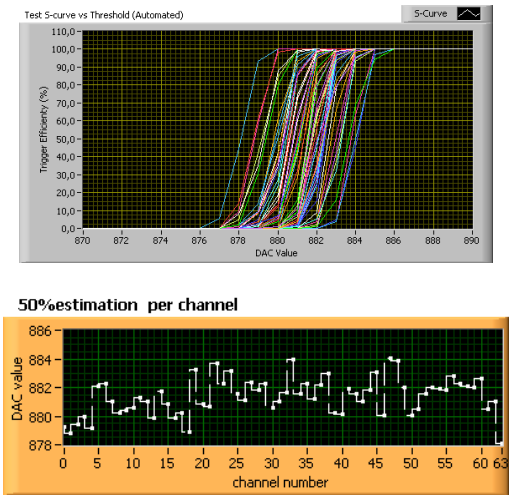


Figure 29 - HG shaper S-Curve measurement without HG shaper reference voltage trimming

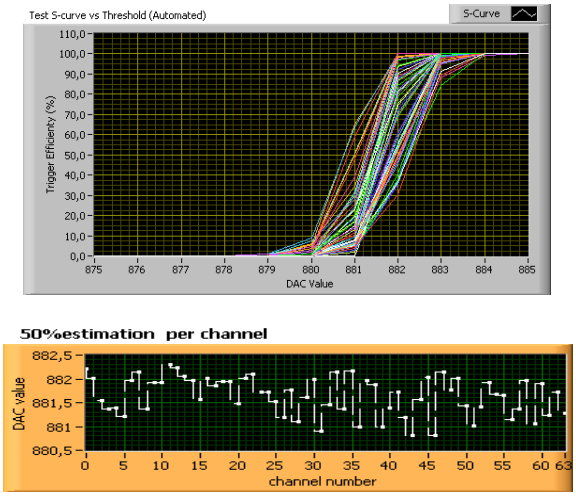


Figure 30 - HG shaper S-Curve measurement without HG shaper reference voltage trimming

The threshold baseline for all 64-channel were taken at midpoint (50%) transition of the trigger efficiency, from 0 to 100% and the results are plotted in Figure 31 and listed in Table 12.

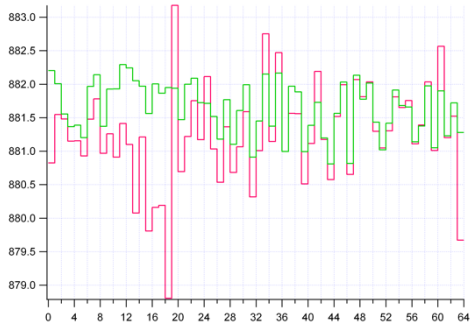


Figure 31 - HG shaper threshold baseline from S-curve before and after correction

	Baseline threshold without HG shaper reference voltage trimming	Baseline threshold with HG shaper reference voltage trimming
Average DAC value	881.242	881.644
Standard Deviation	0.735	0.397

Table 12 - S-curve threshold baseline with and without HG shaper reference voltage trimming

10.2 Charge injection with 20 pF detector capacitance

HG shaper configuration is set to 150 ns of peaking time (SC bits #73-74 = "10") and detector capacitance of 20 pF were added to the input. The HG reference voltage trimming has been applied and various charge injection starting from 1fC used. The S-curve for 1fC charge injection is illustrated in Figure 32.

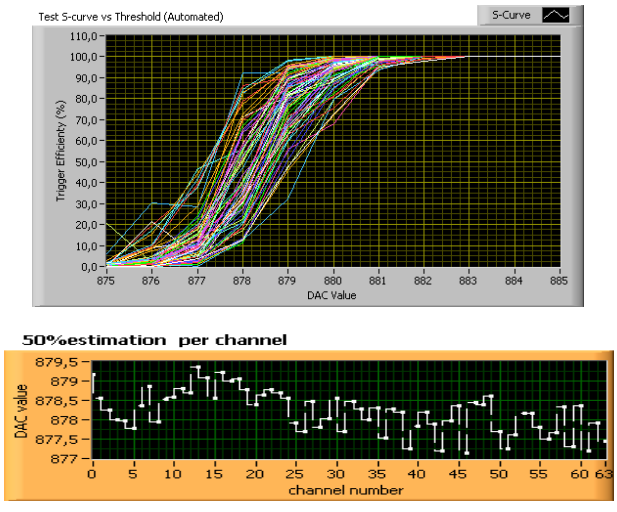


Figure 32 - HG shaper S-Curve for 1fC charge injection

The midpoint transitions (50%) of trigger efficiency for all channels and for baseline, 1fC and 2fC inputs are illustrated in Figure 33.

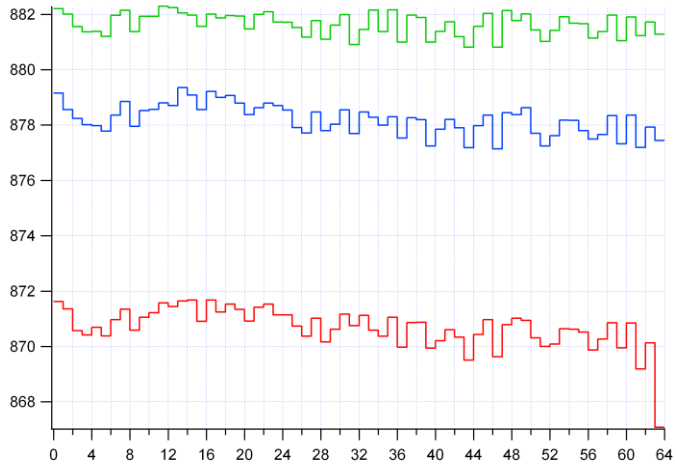


Figure 33 - HG shaper 50% triggering efficiency point from S-Curves for baseline (green), 1fC (blue) and 2fC (red)

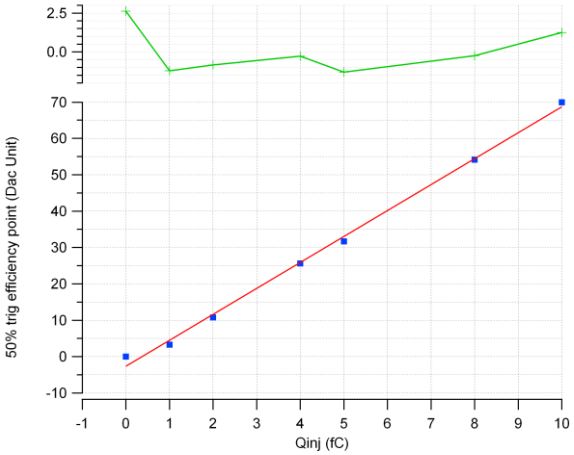


Figure 34 - HG shaper 50% triggering efficiency point vs input charges

The midpoint trigger efficiency transition for one channel versus input charges up to 10fC is plotted in Figure 34. This plot gives the information of threshold variation linearity which is about 7.13 DAC Unit/fC. The minimum detectable signal in this configuration is about 1fC which is around five times higher than the level of the equivalent output noise ~0.2fC.

10.3 Charge injection with 88 pF detector capacitance

Similar measurements were performed with 88 pF of detector capacitance, HG shaper was under identical peaking time configuration and voltage trimming applied. Midpoint triggering efficiency for all channels versus various input charges are illustrated in Figure 35.

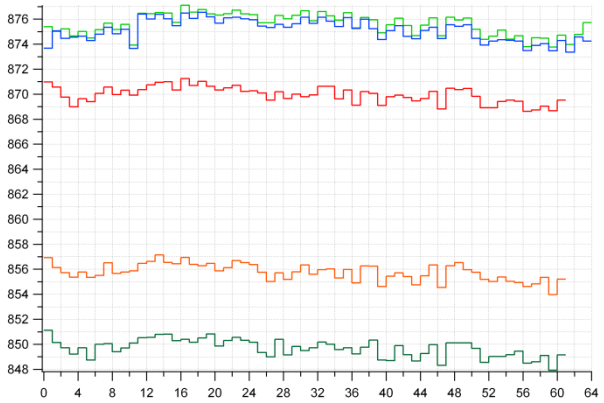


Figure 35 - HG shaper 50% triggering efficiency for 88pF equivalent detector capacitance and various injected charge (baseline (light green), 1fC (blue), 2fC(red), 4fC(orange) and 5fC(dark green))

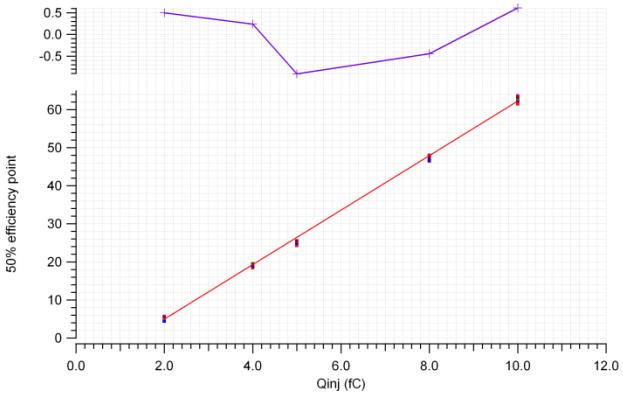


Figure 36 – HG shaper 50% triggering efficiency for 88pF equivalent detector capacitance vs injected charge

Figure 36 shows the midpoint (50%) trigger efficiency transition for one channel versus input charges up to 10fC. The extracted threshold variation linearity is around 7.15 DAC Unit/fC. The minimum detectable signal is around 2fC which translated in signal-to-noise ratio of about five times higher than the level of the equivalent output noise ~0.4fC.

11 Pinout & mechanics

GEMROC1 is available in LQFP 160 package.

11.1 Pin type description

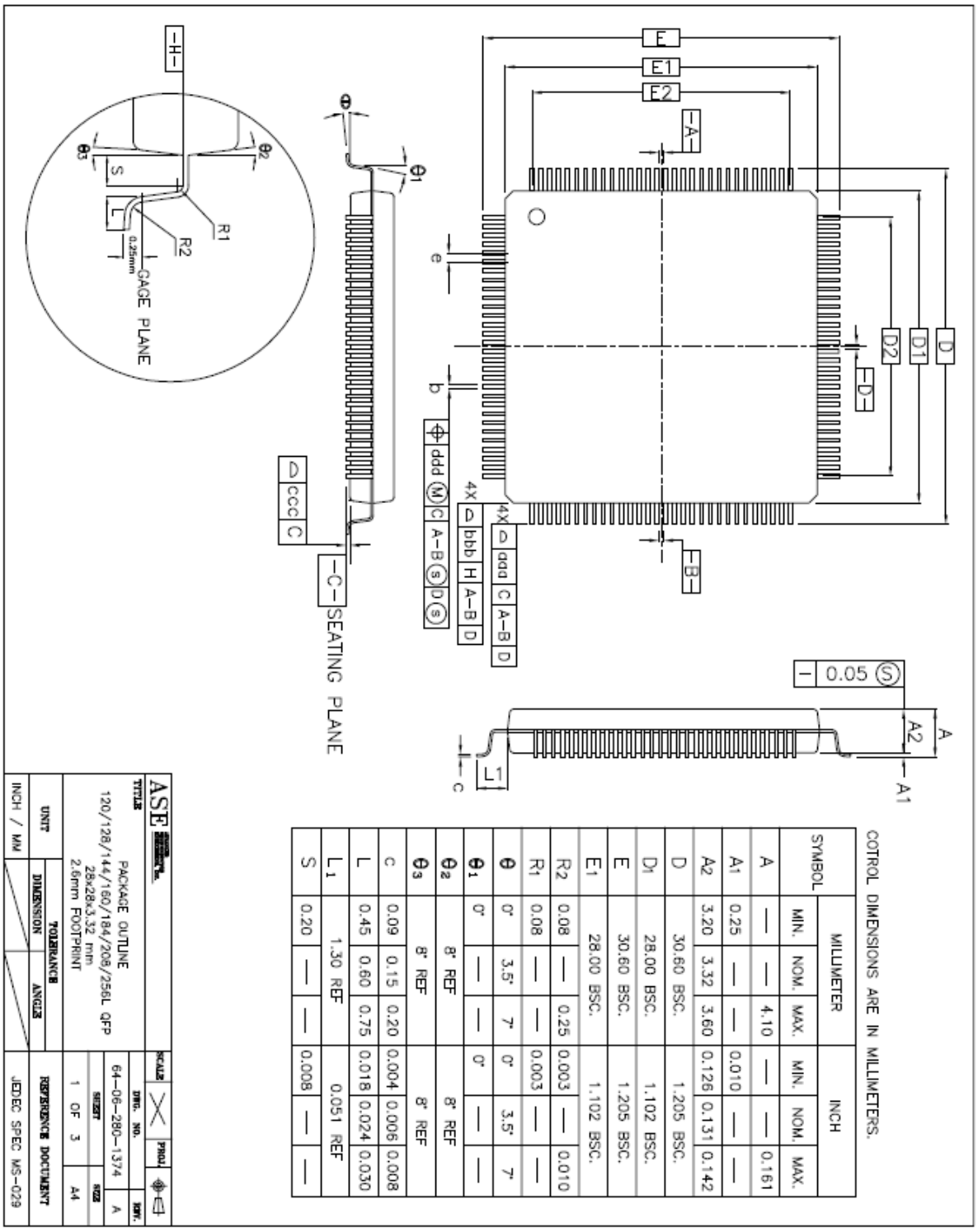
Pin type	Description	Connection
Power	Power or Ground Pin	Decoupling capacitors advised to be added
Analog input	Analog signal input	Detector connection
Analog output	Analog signal output	External buffering required if cable driving
Analog bias	Analog bias connection. Bias is internal and can be tuned externally through these pins	N/A unless specified
Digital input	Digital input connection	LVCMOS (3.3V) level
Digital output	Digital output connection	LVCMOS (3.3V) level
Digital output OC	Open Collector digital output connection	External pull-up resistor required
Digital input LVDS	LVDS receiver	LVDS load resistor required to be close to ASIC

Table 13 – Pin type description

11.2 LQFP 160 packaging

11.2.1 Package layout & mechanics

ASE ADVANCED SEMICONDUCTOR ENGINEERING,INC



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	4.10	—	—	0.161
A_1	0.25	—	—	0.010	—	—
A_2	3.20	3.32	3.60	0.126	0.131	0.142
D	30.60 BSC.			1.205 BSC.		
D_1	28.00 BSC.			1.102 BSC.		
E	30.60 BSC.			1.205 BSC.		
E_1	28.00 BSC.			1.102 BSC.		
R_2	0.08	—	0.25	0.003	—	0.010
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	8° REF			8° REF		
θ_3	8° REF			8° REF		
c	0.09	0.15	0.20	0.004	0.006	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.30 REF			0.051 REF		
S	0.20	—	—	0.008	—	—

ASE ADVANCED SEMICONDUCTOR ENGINEERING,INC.

TITLE: PACKAGE OUTLINE 120/128/144/160/184/208/256L QFP 28x28x3.32 mm 2.6mm FOOTPRINT

SCALE: X | PROJ.

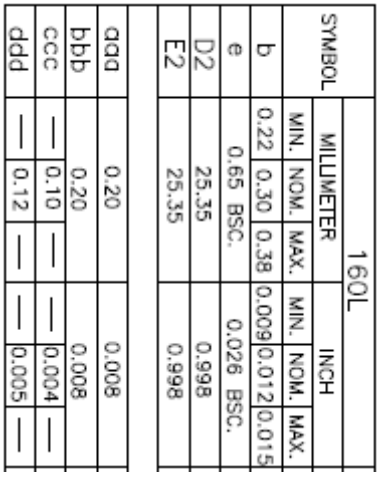
DWG. NO. 64-06-280-1374 | REV. A

SHEET 1 OF 3 | SIZE A4

UNIT: INCH / MM

TOLERANCE: DIMENSION / ANGLES

REFERENCE DOCUMENT: JEDEC SPEC MS-029



SYMBOL	MILLIMETER			INCH			160L
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
b	0.22	0.30	0.38	0.009	0.012	0.015	
e		0.65 BSC.			0.026 BSC.		
D2	25.35			0.998			
E2	25.35			0.998			
aaa		0.20			0.008		
bbb		0.20			0.008		
ccc	—	0.10	—	—	0.004	—	
ddd	—	0.12	—	—	0.005	—	

Figure 37 - GEMROC1 LQFP160 mechanics

11.2.2 Pin list

Pin #	Pin name	Pin type	Description	Connection
1	vssi	Power	Inputs Bulk	to GND
2	vdd_pad	Power	Inputs Pads Protection	
3	in<14>	Analog Input		
4	in<15>	Analog Input		
5	in<16>	Analog Input		
6	in<17>	Analog Input		
7	in<18>	Analog Input		
8	in<19>	Analog Input		
9	in<20>	Analog Input		
10	in<21>	Analog Input		
11	in<22>	Analog Input		
12	in<23>	Analog Input		
13	in<24>	Analog Input		
14	in<25>	Analog Input		
15	in<26>	Analog Input		
16	in<27>	Analog Input		
17	in<28>	Analog Input		
18	in<29>	Analog Input		
19	in<30>	Analog Input		
20	in<31>	Analog Input		
21	gnd_pa	Power	Analog (PreAmp) Ground	to GND
22	in<32>	Analog Input		
23	in<33>	Analog Input		
24	in<34>	Analog Input		
25	in<35>	Analog Input		
26	in<36>	Analog Input		
27	in<37>	Analog Input		
28	in<38>	Analog Input		
29	in<39>	Analog Input		
30	in<40>	Analog Input		

31	in<41>	Analog Input		
32	in<42>	Analog Input		
33	in<43>	Analog Input		
34	in<44>	Analog Input		
35	in<45>	Analog Input		
36	in<46>	Analog Input		
37	in<47>	Analog Input		
38	in<48>	Analog Input		
39	in<49>	Analog Input		
40	vdd_pad	Power	Inputs Pads Protection	
41	vssi	Power	Inputs Bulk	to GND
42	gnd_pa	Power	Analog (PreAmp) Ground	to GND
43	in<50>	Analog Input		
44	in<51>	Analog Input		
45	in<52>	Analog Input		
46	in<53>	Analog Input		
47	in<54>	Analog Input		
48	in<55>	Analog Input		
49	in<56>	Analog Input		
50	in<57>	Analog Input		
51	in<58>	Analog Input		
52	in<59>	Analog Input		
53	in<60>	Analog Input		
54	in<61>	Analog Input		
55	in<62>	Analog Input		
56	in<63>	Analog Input		
57	gnd_pa	Power	Analog (PreAmp) Ground	to GND
58	vssi	Power	Analog part Bulk	to GND
59	ctest	Analog Input	Calibration input	
60	vdd_pa	Power	Analog (PreAmp) Power Supply	to 3.3V
61	vref_pa	Analog ref	Pre Amps bias voltage	40k, 10k to v_bg
62	vref_sh	Analog ref	Pre Amps bias voltage	2.2k, 300 to v_bg
63	NC			
64	vssa	Power	Analog part Bulk	to GND
65	Ib_4bit_dac	Analog Bias	4 bit dac bias	400k to gnd
66	gnd_dac	Power	Analog Ground	to GND
67	vdd_dac	Power	Analog Power Supply	to 3.3V
68	vdd_bg	Power	Analog bandgap Power Supply	to 3.3V
69	gnd_bg	Power	Analog (BandGap) Ground	to GND
70	v_bg	Analog Output	BandGap output	
71	vref_dac	Analog Bias	10-bit triple DAC OTAs Input stage bias	200k,400k to v_bg
72	ibo_dac	Analog Bias	Bias dac	100k to vdd_dac
73	Iref_dac	Analog Bias	10-bit triple DAC bias current	150k (vbg), 250k vrefdac External 200k to add in // with 150k => vref_dac=940mV
74	vssa	Power	Analog part Bulk	to GND
75	vssm	Power	Mixed part Bulk	to GND
76	vdd_discri	Power	Mixed (Discriminator) Power Supply	to 3.3V
77	vth2	Analog Output	10-bit dual DAC output 2	
78	vth1	Analog Output	10-bit dual DAC output 1	
79	vth0	Analog Output	10-bit dual DAC output 0	
80	vddd2	Power	Digital (Digital ASIC) Power Supply	to 3.3V

81	**vssd**	Power	Digital part Bulk	**to GND**
82	**vddd**	Power	Digital (LVDS receivers & digital glue) Power Supply	**to 3.3V**
83	**out_trig2b**	Digital Output	**Open collector signal (internal 30k)**	
84	**out_trig1b**	Digital Output	**Open collector signal (internal 30k)**	
85	**out_trig0b**	Digital Output	**Open collector signal (internal 30k)**	
86	trig_ext	Digital Input	External Trigger signal	Active ↑
87	pwr_on_dac	Digital Input	DAC Power Pulsing Control	Active H
88	pwr_on_adc	Digital Input	Slow shaper Power Pulsing Control	Active H
89	pwr_on_a	Digital Input	Analog Part Power Pulsing Control	Active H
90	pwr_on_d	Digital Input	Digital Power Pulsing Control	Active H
91	ib_rec	Analog Bias	LVDS receiver bias current	
92	StartAcq	Digital Input	Start & maintain acquisition	Active H
93	val_evtp	Digital (LVDS) Input	Valid Events Signal	Active H
94	val_evtn			
95	raz_chnp	Digital (LVDS) Input	External Raz Channel	Active H
96	raz_chnn			
97	ck_5p	Digital (LVDS) Input	Slow Clock	
98	ck_5n			
99	ck_40p	Digital (LVDS) Input	40MHz Clock	
100	ck_40n			
101	**vssd**	Power	Digital part Bulk	**to GND**
102	resetb	Digital Input	Reset ASIC digital part	Active L
103	rtn	Power	Open Collector Ground	**to GND**
104	Dout1b	Digital (OC) Output	Data Serial Output	Open Collector
105	Dout2b	Digital (OC) Output	Data Serial Output	Open Collector
106	TransmitOn1b	Digital (OC) Output	Active data readout	Open Collector / Active L
107	TransmitOn2b	Digital (OC) Output	Active data readout	Open Collector / Active L
108	ChipSatb	Digital (OC) Output	Chip is Full	Open Collector / Active L
109	RstCounterb	Digital Input	Reset Gray Counter	Active L
110	StartReadout1	Digital Input	Digital RAM start reading signal	Active H
111	StartReadout2	Digital Input	Digital RAM start reading signal	Active H
112	EndReadout1	Digital Output	Digital RAM end reading signal	Active H
113	EndReadout2	Digital Output	Digital RAM end reading signal	Active H
114	select	Digital Input	Select Slow Control Register (1) or Read Register (0)	
115	sr_rstb	Digital Input	Selected Register Reset	Active L
116	sr_ck	Digital Input	Selected Register Clock	Active ↑
117	sr_in	Digital Input	Selected Register Input	
118	sr_out	Digital Output	Selected Register Output	
119	**hold**	Digital Input	Hold Signal	Active H
120	**vddd**	Power	Digital (LVDS receivers & digital glue) Power Supply	**to 3.3V**
121	**vssd**	Power	Digital part Bulk	**to GND**
122	gndd	Power	Digital (LVDS receivers & Digital glue) Ground	to GND
123	ibo_d	Analog Bias	Discriminator output stage bias current	
124	ibi_d	Analog Bias	Discriminator input stage bias current	100k to vdd_discri
125	gnd_discri	Power	Analog (Discriminator) Ground	to GND
126	**vssm**	Power	Mixed part Bulk	**to GND**
127	**vssa**	Power	Analog part Bulk	**to GND**
128	**out_sh**	Analog Output	multiplexed Shaper Output (HG or LG)	

129	out_t&h	Analog Output	Multiplexed shaper Output after t&h	
130	ib_otaq	Analog Bias	Analog Outputs (Shapers) OTA bias current	15k to vdd_sh
131	ibo_sh	Analog Bias	Shaper output stage bias	100k gnd_sh
132	ibi_sh	Analog Bias	Shaper input stage bias	61k gnd_sh
133	ibgb_pa	Analog Bias	pac bias	280k vdd_pa
134	Ibm_pa	Analog Bias	pac bias current	50K to vdd_pa
135	Ibo_pa	Analog Bias	pac bias current	250k to vdd_pa
136	Ibi_pa	Analog Bias	pac bias current	7.3k vdd_pa
137	vdd_sc	Power	Slow control Power Supply	to 3.3V
138	gnd_sc	Power	Slow control Ground	to GND
139	vssa	Power	Analog Ground	to GND
140	gnd2_pa	Power	ground 2 of the PAC	to GND
141	gnd_capa	Power	Analog (Hold Capacitor) Ground	to GND
142	gnd_sh	Power	Analog (Shaper) Ground	to GND
143	vdd_sh	Power	Analog (Shaper) Power Supply	to 3.3V
144	vssi	Power	Analog part Bulk	to GND
145	gnd_pa	Power	Analog (PreAmplifiers) Ground	to GND
146	in<0>	Analog Input		
147	in<1>	Analog Input		
148	in<2>	Analog Input		
149	in<3>	Analog Input		
150	in<4>	Analog Input		
151	in<5>	Analog Input		
152	in<6>	Analog Input		
153	in<7>	Analog Input		
154	in<8>	Analog Input		
155	in<9>	Analog Input		
156	in<10>	Analog Input		
157	in<11>	Analog Input		
158	in<12>	Analog Input		
159	in<13>	Analog Input		
160	gnd_pa	Power	Analog (PreAmplifiers) Ground	to GND

Table 14 – LQFP 160 pinout

12 Bug list & hotfix log

- Non recorded

13 Document version

Version	Date	Pages	Changelog
0.2	18/09/2018	33	Initial Release
0.3	03/04/2019	34	Updated info in pinlist
0.4	07/01/2021	44	Updated information, document structure revised
0.5	12/04/2022	40	New packaging ASIC