weeroc

High-end Microelectronics Design

GEMROC Evaluation Board Software User Guide

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1 Introduction

Gemroc is a 64-channel front end ASIC dedicated to the read-out of gaseous detectors (Micromegas). Dynamic range: 2fC up to 500 fC (dedicated for MICROMEGAS or GEM detectors).

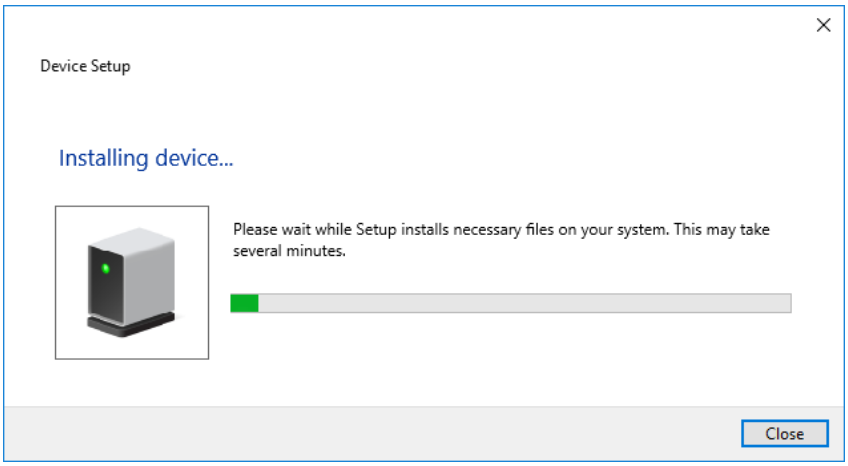
2 Installation & Test of the evaluation board

2.1 Pre requisites

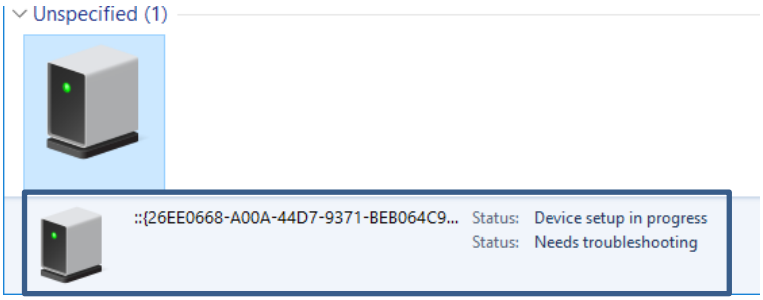
The use of this PCB requires:

- A computer (windows OS) with USB connection
- The FTDI driver that you can find on their website: https://www.ftdichip.com/Drivers/D2XX.htm
- A USB-A to mini-USB cable
- An External supply source for the board(Supply: 6.5V; -7.5V on J1 connector)

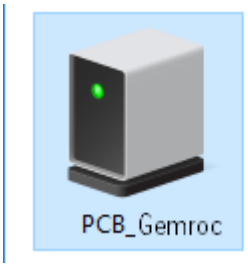
The first time a Weeroc testboard is plugged, the following message should prompt.



In order to verify that the drivers are correctly installed, go in the control panel under the "Devices and Printers" window. PCB_GEMROC device should have gone from



To



2.2 Installation guide

Before running the software for the first time, please verify that the testboard is correctly identified in the "Devices and Printers" window under the control panel. The release of the GEMROC user interface can be found in the Weeroc download center on the website http://www.weeroc.com .

3 Evaluation board presentation

This evaluation board is mainly developed to allow characterization and debug of the ASIC. Some features were added on the board or in the firmware/software in order to allow its use with real detector or within an experiment. Schematics of this board, firmware and software code sources are provided so that users can modify this evaluation system to fit their requirements.

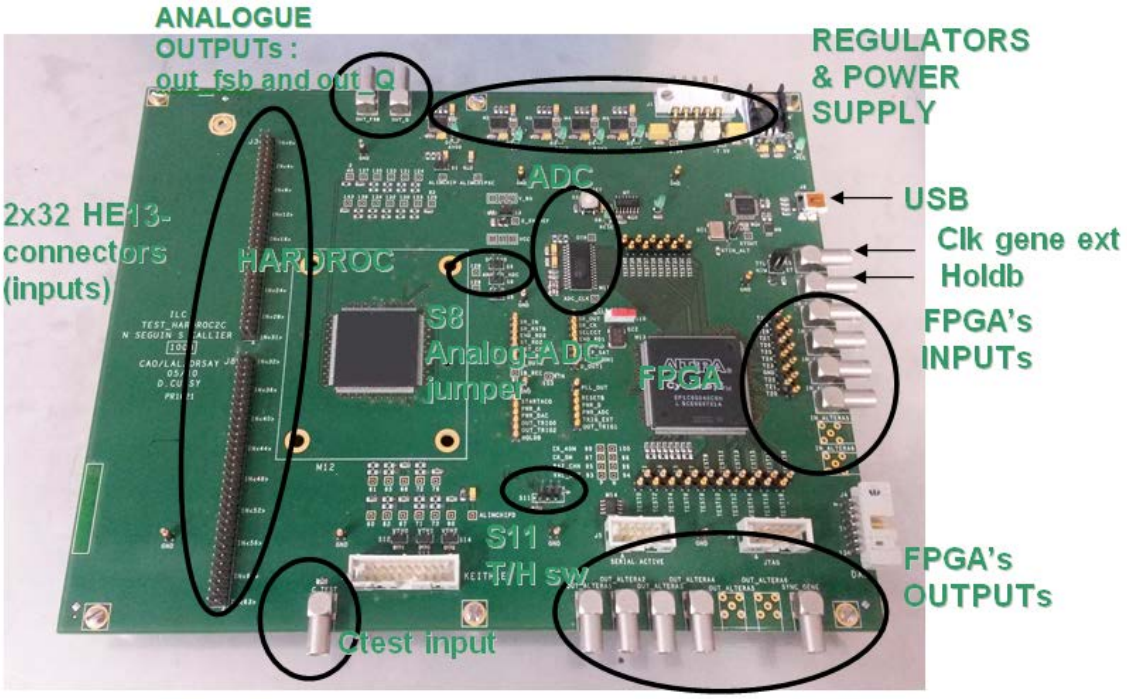


Figure 1 – Evaluation board switches, I/Os and power supply connectors

- The PCB allows easy access to each Gemroc's pin, as all analogue pins are connected to "square" holes (where the pin number is written on the silkscreen layer) and as all the digitals I/Os are connected to probes between the ASIC and the FPGA.
- Many test points are also connected to the FPGA, outputting digital internal nodes.
- The 3 OR64 trigger signals outputs are available on connectors
- 2 analogue buffers provide ASIC's analogue outputs on connectors: out_fsb for the output of the fast shaper (0, 1 or 2) and out_Q for the output of the charge (analogue memory after the slow shaper).
- 1 external ADC is on-board, allowing ASIC data acquisitions. A jumper must be put on S8 to send the analog output to the ADC as well as on S11 to select the "Hold" position.

Note that Gemroc power consumption can be monitored on connector S1 as a 10 Ohms resistor is inserted in series with the power line.

3.1 Setup for power supply

This board can be powered by a test bench DC power with a 6.5V and -7.5V power supply.
J1 connector is used to connect the board to an external DC power supply.

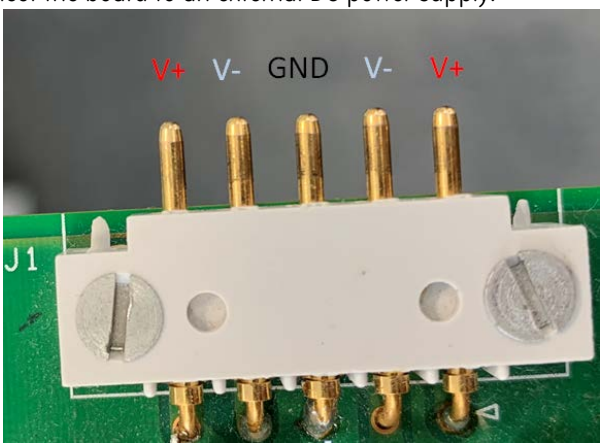


Figure 2 – Gemroc power supply connector.

4 Software interface

4.1 Setup tab

The software has been written in the C# language and has been developed with visual studio. The source code is available to help comprehend the functionality of this software. This is especially useful if users aim to develop their own DAQ system.

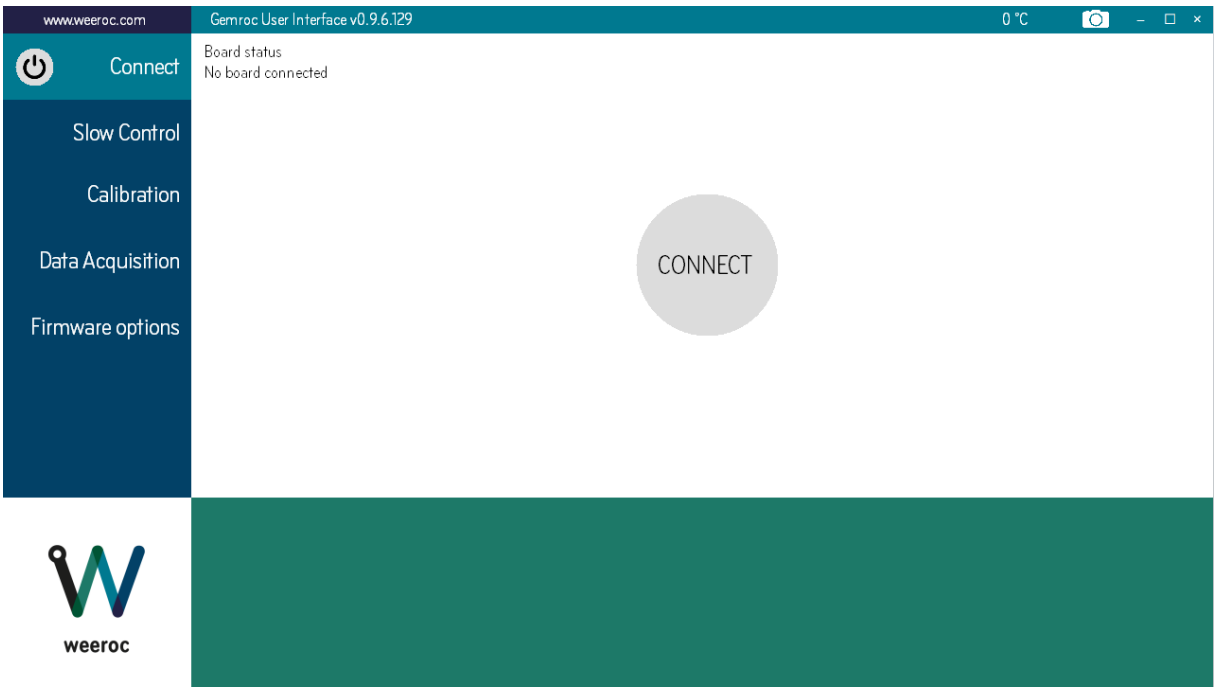


Figure 3 – Gemroc software connect tab.

To start the evaluation board, the following steps are required:

1. Connect the USB cable from the PCB to your computer.
2. Provide power supply to the PCB because it is not provided by the USB.
3. Start the software and click on the "Connect" round button.

When connecting the evaluation board, drivers for the USB device should install automatically. If it is not the case, the drivers can be found on the FTDI website (http://www.ftdichip.com/Drivers/D2XX.htm).

When this software is launched and the "Connect" button clicked, no error should occur, meaning that the installation has been done successfully and all the drivers and dll have been found. If a crash occurs or if you need assistance for any other issue with the software, contact the Weeroc support by opening a new support ticket at the address http://www.weeroc.com/my-weeroc/support.

While this guide will help users to use this software and evaluation board, it should be noted that there is an embedded help in the software. By hovering controls with the mouse, the green bottom part will be filled with information on the object being hovered.

4.2 Slow Control and Read tabs

All the slow control parameters (referred as SC afterwards) of the GEMROC are displayed on 4 tabs, allowing tuning & tests of different settings.

To program the GEMROC, just click once on the "Send SC" button available on any tab. In each SC related tabs, there is an indicator displaying the status of this SC register and should be green after a "Send SC" command.

The Slow Control settings tab can be saved in a text format file through "Save SC" button, and reloaded from this file by the "Load SC" button. Note that the path & name for this file has to be provided in the saving pop up page.

To load old GEMROC software slow controls from LabVIEW press the "Import LV file" button.

To send the Read Register, select the channel and click on "Send Read Register". It's also possible to reset the read register by clicking on the "Reset Read Register button".

4.2.1 Slow Control 1 – Main settings: Analog front end and digital settings

The "Main settings" tab allows users to access various parameters of the analog and the digital part of this ASIC. The parameters here will affect the behaviour of the whole ASIC.

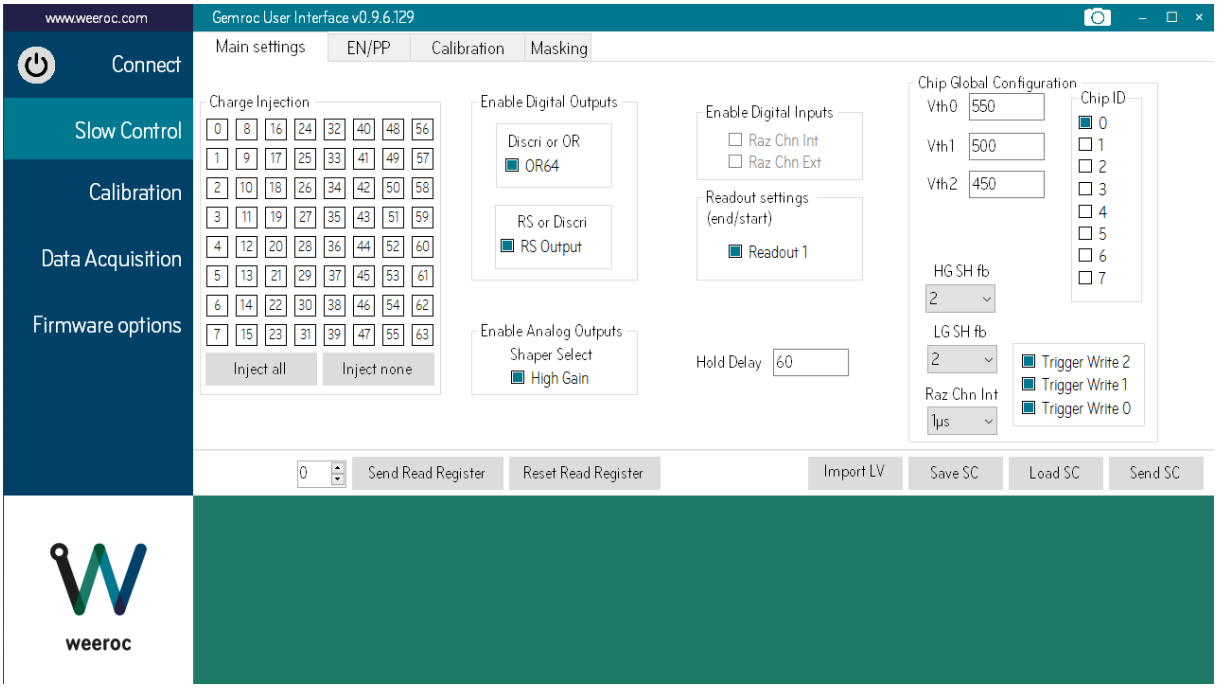


Figure 4 – Slow Control "Main settings" tab

In this section, it is possible to set up some important ASIC parameters such as the trigger thresholds (Vth0, Vth1 and Vth2) where users need to put a code value between 0 and 1023 to see the threshold voltage changes.

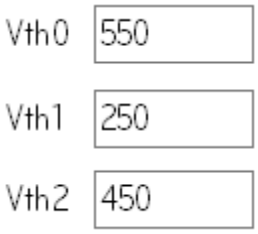


Figure 5 – Slow control Threshold Value

With the Charge injection matrix setting, it is possible for users to select the channels which will receive charge injection stimuli.

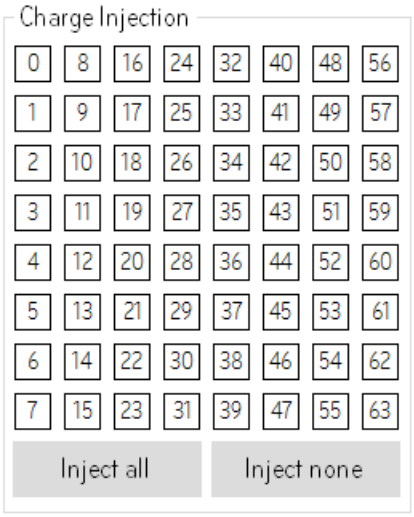


Figure 6 – Slow control trigger charge injection matrix

On this page user can change the hold delay from the track and hold parameter (note that this is a FPGA parameter and it is only needed to enter a new value to change it).

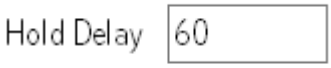


Figure 7 – Slow control Hold Delay

Within this page it is also possible to enable or not the different Digital input and output options.

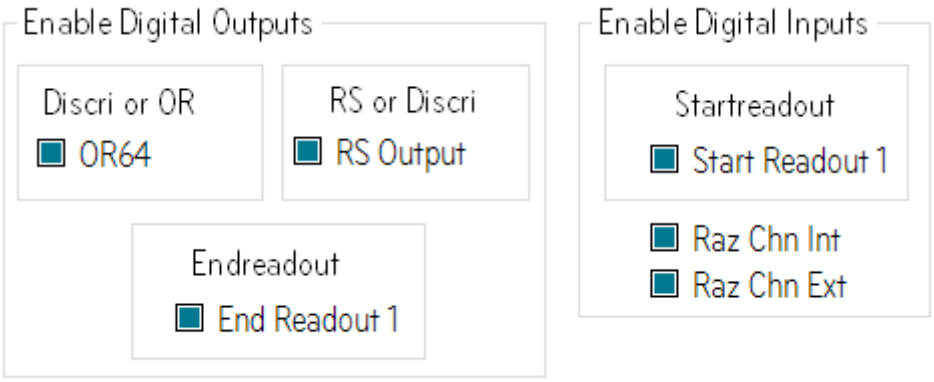


Figure 8 – Slow control Enable Digital I/O

The Discri or OR option allow user to read data provided by the OR64 of the ASIC (OR64) or a specific channel (Read Chan. - it need to be set up with the read register. Refer to Read Register section).

RS or Discri is a latch trigger option, it allow user to latch the output trigger (RS) or direct trigger output (Direct output).

Raz Chn Int/Ext allow user to enable the internal and external reset signal for discriminator latch.

In the global configuration settings you will find also the chip ID where the user can define the ID of the chip in order to make the difference between some ASIC which will be embedded in digital data output.

User will also find the gain and shaping time adjustment of the high gain and low gain shapers.

It's also possible to change the Raz Chn Int (internal discriminator Latch reset) delay in this section.

Lastly user can set digital readout authorisation based on the combination of 3 triggers available in this ASIC (Trigger Write 0, Trigger Write 1 or Trigger Write 2).

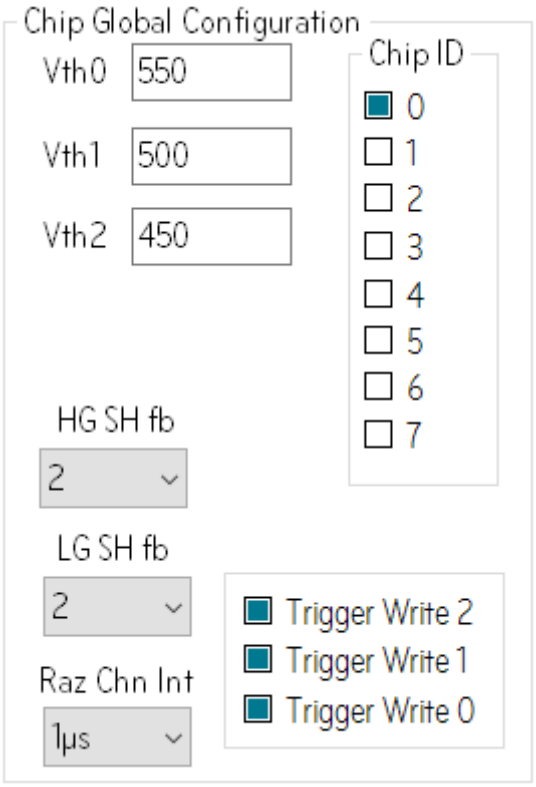


Figure 9 – Slow control Chip Global Configuration

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4.2.2 Slow Control 2 – Enable tab

This Slow Control tab has been created to allow user to enable or disable some ASIC part and also put some part on Power Pulsing (On/Off) mode (Please find information on the options of this tab page in the slow control part of the datasheet).

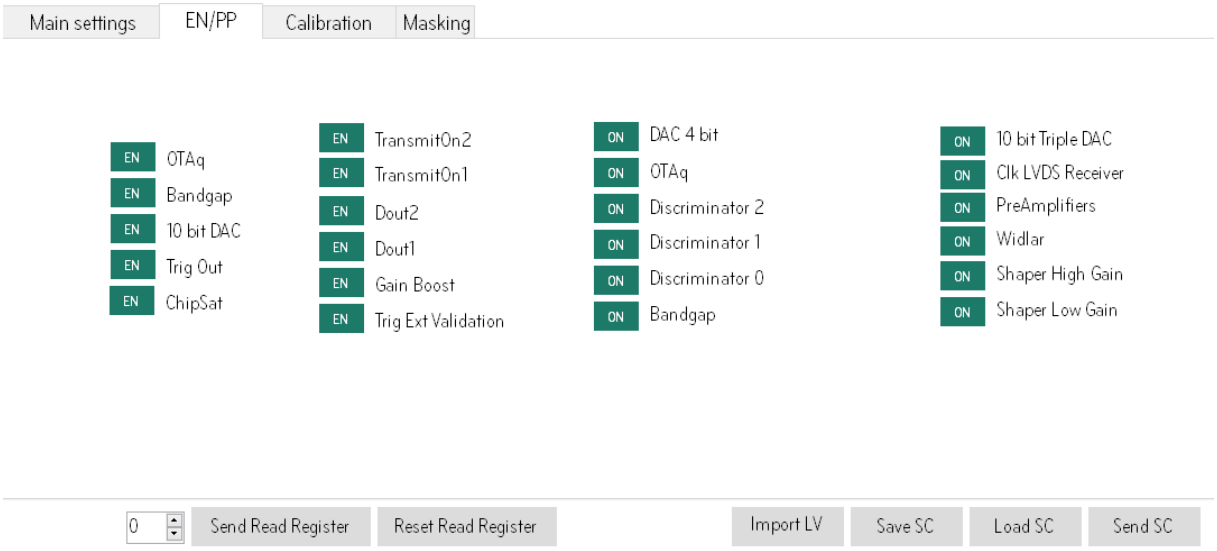

Figure 10 – Slow Control 2 tab – Enable and disable tab

4.2.3 Slow Control 3 – Calibration tab

Slow Control 3 tab is for fine tuning threshold charge. Threshold can be tuned individually for each channel via a DAC adjustment parameter. Users can choose to adjust the threshold value for each channel, use a common value for all channels or apply a value to a specific channel and another value for other channels. All the channel values can be changed at the same time with the set all option and the associated text box and button.

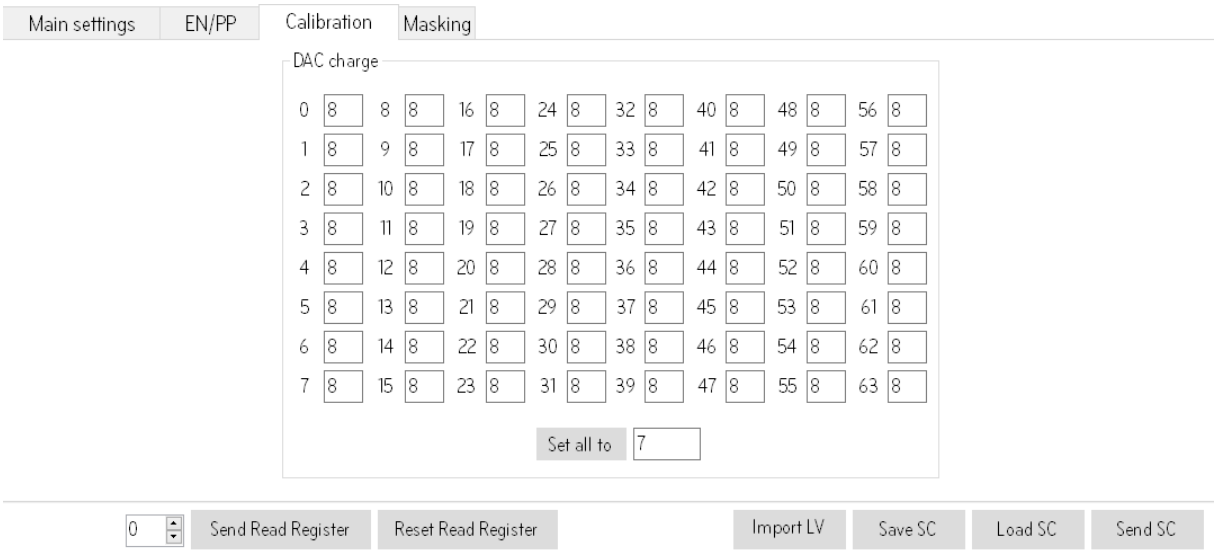

Figure 11 – Slow Control 3 tab – Calibration tab

4.2.4 Slow Control 4 – Masking tab

Slow Control 4 tab is dedicated to the channel masking/enable. User can select the channels he wants to mask or not, this result a channel with no triggers. All the channels can be masked or unmasked with the associated buttons.

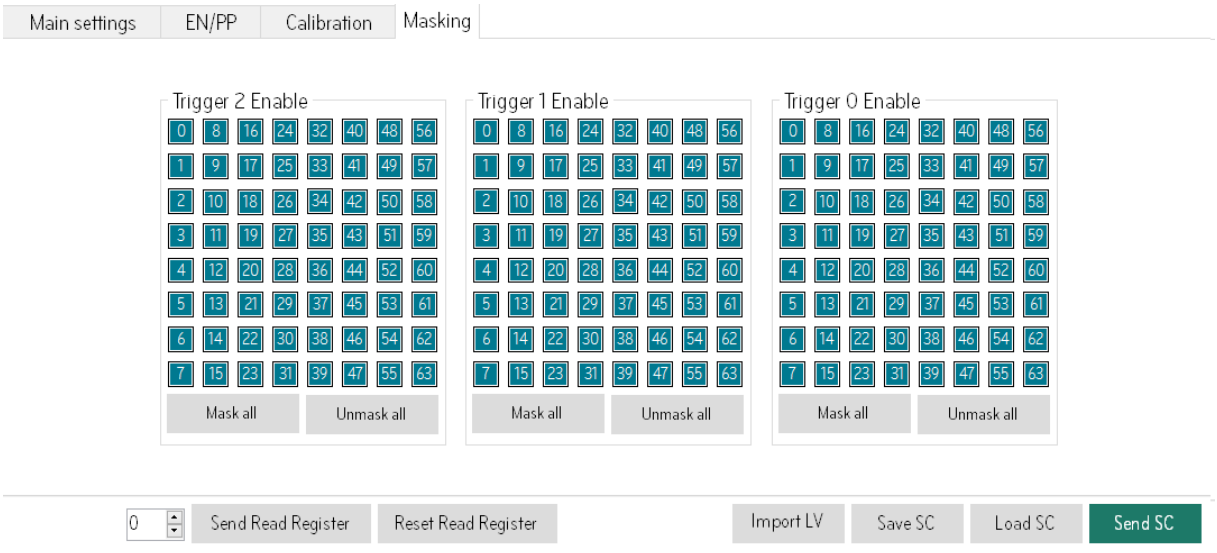

Figure 12 – Slow Control 4 tab – Masking tab

4.2.5 Read Register

In the slow control page user will find the read register settings which is a shift register which allows outputting sequentially the analogue hold data from the Analogue Memory (SCA) (OUT_Q) and shaper output (OUT_FSB) to pins 129 and 128 (also buffered on connectors and DC level monitored on S9 & S6 respectively). This register is controlled by the channel number box and the send read register button.

A hold signal has to be provided to the board at the maximum signal of the charge, and the switch S11 has to be set on the "HOLDB" mode, otherwise, no hold is performed on the analogue memory. The "TRACK" mode is only useful for debug. Note that display shown using that mode does not indicate the maximum value of the charge, as internal buffers have low biasing current for saving power consumption and thus slow down the signal displayed.

Note that in order to see the Triggers from the chip, "Raz Chn Int" has to be disabled and "RS or discri" has to be set on "Direct output" in main the Slow Control tab (Refer to Figure 11).

Note also that the direct individual triggers can be displayed; this requires to use this Read Register and have the Slow Control setting "Disc or OR" set to "Read Chn." instead of OR64 (Refer to Figure 8).

Figure 13 – Read Register Parameter

4.3 Firmware option configuration

This tab is essentially used for the configuration of the FPGA on board.

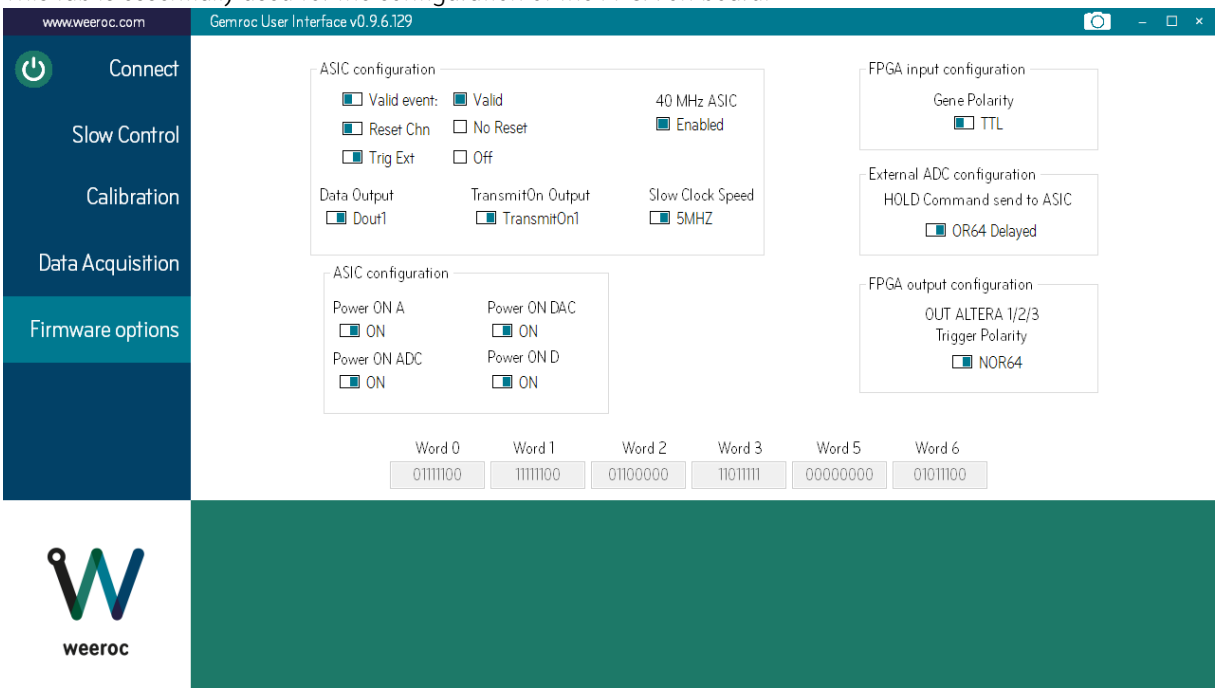

Figure 14 – Firmware Options tab

On this tab, several signals for ASIC, which are mostly related to the digital part, can be modified. The settings for some signal are displayed by a toggle switch-button. A right switch on the front page corresponding to logic value "1" or ON (example: "Valid Event" or "Reset") and vice versa.

Users can visualize the FPGA configuration word sent to evaluation board on the bottom of the page.

4.4 S-curve tests

Trigger efficiency or S-curve measurement can be accessed from the according tab. This tab is used for testing the different channels trigger efficiency in function of the threshold value. This calibration test can be performed either in digital or analog mode.

In order to perform the measurements, the following setup to the evaluation board is required:

- Reference Synchronisation on CLK GENE EXT connector for Analog S-curves
- Input signal: on-board connectors (IN <0 to 63>), Internal Charge injection (C_test). For the injection signal to be applied please refer to section 4.7.
- Users can select the injection frequency with the synchronisation signal sent by the pulser/charge injector to FPGA (refer to section 4.7). To modify this value, users have to select clock value in the clock drop-down list. Available values: 1 kHz, 10 kHz, 50 kHz and 100 kHz.

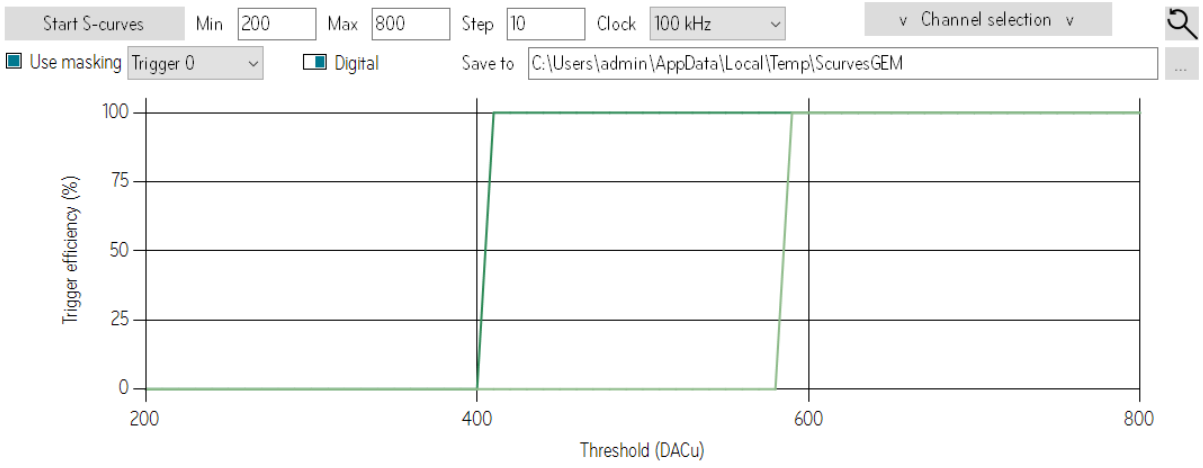

Figure 15 – S-curves test

Lastly, this tab will modify ASIC Slow Control parameter in order to make sure to perform S-Curves correctly.

The remaining fields of this tab, "Min", "Max" and "Step" should be filled accordingly to all threshold DACs range which is 10-bits, thus giving maximum DAC code of 1023.

Some slow Control parameters are automatically modified in order to perform the test correctly.

A reference clock must be provided on the CLK_GENE_EXT connector. For that, a TTL signal must be generated by the channel 2 of pulse generator (refer to Figure 24), with the same phase and frequency (10KHz-100KHz) as the injected signal generated by the channel 1.

In this tab it is possible to modify directly some parameters in order to have different test results:

- "Mask channel": If activated (Green on selected channels), only the currently measured channel will be unmasked if the "Use Masking" checkbox is check.
- "Analog/Digital S-Curves" with this switch box you can select if you want to have a digital S-Curve based on the data acquisition system or an analog S-Curves.

4.5 Hold Scan

The second tab under the calibration page is the "Hold scan". It will trace shaper output signal by varying the "hold" delay value on a single channel. Users will have to select channel to be observed in "Channel" field. In order to have it working properly a signal should be injected in the measured channel and a trigger must start the data acquisition with the external ADC (For the injection signal setup, refer to section 4.7). A fit on the result of the scan is performed and the x-axis value corresponding to the maximum of the fit is automatically extracted. The delay parameter (in Main settings tab – Figure 7) is updated with the extracted value. The fit is meant to be used with the SCA.

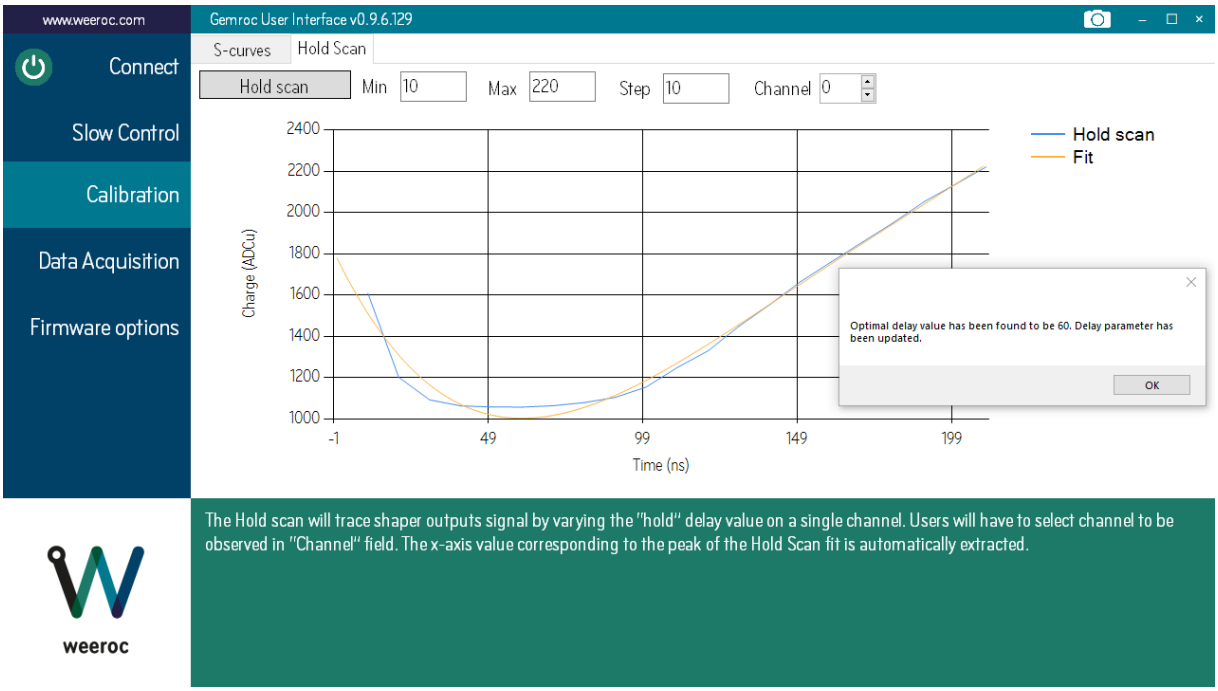

Figure 16 - Hold Scan data per channel

User can select the channel out shaper signal to plot and the Max, Min and step of the time axis of the plot. Some slow Control parameters are automatically modified in order to perform the test correctly.

4.6 Data Acquisition

4.6.1 Analog Acquisition

Gemroc has one analogue output, which can be digitized using an external ADC (AD9220 from Analog Devices embedded on the evaluation board). In order to use this ADC, pins S8 and S11 has to be set correctly with jumpers. A jumper must be put on S8 to connect the ASIC output to the ADC input. Jumper S11 (track/Hold switch) must be to set to hold mode.

Note that the hold command must be provided. This signal can be delivered externally by injected a HOLDb (active Low) signal through the dedicated connector (refer to Figure 1). It can also be provided by a delayed OR64 Trigger signal. The hold command should arrive at the maximum value of the analogue charge (corresponding to the peaking time).

A simple DAQ interface is also available, the data acquisition will be started when "Start Acquisition" is clicked and the number in "Number of Acquisition" field will indicate how many times the ASIC will be readout. The digital acquisition can be turned off in order to perform only analog acquisition by turning off the associated switchbox.

The tab 1 is used to display the analog data per channel for all the acquisitions (user can select the channel to display with the associated numberbox).

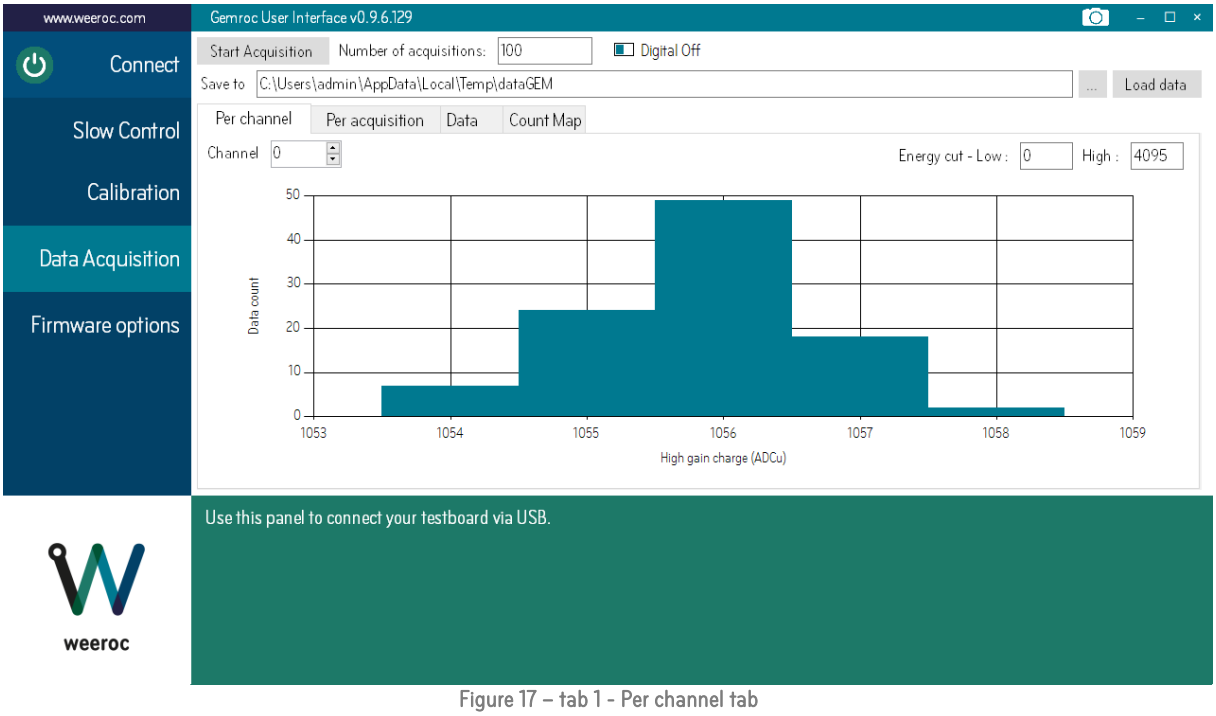

Figure 17 – tab 1 - Per channel tab

The tab 1 is used to display the analog data per acquisition for all the channels (user can select the acquisition to display with the associated numberbox).

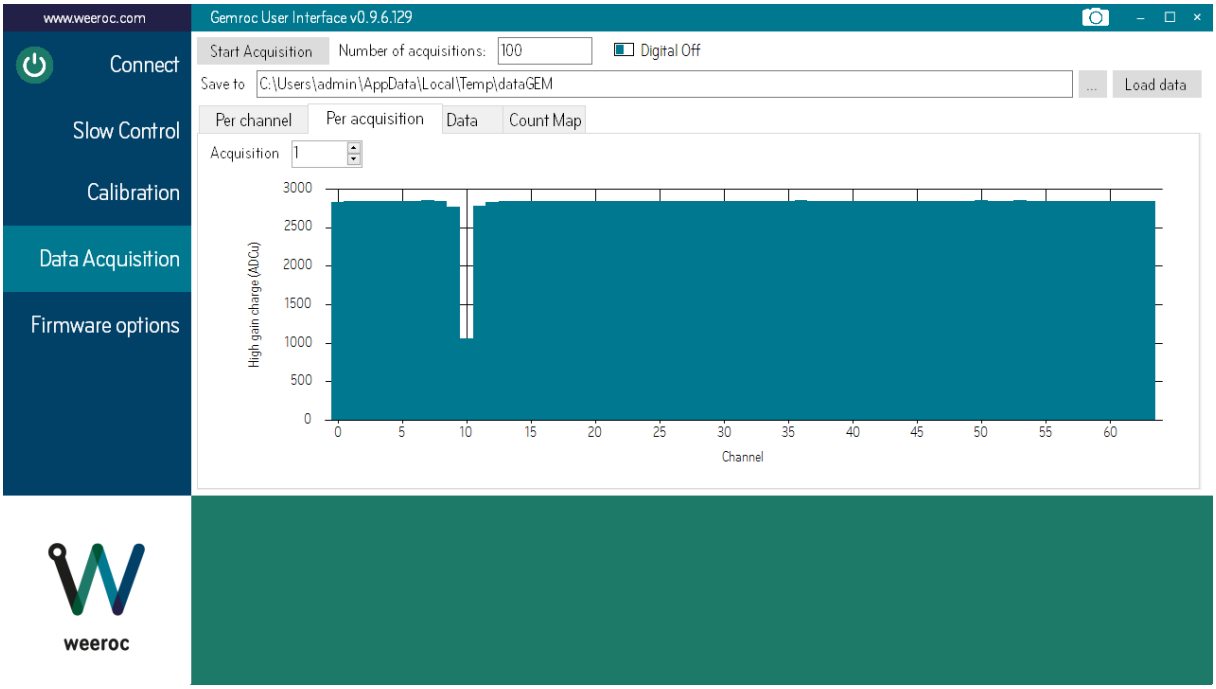

Figure 18 – tab 2 - Per acquisition tab

4.6.2 Digital Acquisition

This page is useful to perform digital acquisitions using the digital part of the ASIC. User has to specify the clock used by the ASIC, which will be used as time tagging reference. It can be either the FPGA internal one (5 or 2.5 MHz) or external clock provided by the user (from 300 kHz up to 5 MHz).

The tab 3 is used mainly for debugging the digital DAQ system, as it will display raw data and decoded data from the digital part of the ASIC. Here user can find the acquisition number, the chip ID which is the identity code of the ASIC (defined in the slow control), the BCID which is a time indicator for the current acquisition and the trigged channel per threeshold (0, 1, 2) and per acquisition (the channel number is indicated under the triggers number).

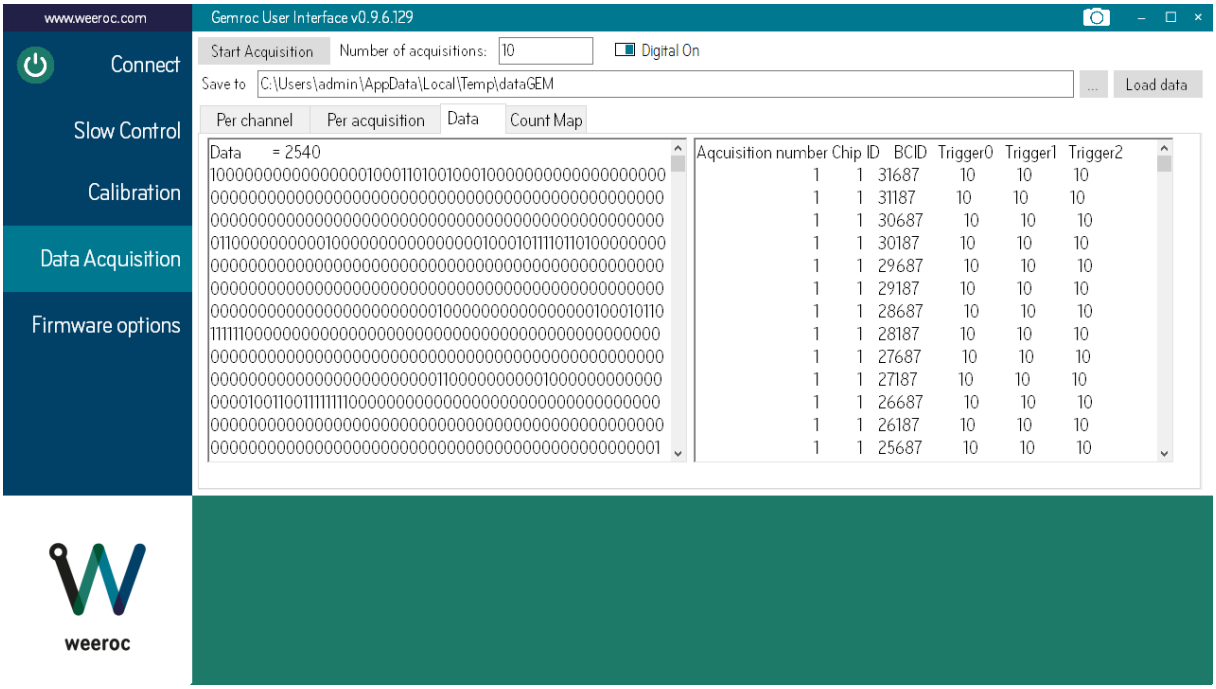

Figure 19 – tab 3 - Raw Data tab

The tab 4 is used to display a matrix of all the channels with the name of fired trigger (T0, T1 or T2) per channel and per acquisition with the digital part of the ASIC (user can display the acquisition with the associated field).

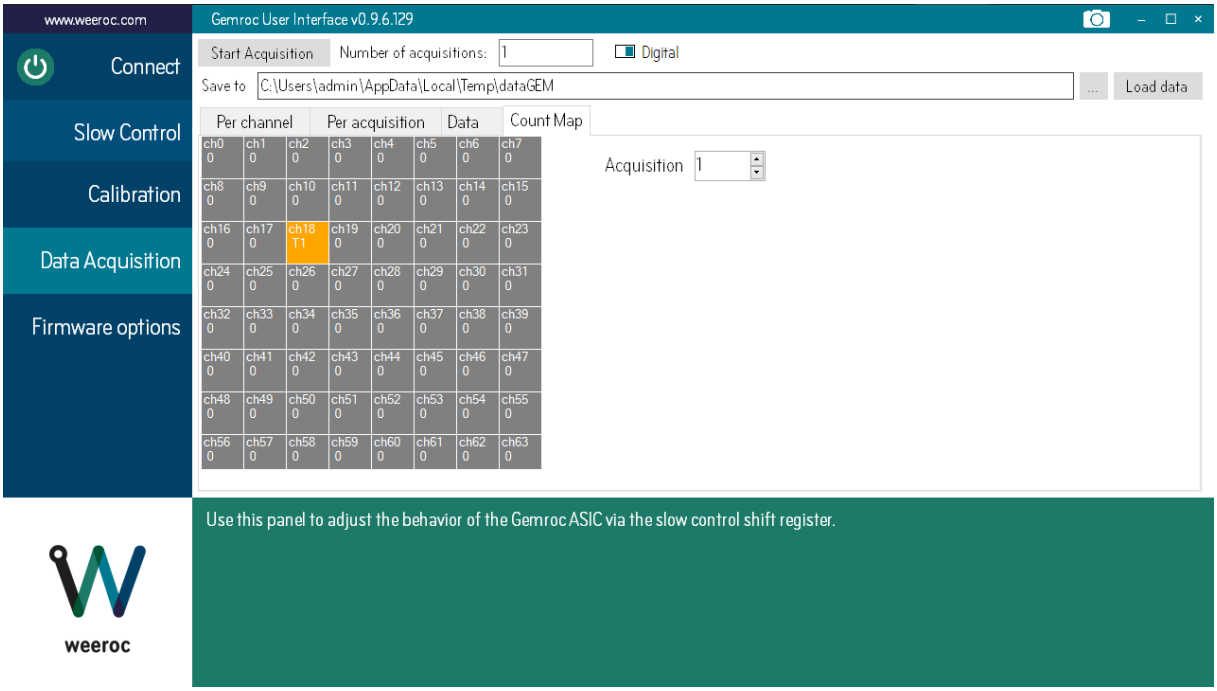

Figure 20 – tab 4 - Flood map tab

The triggers are given by an output code of the digital decoding as described in Table1.

Triggers	Value (code)
No trigger(0)	0
T0	1
T1	2
T2	3

Table 1 – value of trig in the flood map

Those triggers are due to a comparison between the input signal and the 10-bits DAC threshold voltage (set in main Slow Control tab: Vth0, Vth1 and Vth2). If the signal is over the threshold voltage, it will result a trigger. The Vth2 is higher than the Vth1 and the Vth1 is higher than the Vth0. Therefore if the signal is higher than the Vth2 it's also higher than the Vth0 and Vth1 etc...

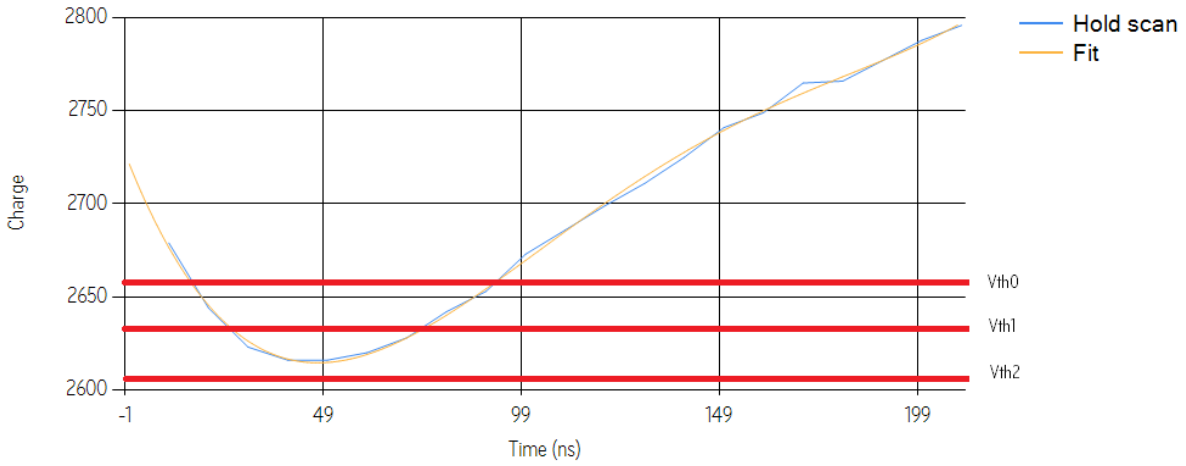

Figure 21 – Input signal vs Vth's

Users have to connect the pulser in order to inject a signal (an injection signal example is available in section 4.7 of this user guide). Some slow Control parameters are automatically modified in order to perform the test correctly. At the end of the acquisitions the data are automatically saved as a text document at the path that users have chosen on the "Save to" textbox. Users have to provide a path and name of the file in order to save the data.

Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
2842	2846	2845	2841	2843
2843	2848	2844	2842	2848

Table 2 – value of trig in the flood map

In this document format the data are separated by a single space character. With this document (as shown in Table 2) users will have the external ADC output value for all the channels and for all the acquisition.

4.7 Injection Test Signal

In order to perform Data acquisition, S-Curves and Hold Scan, a pulser injection signal can be used to simulate input signal for the ASIC. Signal produced by a Tektronix waveform generator as shown in Figure 22 can be used for this application in order to get an input signal similar provided by detector.

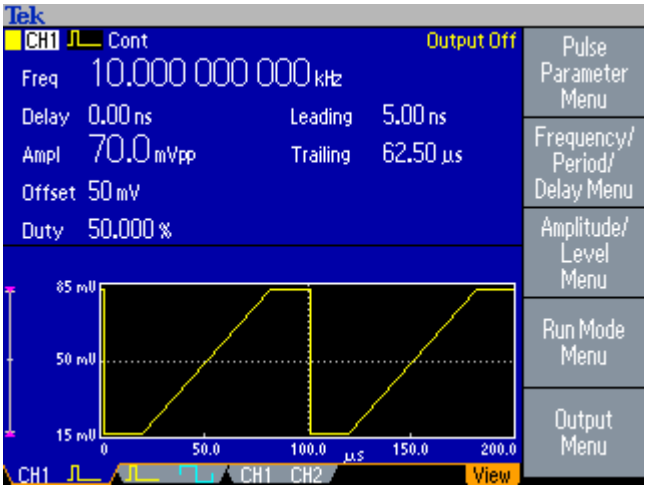

Figure 22 – Pulser injection signal

Signal Setup:

- Function : Pulse -> Continuous
- Output menu : Invert -> On
- Ampl :20µV~5mVpp(with injection in channel directly)
  1mV~250mVpp (with injection in Ctest)
- Frequency : 10~100 kHz
- Trailing Edge : 62.5 us

First tests to be more familiar with the board and the software should be done using the following setup. A negative voltage step can be injected in one channel through a 100pF capacitor in series with the signal. A 50 ohms resistor for the cable adaptation is also necessary. A specific cable with a female "BERG" female connector can be "homemade" to inject in each individual channel using the input connector which is a male HE13 - 2x32pins. A 1mV-step in 100pF simulates an injected charge of 100fC.

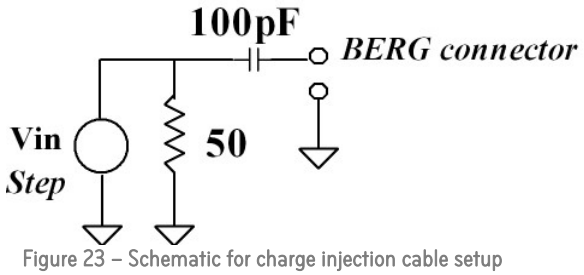

Figure 23 – Schematic for charge injection cable setup

Another way to inject charges in each channel is to use the Ctest input connector which is also available on the testboard. The step voltage is then distributed through the internal 2pF capacitor of each channel. You should select only one of the Ctest, as the number of selected Ctest impacts the amplitude of the input step signal.

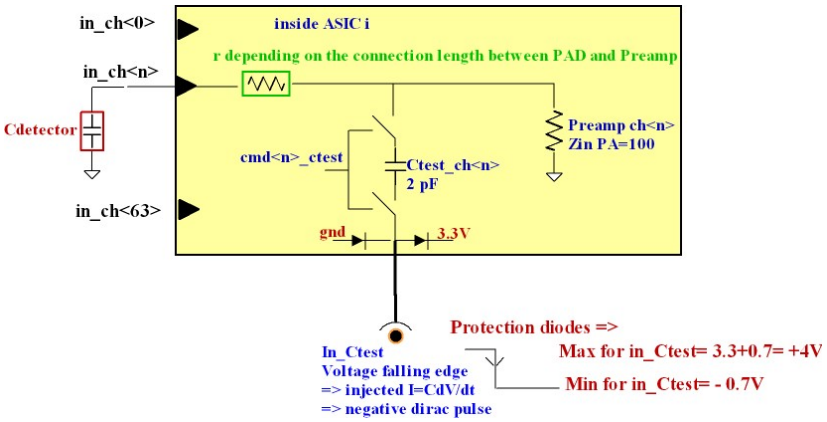

Figure 24 – Injection using Ctest

As shown in Figure 24, the second channel of the waveform generator can be used as the sync signal for the charge injection for example in S-curve tests. This is done by generating 3.6V square wave with similar frequency as the charge injection channel. Refer to section 4.4 for more information regarding the S-curve tests.

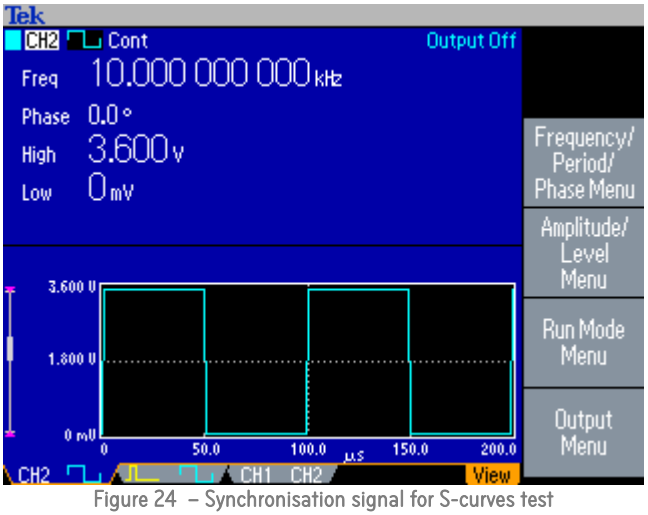

Figure 24 – Synchronisation signal for S-curves test

5 Known bugs and issues

Bug#1: If User have trouble to perform any test or to have data he should try to reset the testboard by pressing the associated button on the board and relaunched the Gemroc testboard software.

6 Document revision

Version	Date	Pages	Changelog
1.0	24/01/2020	26	Initial release for C# software. This document version related to Gemroc 1.0.0.11 software version