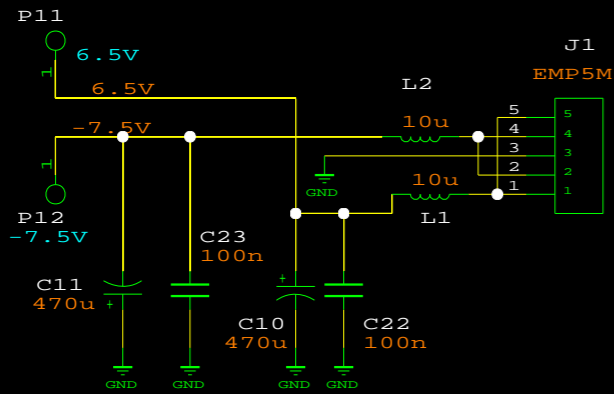


POWER SUPPLY

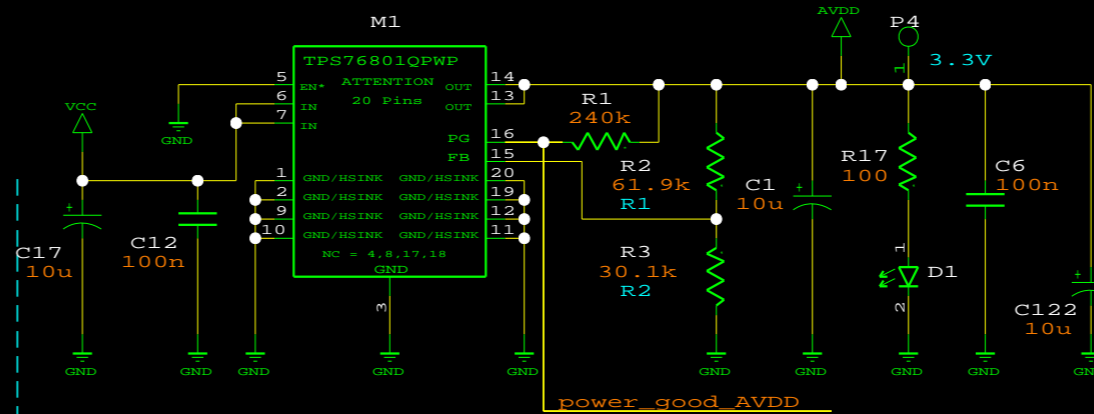
R 0805 (1%) for regulators

$$V_{reg} = 1.1834 * (1 + R1/R2) \text{ et } R2 = 30.1k$$



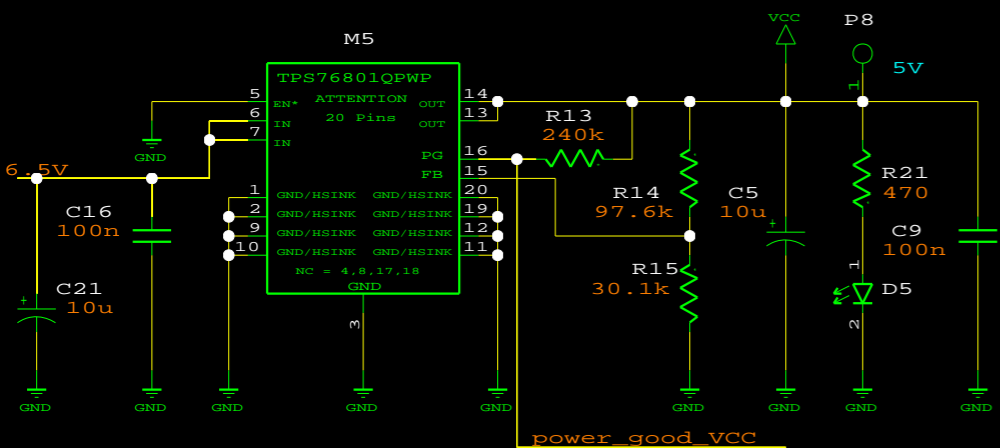
ASIC power supply

ASIC 3.3V



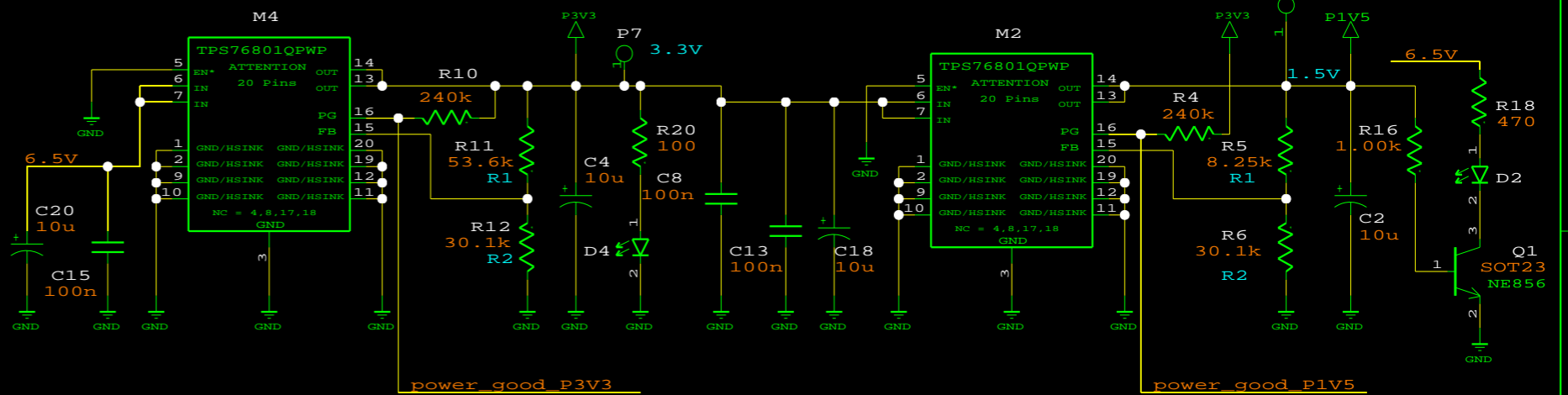
ALTERA power supply

Vcc for Buffers, USB & external ADC



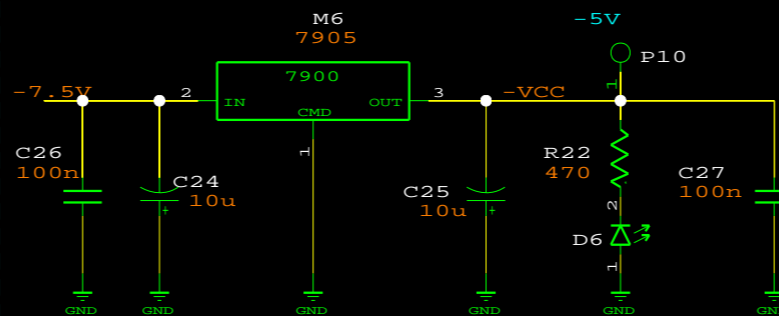
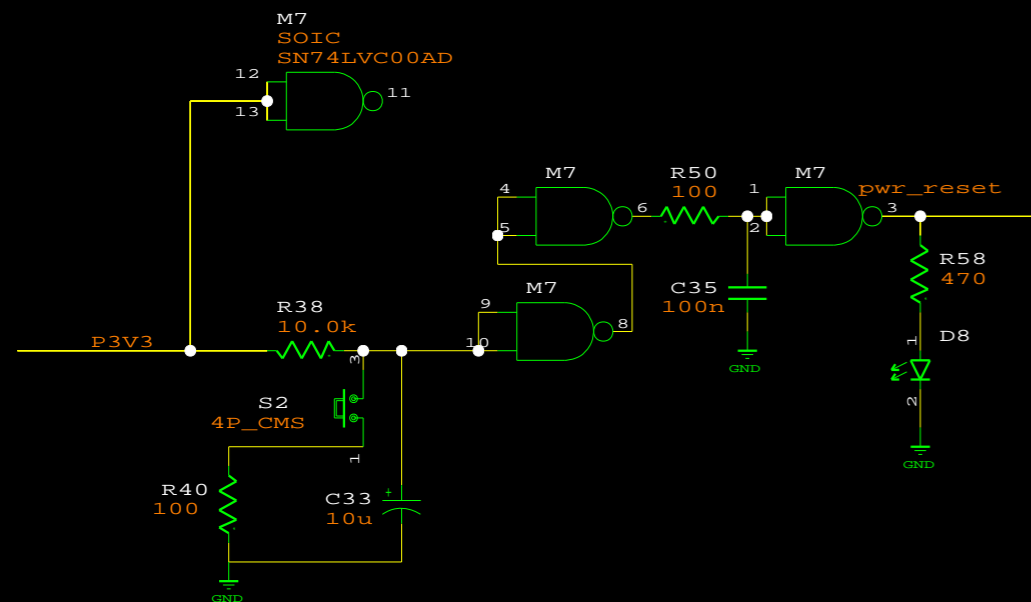
3.3V for banks 1, 2 & 3

Internal Power Supply

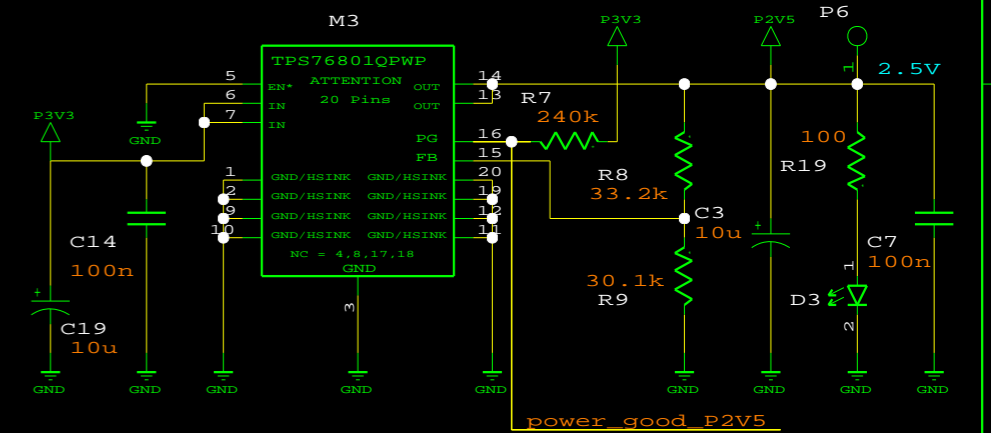


Power-on reset

negative supply for buffers



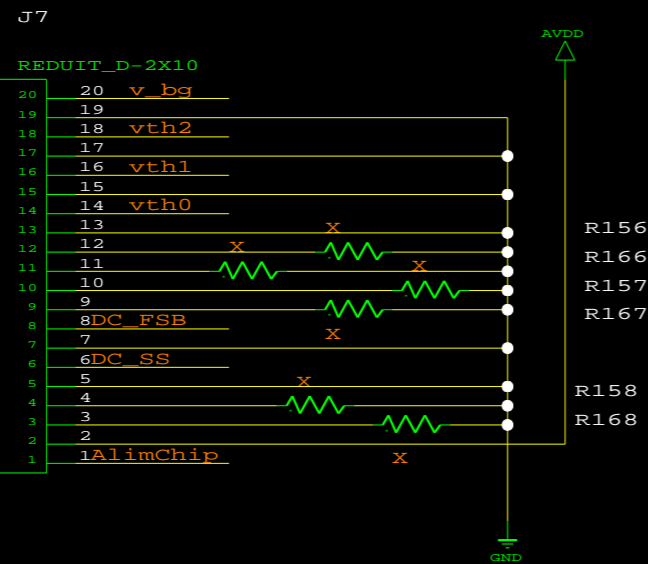
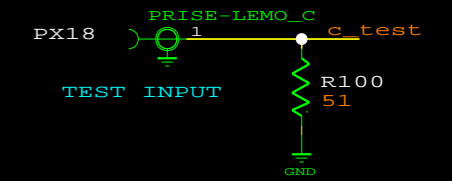
2.5V for bank 4 (LVDS)



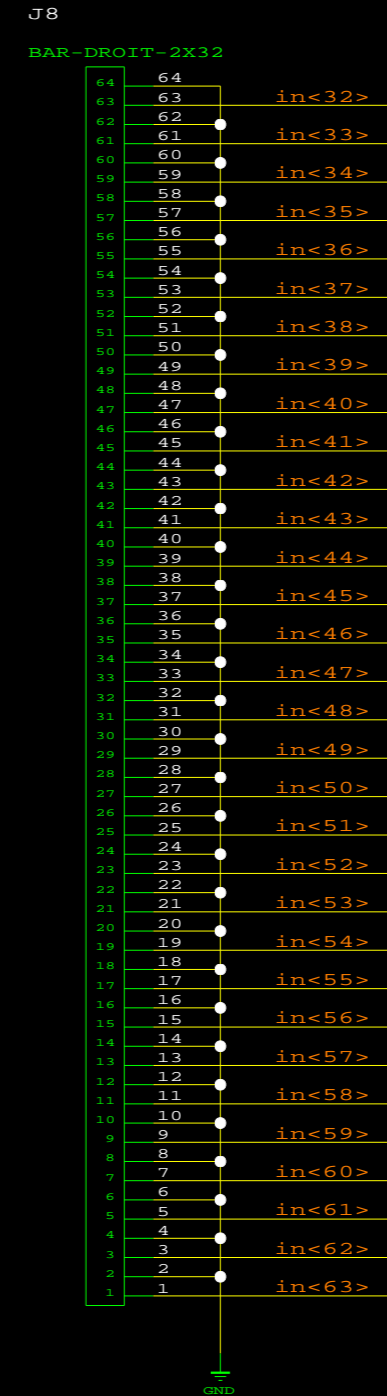
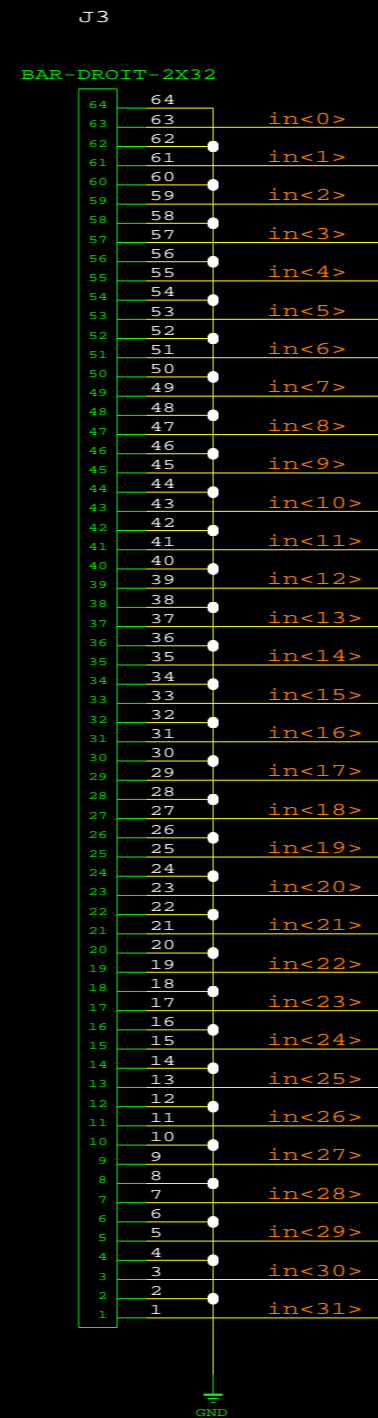
test_hardroc2c

ANALOG INPUTS

KEITHLEY DMM 2000 - CONNECTOR



Chip Consumption



MIRA1
I21
MIREALIGN

MIR2
I23
MIRELOS

MIR3
I22
MIRELOS

MIRA2
MIREALIGN
I17

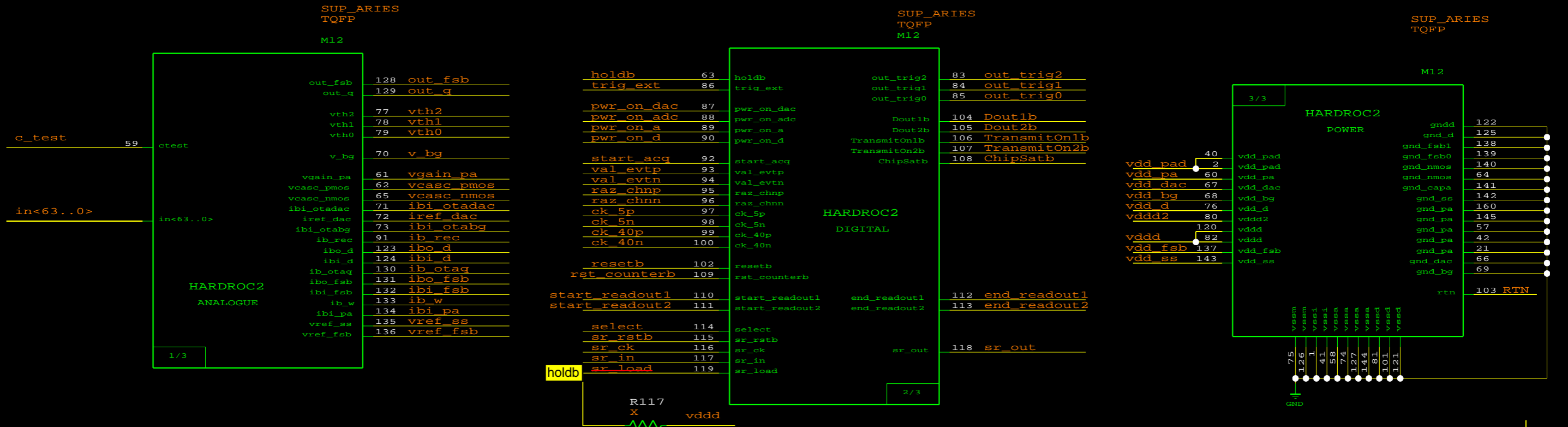
MIRT1
MIRETOP
I18

MIR1
MIRELOS
I19

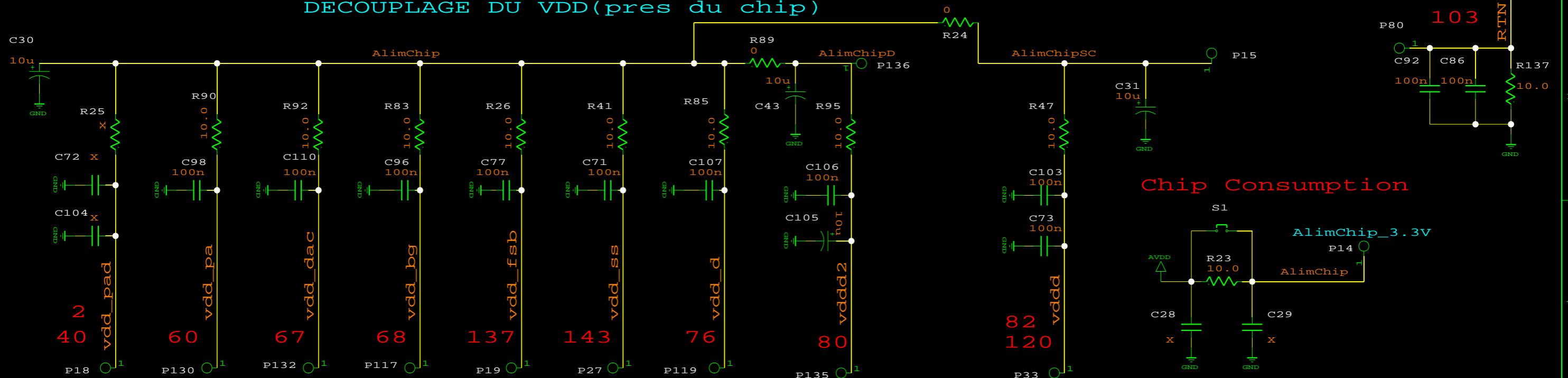
MIRB1
MIREBOT
I20

test_hardroc2c

HARDROC2 CHIP



DECOUPLAGE DU VDD(pres du chip)



test_hardroc2c

for microroc

MODIFIE: Thu May 6 10:30:53 2010

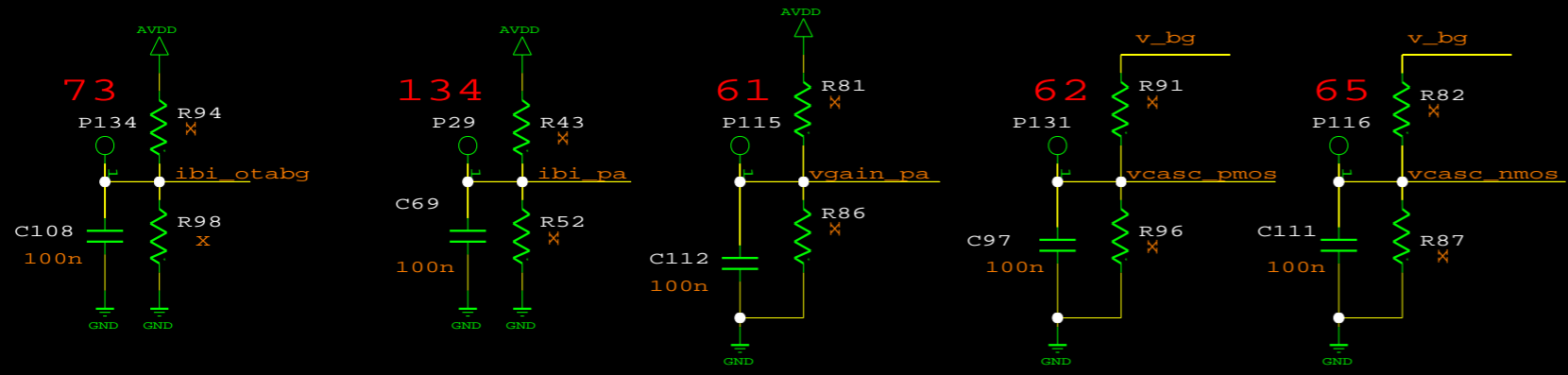
ETUDE: PAGE: 3 / 8

DESSIN:

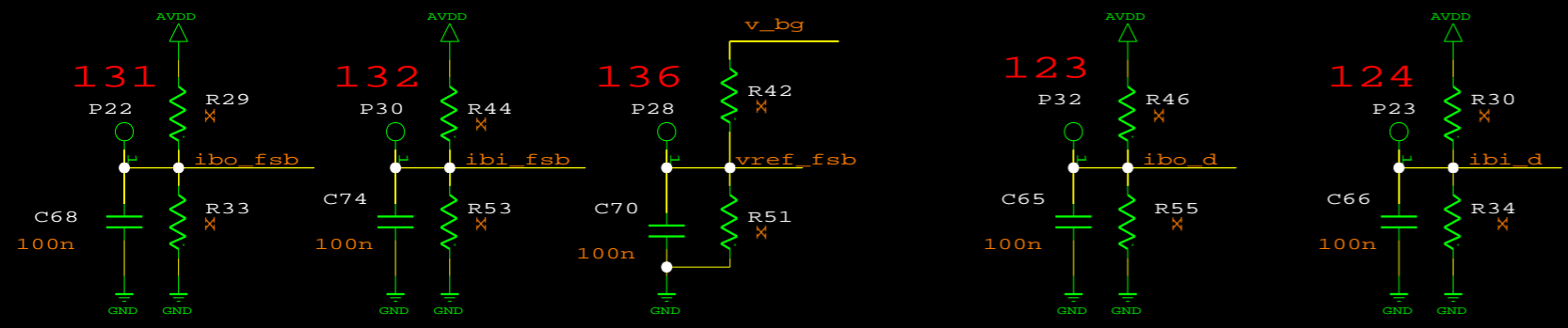
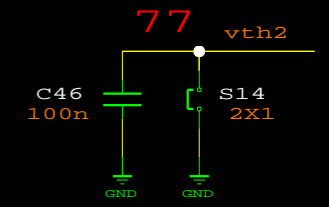
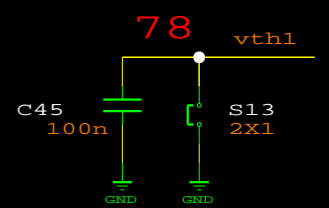
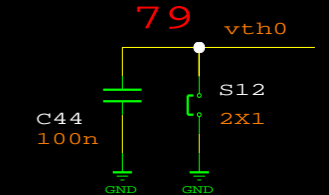


LABORATOIRE DE L'ACCELERATEUR LINEAIRE

CNRS IN2P3 U P S

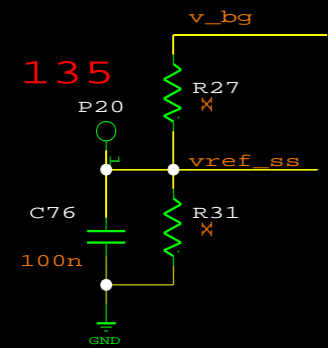


Threshold

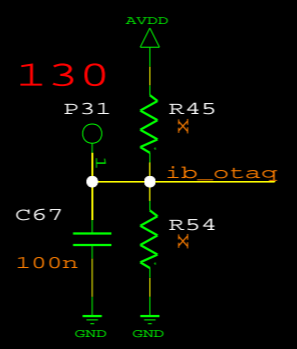


FS BIP

DISCRI SHAPER

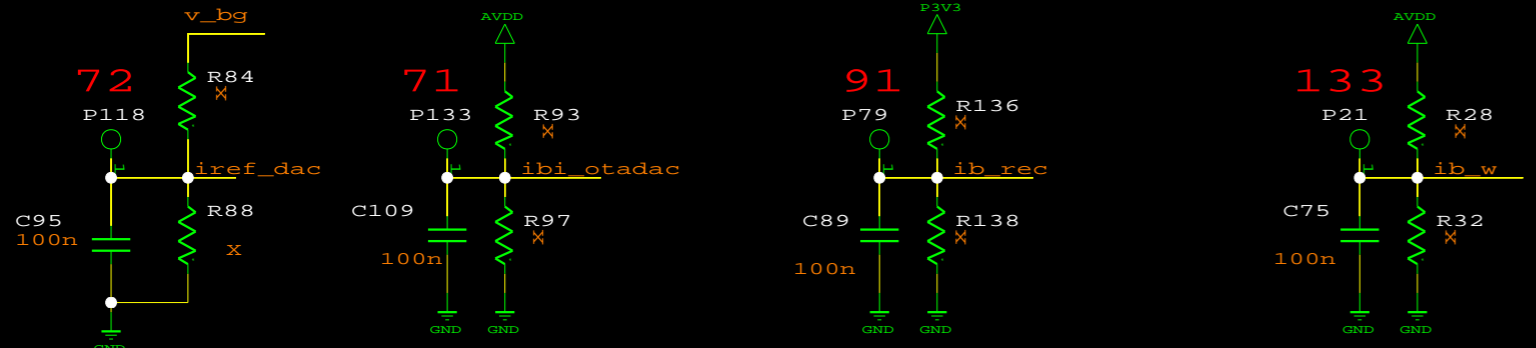
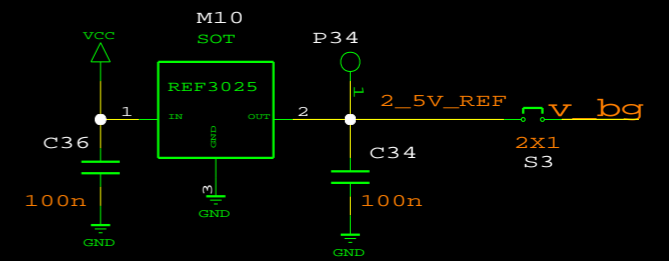


SLOW SHAPER



OTA Q and FSB

REF. VOLTAGE



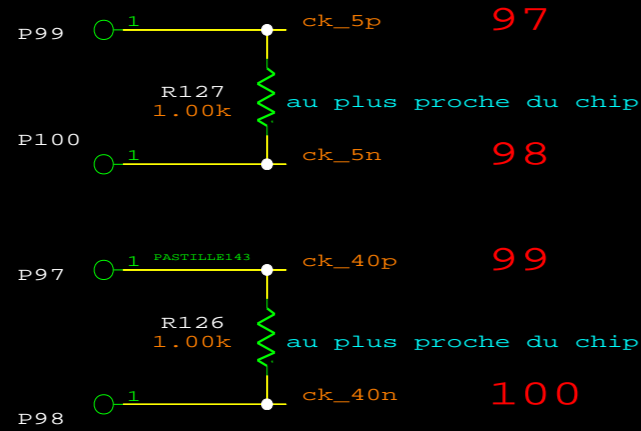
DAC

LVDS to CMOS Rec

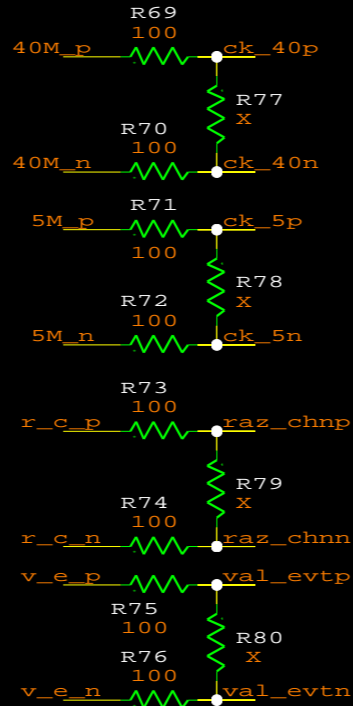
Widlar

test_hardroc2c

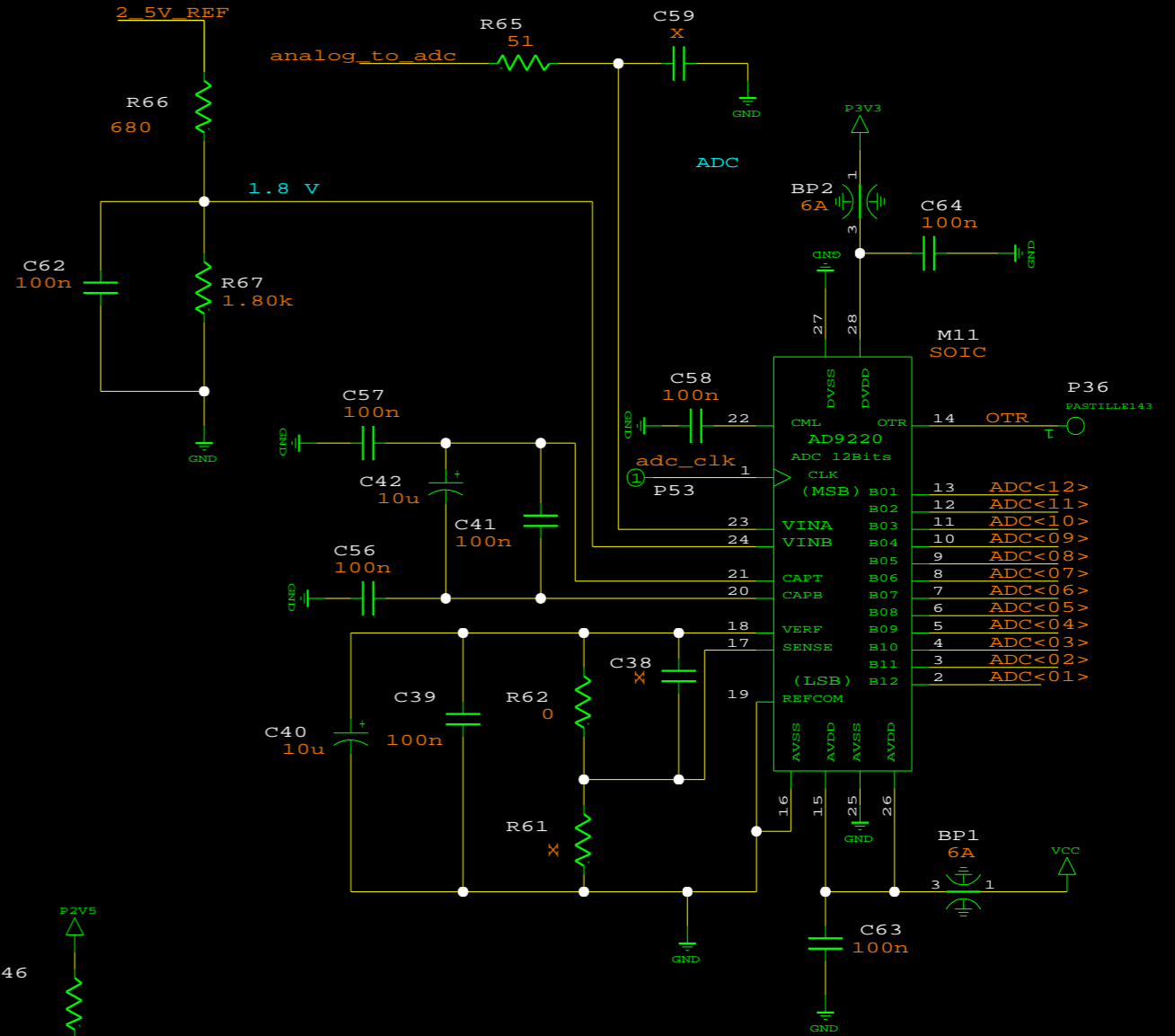
CLOCKS INPUTS



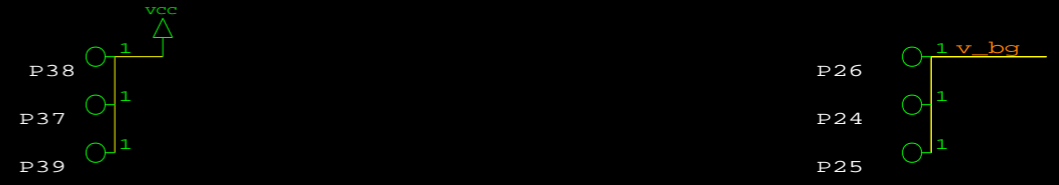
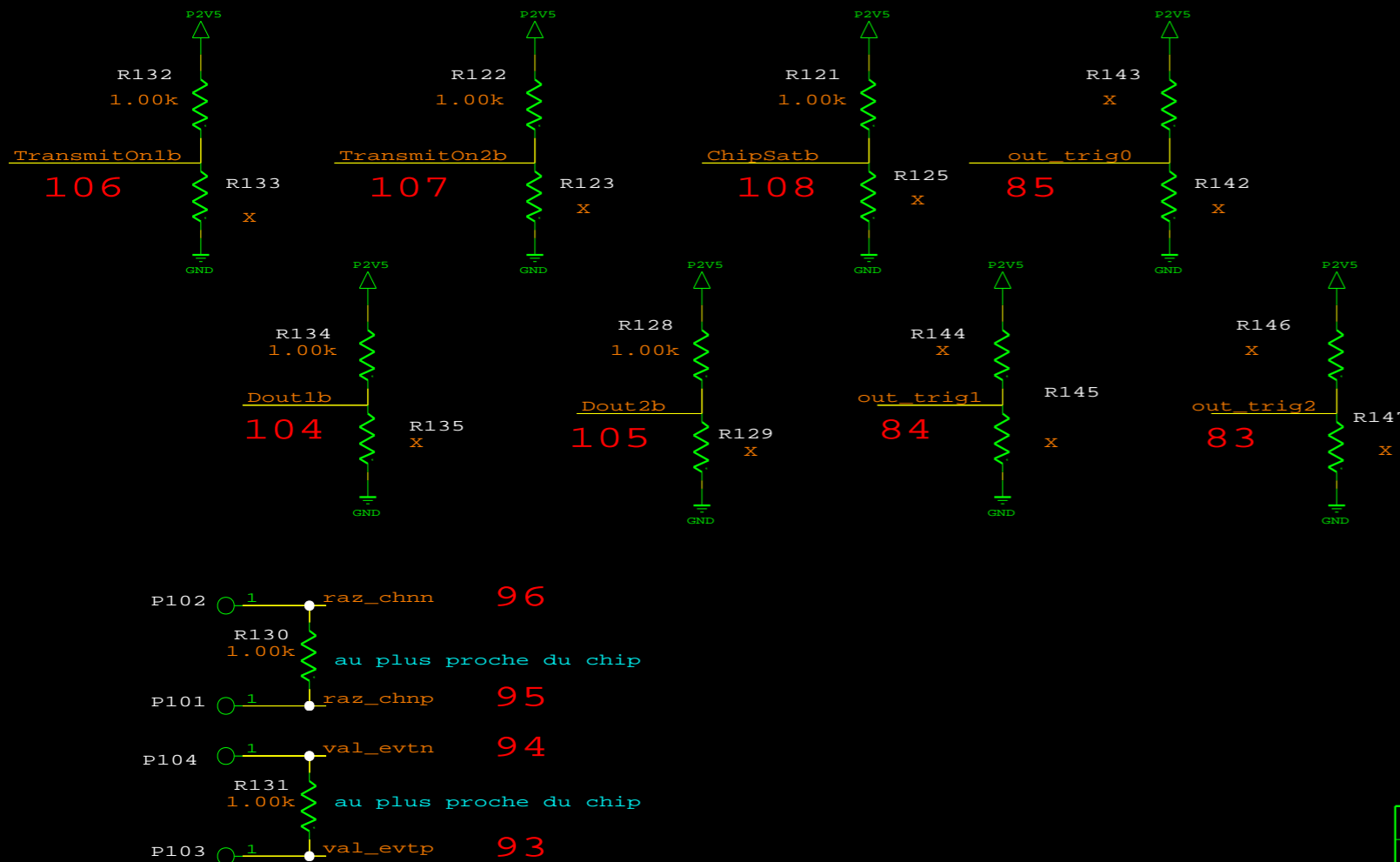
au plus proche de l'altera



external ADC



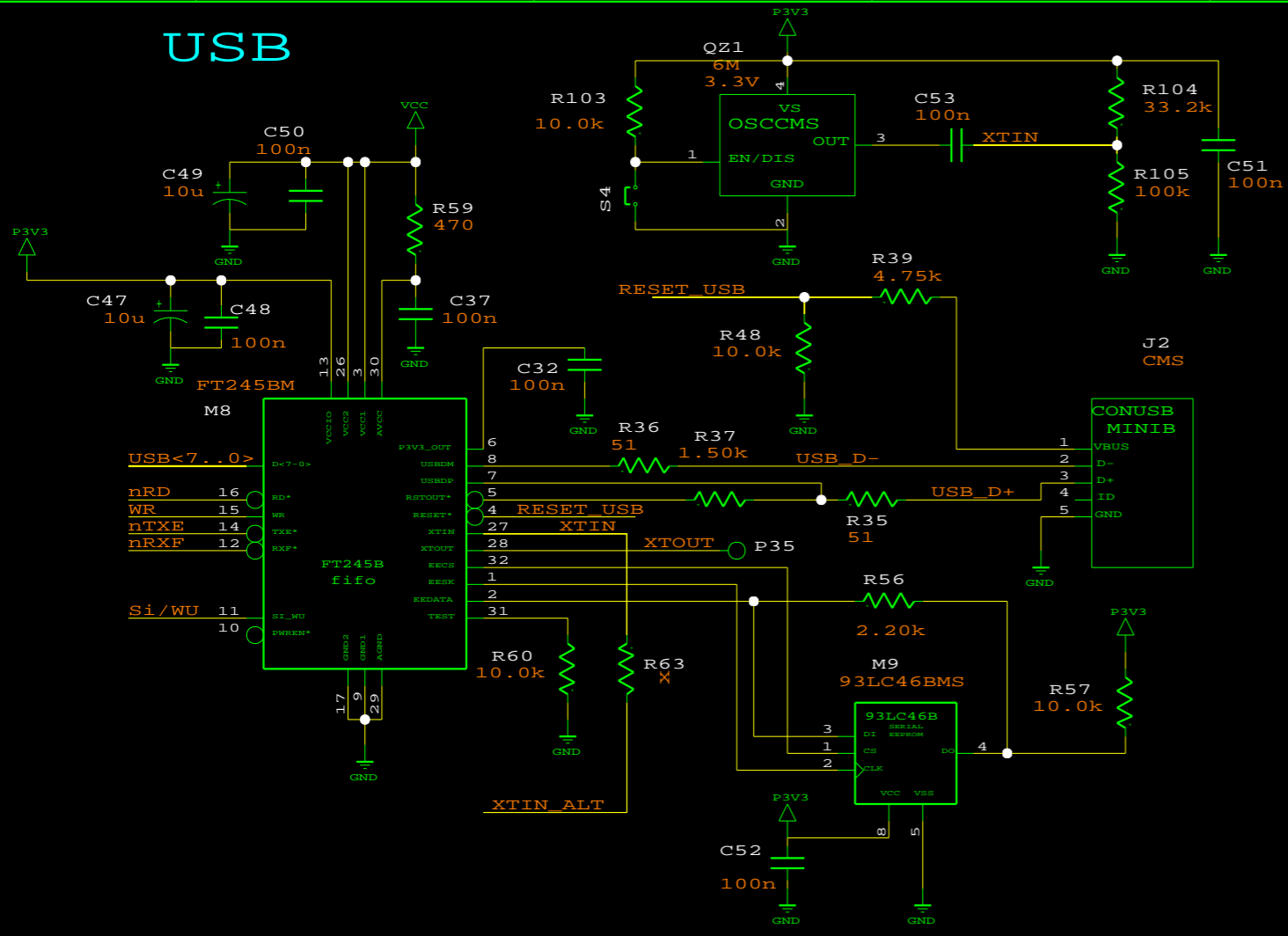
I/O ASIC



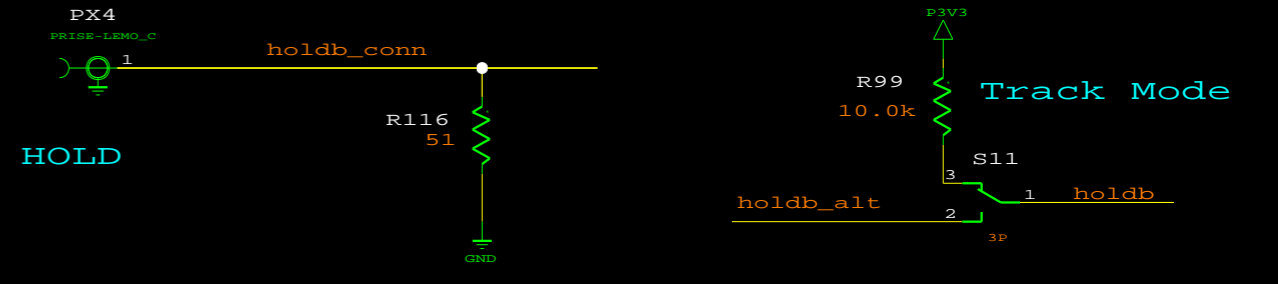
Pastilles pour connexions shapes

test_hardroc2c	MODIFIE: Thu May 6 10:30:52 2010
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	DESSIN:
LABORATOIRE DE L'ACCELERATEUR LINEAIRE	
CNRS IN2P3 U P S	

USB



---HOLD---



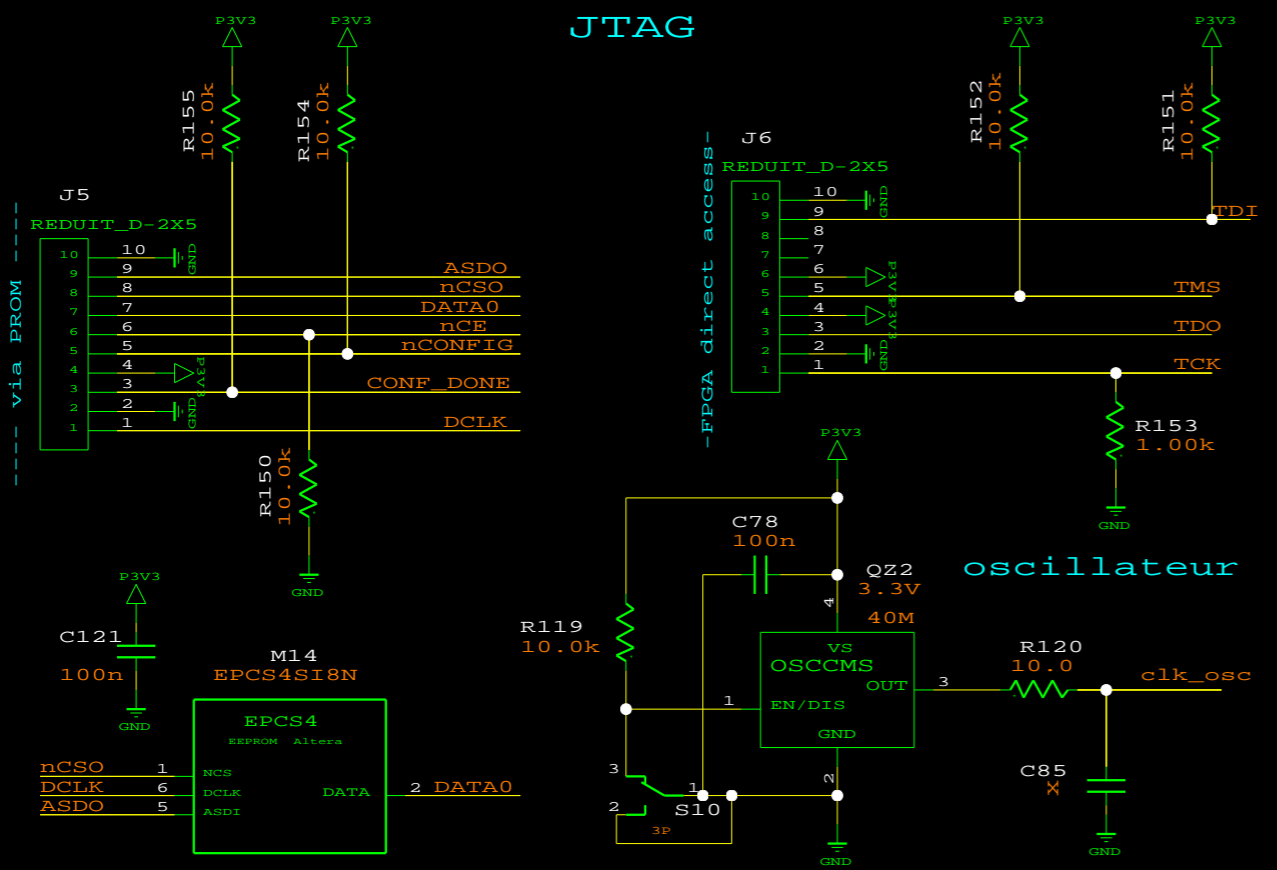
Digital ASIC

holdb	P96	63
trig_ext	P92	86
pwr_on_dac	P91	87
pwr_on_adc	P90	88
pwr_on_a	P89	89
pwr_on_d	P88	90
start_acq	P87	92
resethb	P86	102
Dout1b	P77	104
Dout2b	P75	105
TransmitOn1b	P74	106
TransmitOn2b	P72	107
ChipSarb	P71	108
rst_counterb	P69	109
start_readout1	P68	110
start_readout2	P66	111
end_readout1	P65	112
end_readout2	P65	113
select	P63	114
sr_rstb	P60	115
sr_ck	P59	116
sr_in	P57	117
sr_out	P56	118
out_trig2	P95	83
out_trig1	P94	84
out_trig0	P93	85

PINS TEST

test0	P122
test1	P105
test2	P123
test3	P106
test4	P124
test5	P107
test6	P125
test7	P108
test8	P126
test9	P109
test10	P127
test11	P110
test12	P128
test13	P111
test14	P129
test15	P112
test16	P120
test17	P113
test18	P121
test19	P114
test20	P85
test21	P83
test22	P81
test23	P76
test24	P73
test25	P70
test26	P67
test27	P64
test28	P61
test29	P58
test30	P55
test31	P49
test32	P49
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test35	P47
test36	P42
test37	P46
test38	P41
test39	P45
test40	P40

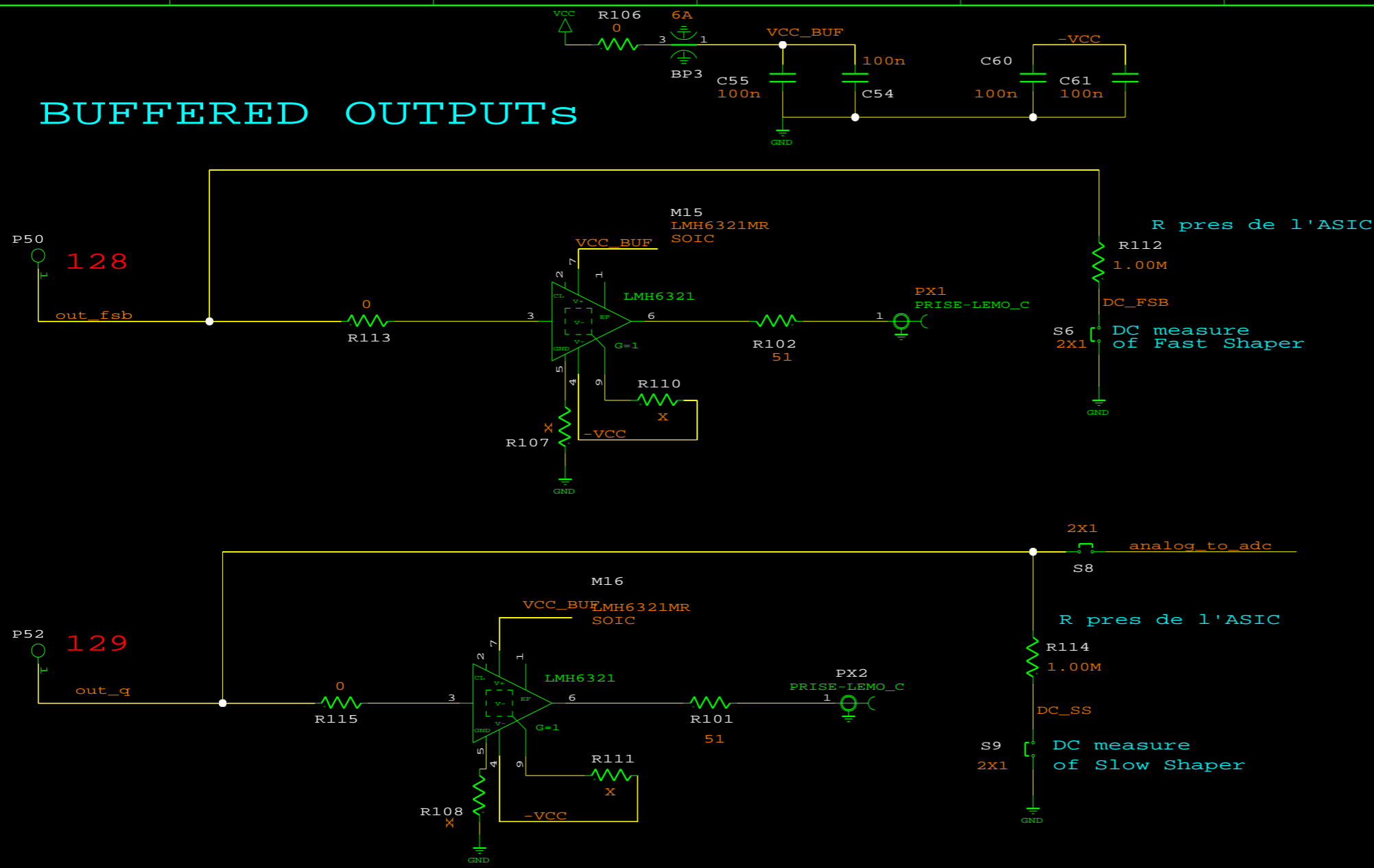
JTAG



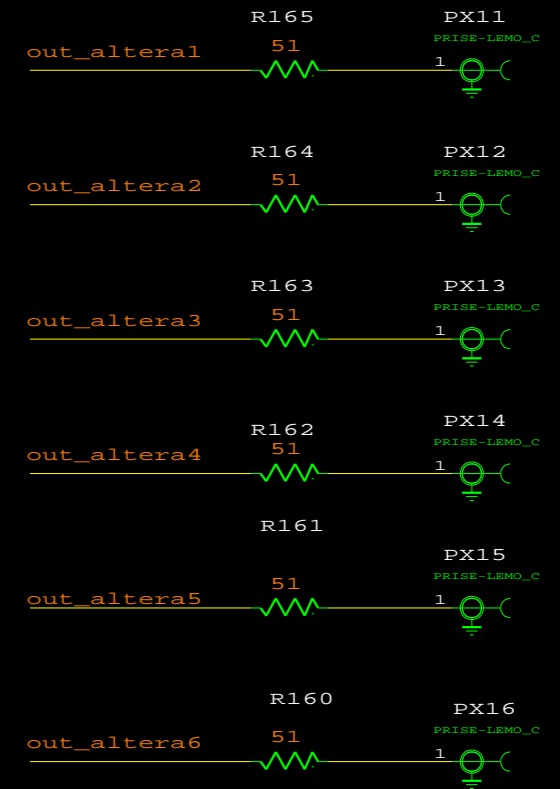
oscillateur

test_hardroc2c

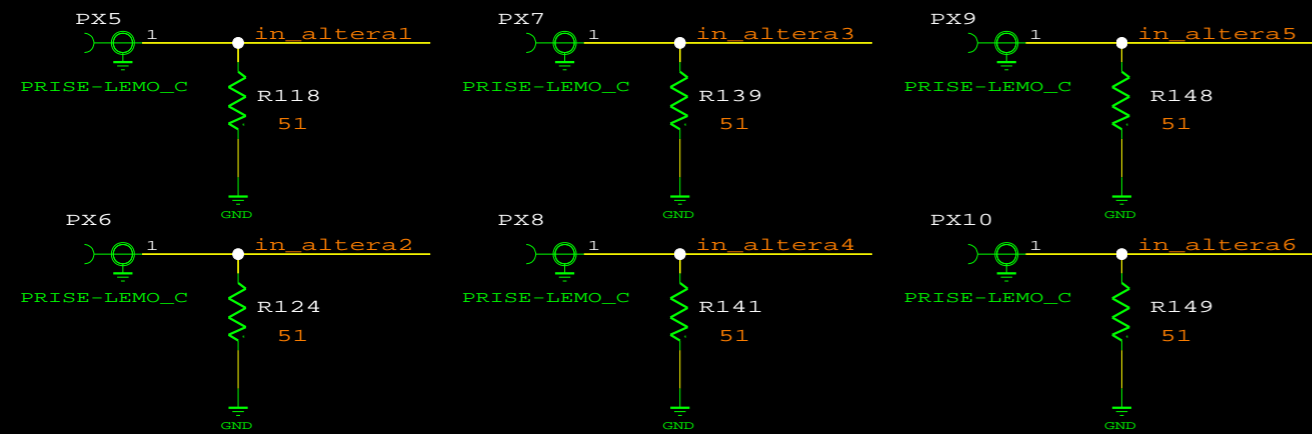
BUFFERED OUTPUTS



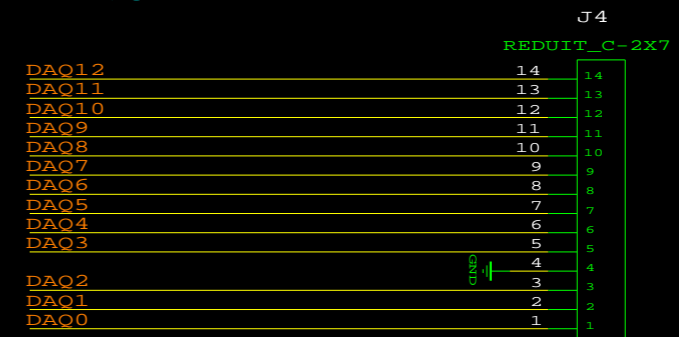
I/O from ALTERA



I/O to ALTERA



DAQ Connector

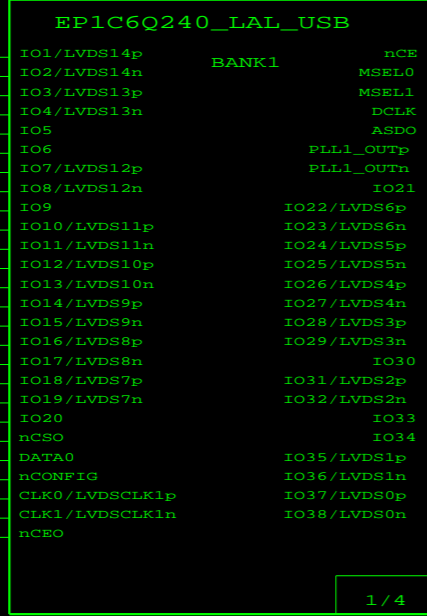


test_hardroc2c

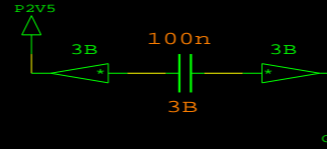
VCCINT=P1V5;VCCIO4=P2V5;VCCIO1=P3V3;VCCIO2=P3V3;VCCIO3=P3V3(pwr)

EP1C6Q240C6
PQFP

M13

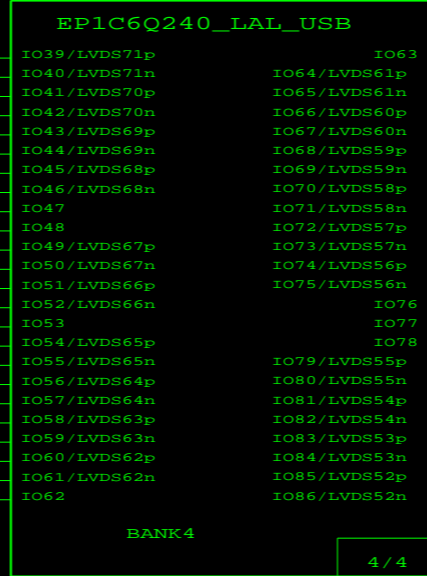


PLL_OUT
P84



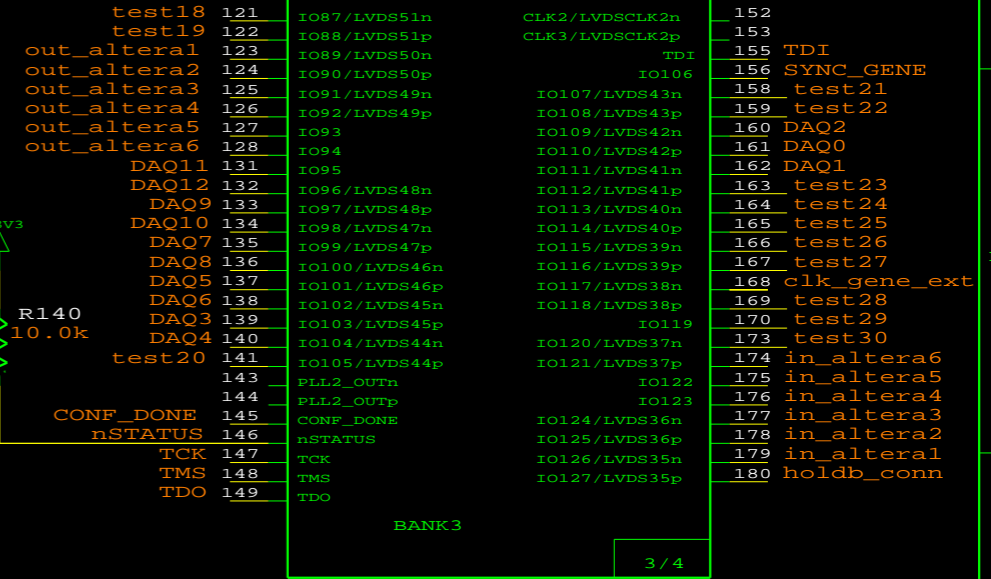
EP1C6Q240C6
PQFP

M13



CONF_DONE
nSTATUS

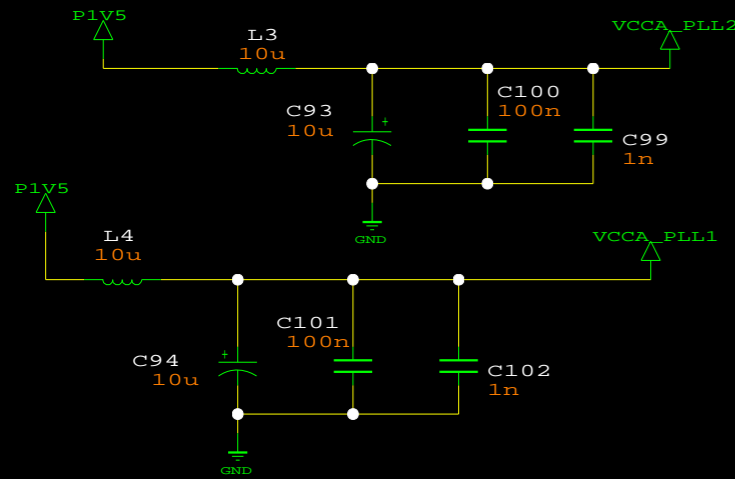
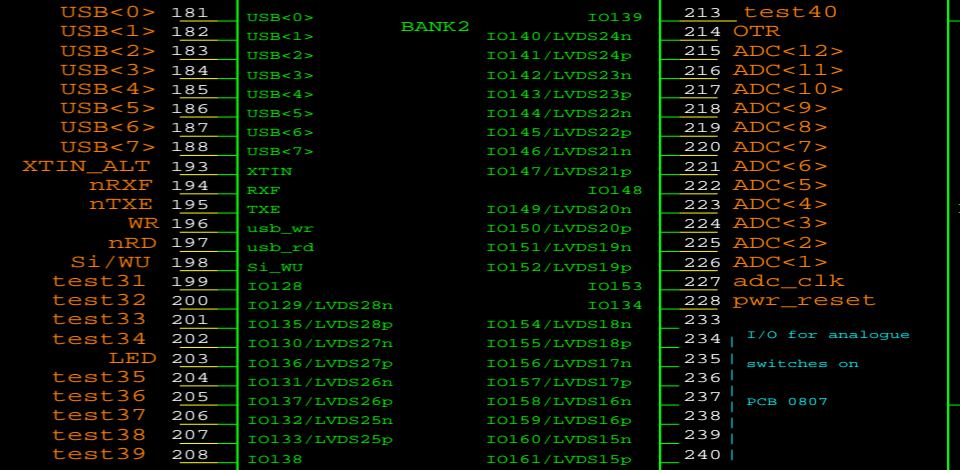
EP1C6Q240_LAL_USB



EP1C6Q240C6
PQFP

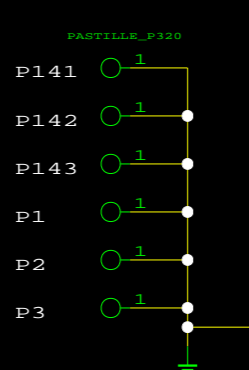
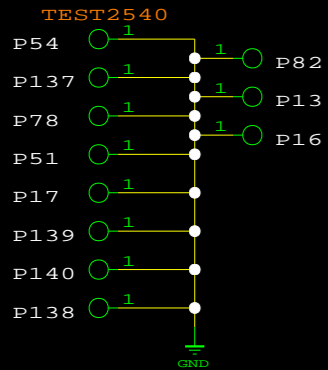
M13

EP1C6Q240_LAL_USB



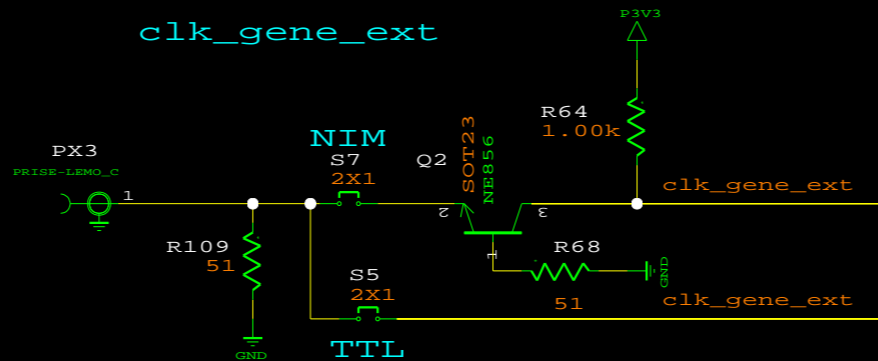
GROUND TEST POINTS

PASTILLES MECANIKES



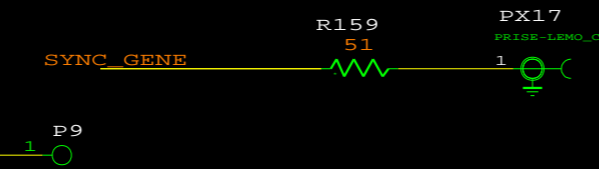
entrees cote altera

clk_gene_ext

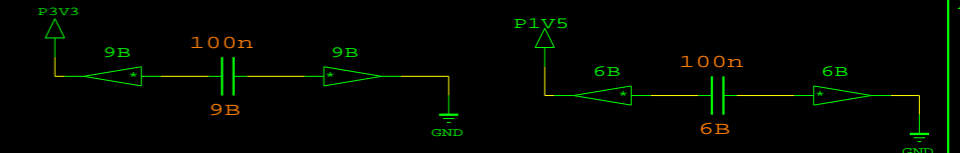


sorties cote altera

SYNC_gene



GROUND HOLE
Sans VE !



test_hardroc2c