**LIROC2
TSMC 013G
V 0.3**

Liroc is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for LIDAR application.

Liroc allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 5ns separated single photo-electrons). Liroc allows fast single photon counting over 300MHz per channel.

An adjustment of the SiPM high-voltage (gain) is possible using a channel-by-channel 6-bit DAC connected to the ASIC inputs. Channel-by-channel calibration on the trigger threshold is also possible thanks to 7-bit DACs. Liroc can be calibrated using the dark noise of the SiPM.

Liroc features a GHz measurement line composed of an RF preamplifier with pole zero cancellation followed by a fast discriminator and low swing LVDS fast driver.

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron
	Better than 3ns double-peak separation on single photo-electron
	Over 300MHz photon counting rate
Dynamic Range	Over 100 photo-electrons
Packaging & Dimension	BGA 20x20 mm^2
	Flip-Chip low inductance packaging technology
Power Consumption	210mW (TBC) – Supply voltage: 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 LVDS triggers
Internal Programmable Features (I^{2}C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7-bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp pole-zero cancellation adjustment, individual trigger masking.

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Maximum ratings

Ref.	Name	Description, comments or Ballout	Min.	Typ.	Max.	Unit
001	Operating Temperature	Asic operating temperature	-40	25	120	C
002	Power Supply	VDD, VDDI, DVDD	1.08	1.2	1.32	V
003	Ground	GND	0	0	0	V
004	Analog Inputs	IN<0:63>	0	-	1.5	V
005	Digital Inputs (Single ended)	POWER_ON, SDA, CLK_SM_I2C, SCL, RSTB_I2C, RSTB_SC, RSTB_PROBE, CLK_PROBE, SRIN_PROBE, CHIP_ID<0:3>	0	-	1.5	V
006	Digital Inputs (Differential - Common Model)	VALEVENT_N/P	520	580	640	mV
007	Digital Inputs (Differential - Swing)	VALEVENT_N/P	300	410	410	mV
008	Digital Outputs (Single Ended)	ERROR_SC, SDA, SCL, SROUT_PROBE,NOR54	1.08	1.2	1.32	V
009	Digital Outputs (Differential - Common Model)	TRIG<0:63>_n/p	520	580	640	mV
010	Digital Outputs (Differential - Swing)	TRIG<0:63>_n/p	300	410	410	mV

Table 1 – Maximum ratings

ASIC Architecture

LIROC is a 64-channel fully analog ASIC for reading out SiPM and providing fast trigger outputs. Main features of this ASIC include: individual input DAC for trimming SiPM overvoltage for detector gain correction, high bandwidth pre-amp, fast discriminator with channel-by-channel threshold trimming and differential buffer for trigger outputs. This ASIC is capable of producing low-jitter short trigger pulses which mean it is highly suitable for photon counting application or LIDAR application required sharp trigger edges.
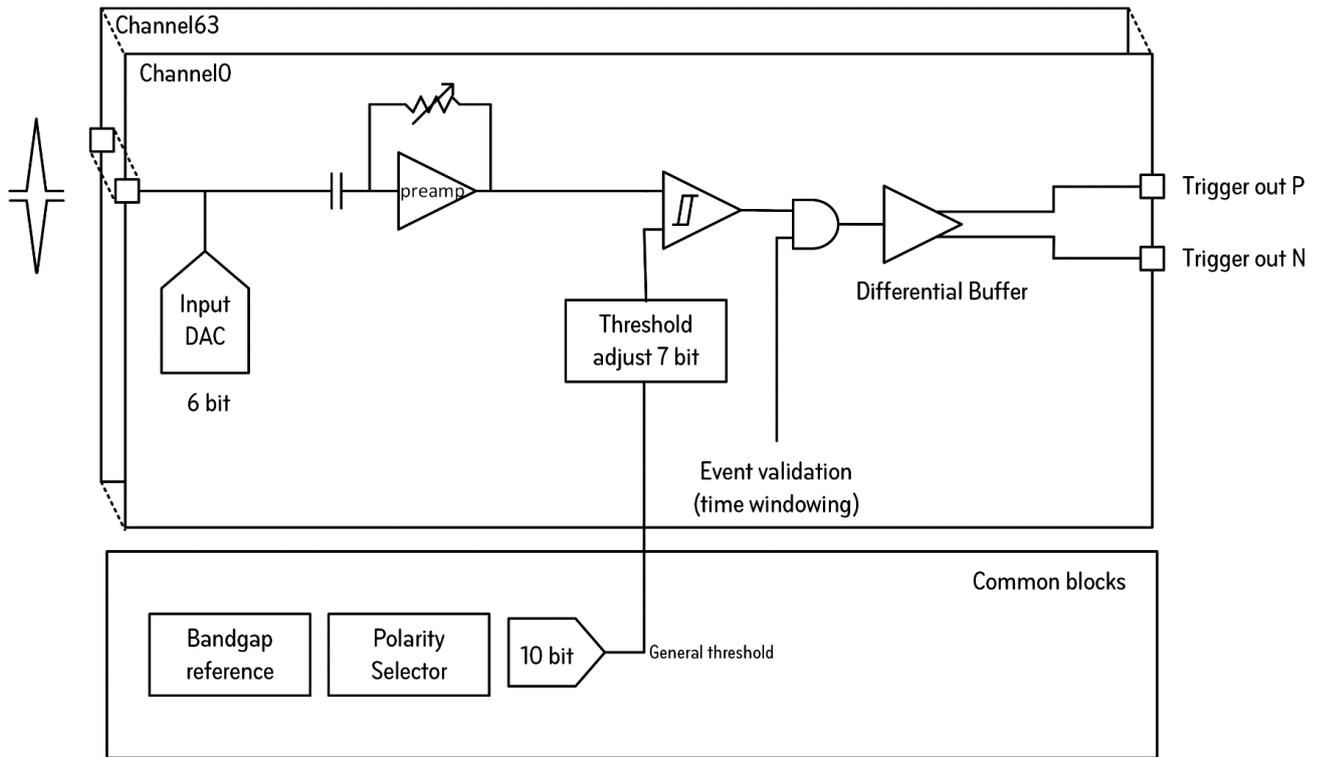
Figure 1 – ASIC block diagram

Block diagram of this ASIC is shown in Figure 1 and this ASIC is optimized for positive and negative polarity input signal. Additionally, users would be able to perform time windowing of the trigger output through an external signal, mask the trigger outputs individually and change the polarity of the trigger outputs if required.

Power consumption & DC levels

Following DC levels are observed at the references and biasing point of LIROC:

Signal name	Nominal SIM (mV)
ib_7b	278
icasc_pa	906
ibo_pa	581
ibd_pa	342
ibi_pa	376
vdac_pa	332
ibo_discri	580
ibm2_discri	871
ibm1_discri	872
ibi_discri	342
I_offset_disc	368
Vcasc_Discri	999
Ibi_P	818
Ibi_N	335
Vth	498
ibo_Bg	706
ibi_Bg	840
Vbg	318

Table 2 – DC points

Power consumption of static power (amplifier biasing) is 115mA over 1.2V thus 135mW for the full chip at room temperature. That power consumption does not include output buffer toggling in operation.

I^{2}C configuration

This ASIC can be configured using I^{2}C interface. The I^{2}C slave core can be programmed using a custom I^{2}C protocol that does not follow the IEEE standard. The I^{2}C slave core has been designed with SEU mitigations in place.

Features of this IP are the following:

- Triplicated Design
- 2048 addresses for the channel numbers
- 32 addresses for the register numbers
- 15 Chip ID numbers

The I^{2}C slave core must receive a clock through the clk_sm_i2c port. This clock must have a frequency 20 times higher than the clock sent by the I^{2}C master on the SCL line. These clocks must be synchronous.

Figure 2 and Table 3 describe the I^{2}C slave core structure in the ASIC and the registers content.

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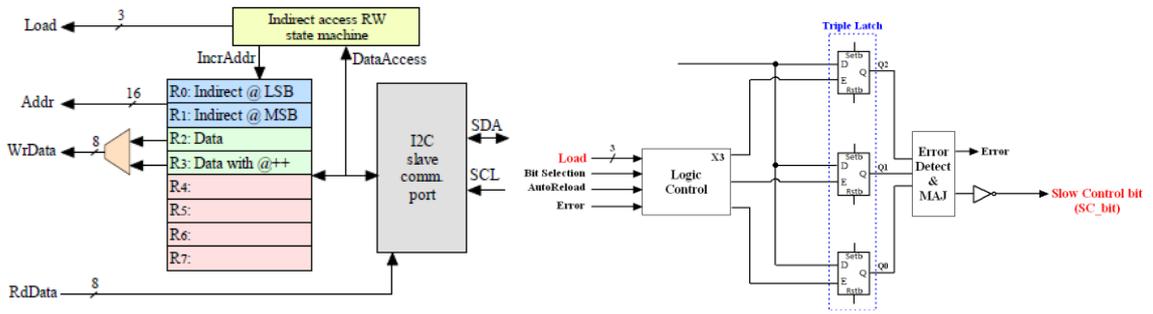
Figure 2 – Left: I2C slave core registers. Right: Slow Control bit cell design

I2C Address	Register
0	ASIC parameter address (LSB): Channel
1	ASIC parameter address (MSB): Register
2	Data Read/to Write
3	Data with auto-incremental Address
4-5-6	TBD
7	Status register (error, parity)

Table 3 – I2C slave core register descriptions

To address the Slow control parameters, the user can read or write each sub-address directly or it can use the auto increment feature that increments the sub-address based on the previous sub-address.

Figure 3 describes simple read and write I2C procedures. Such transfer is performed by sending 3 I2C frames of 16 bits as described in Figure 3. The full address to be sent is composed of the address and the sub-address of the slow control register, as described in Figure 4. The slow control registers associated addresses and sub-addresses can be found in Table 4.

Figure 5 shows a screenshot of an I^2C write procedure to the slow control register with address 31 and sub-address 1.

Figure 3 – Slow Control simple or direct parameter sub-addressing procedure

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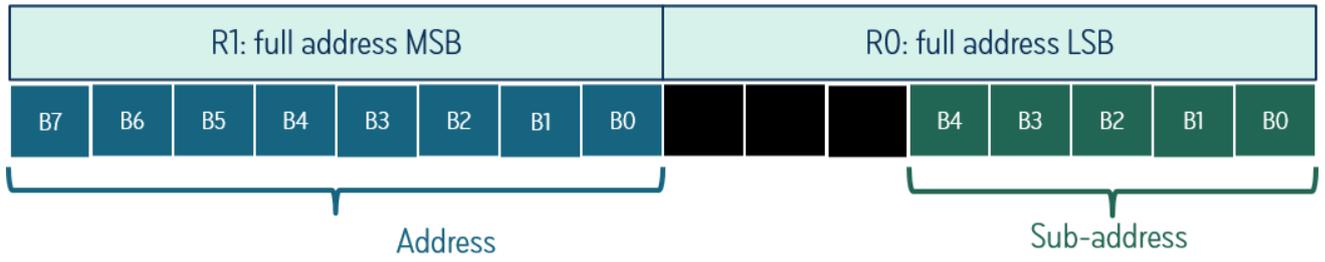
Figure 4 - Address and Sub-Address of the I^{2}C register for setting the Slow Control of Lirocv0
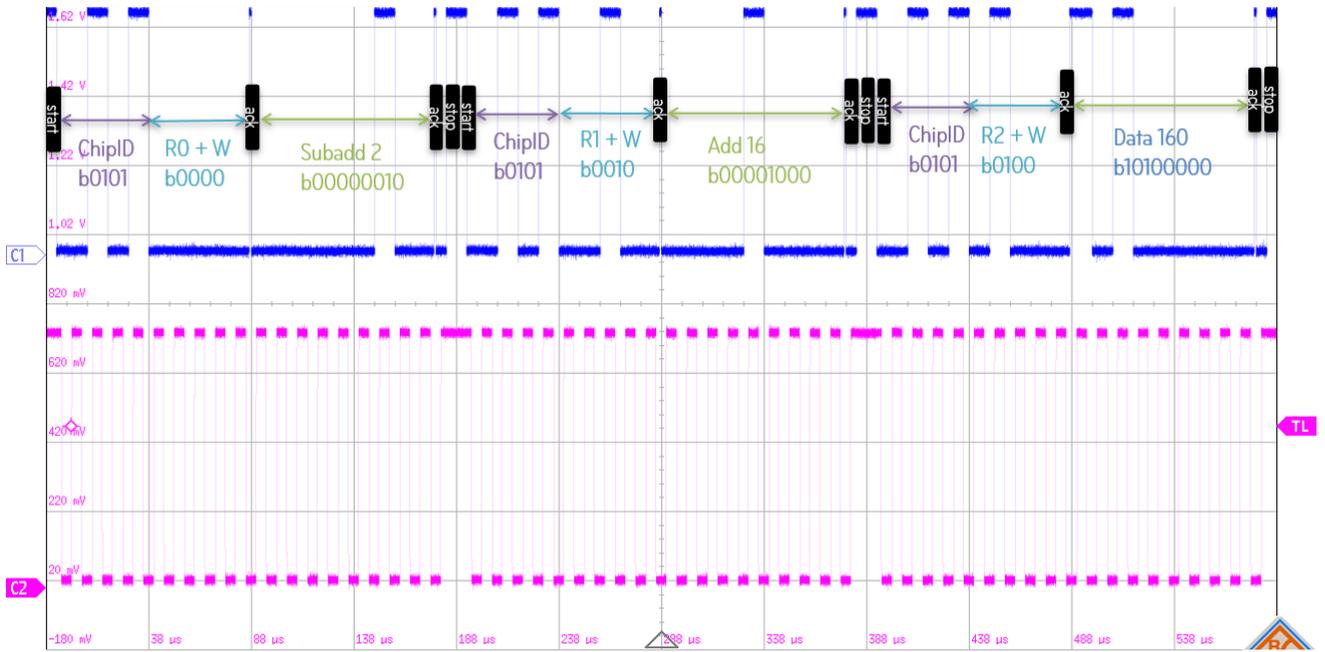
Figure 5 – SDA and SCL signals during an I^{2}C write procedure of value 90 to address 3 sub-address 1

Slow Control parameters available for this ASIC are listed in the Table 1. "NC" term denotes non used Slow Control bits. Data in "Address" and "Subadd" columns (Table 4) denote the sub address in R1 & R0 writing sequences. The "Address" section takes 8-bit of addressing, which includes the whole 8-bit of R1. The "Sub-address" section will be the lowest 5-bit of R0 (Figure 4) and the remaining 3-bit of R0 are not used. Data payload in R2 (direct parameter addressing - Figure 3) or R3 will be based on data in "Parameters/Default value" column.

| Address	Subadd	Bit#	Default value	Name	Description
0-63	0	7-2	000000	DC_PA[5:0]	Channel-by-channel input DC level setting
		1	0	Ctest	Injection capacitance connection switch. Default is switch open (0)
		0	0	NC	Not connected
	1	7	0	Mask	Mask Trigger. Default is not masked (0)
		6-0	1000000	DAC_local[6:0]	Channel-by-channel 7-bit threshold adjustment
64	0	7	1	EN_pa	Enable of Pre-Amp. Default is enabled (1)
		6	0	PP_pa	Power pulsing of Pre-Amp. Default is not Power Pulsed (0)
		5-2	1010	PA_gain[3:0]	Pre-Amp pole zero cancellation adjustment
		1-0	00	NC	Not connected
	1	7	1	EN_7b	Enable of 7-bit channel-by-channel threshold. Default is enabled (1)
		6	0	PP_7b	Power pulsing of 7-bit channel-by-channel threshold. Default is not Power Pulsed (0)
		5-4	00	NC	Not connected
		3-0	0010	PA_comp<3:0>	Pre-amp biasing baseline compensation.
	2	7	1	EN_disc	Enable of discriminator. Default is enabled (1)
		6	0	PP_disc	Power pulsing of discriminator. Default is not Power Pulsed (0)
		5	1	Polarity	Discriminator polarity selection. Default is (1) : negative trigger out polarity for negative input charge.
		4	0	Cmd_hysteresis	Discriminator hysteresis.
		3-0	0000	NC	Not connected
65	0	7	1	EN_bg	Enable of bandgap. Default is enabled (1)
		6	0	PP_bg	Power Pulsing of bandgap. Default is not Power Pulsed (0)
		5-0	0	NC	Not connected
	1	7	1	EN_10bDAC	Enable of 10b threshold DAC. Default

Address	Subadd	Bits	Default	Name	Description
					is enabled (1)
		6	0	PP_10bDAC	Power Pulsing of 10b threshold DAC. Default is not Power Pulsed (0)
		5-2	0000	NC	Not connected
		1-0	01	dac_threshold<9:8>	MSB DAC values. Default is 01.
	2	7-0	11011000	dac_threshold<7:0>	LSB DAC value. Default is 11011000.
66	0	7-4	0100	EN-CLPS<0:3>	CLPS buffer size trimming. Default value is 0100
		3-0	0000	EN-pE<0:3>	CLPS pre-emphasis trimming. Default is 0000.
	1	7-6	00	pE-delay<0:1>	CLPS pre-emphasis delay trimming. Default is 00
		5-0	000000	NC	Not connected
	2	7	1	EN_Rx	Enable LVDS of receiver for ValEvt. Default is enabled (1)
		6	0	PP_Rx	Power pulsing of LVDS receiver for ValEvt. Default is not Power Pulsed (0)
		5	1	Forced_ValEvt	Internal ValEvt. Bypass of external ValEvt is effective when EN_Rx = '0'.
		4-1	0000	NC	Not connected
		0	1	EN_NOR64	Enable Trigger NOR64 output. Default is enabled (1)
67	0	7	1	EN_probe	Enable of analogue probe. Default is enabled (1)
		6	0	PP_probe	Power pulsing of analogue probe. Default is not Power Pulsed (0)
		5-3	000	NC	Not connected
		2-0	100	MillerComp <2:0>	Probe amplifier compensation capacitance trimming. Default is 100. Range : 0 ~ 700fF. Step : 100fF. Default : 400fF
	1	7-6	10	Ibi_probe <1:0>	Input bias of probe amplifier. Default is 10 "00" - 20uA "01" – 30uA "10" – 40uA "11" – 80uA
		5-0	100000	Ibo_probe <5:0>	Output bias of probe amplifier. Default is 100000. Range : 0 ~ 38uA. Step : 0.6uA. Default : 20uA

Table 4 - Slow Control list

Specifically, for "Address" 0-63, each "Subadd" in this section will correspond only to the selected channel. This means that, in order to have all channels wide operation, each Address will have to be selected when writing the Slow Control operation. Otherwise, all the other Address (64-67) operations will be effective for the whole ASIC.

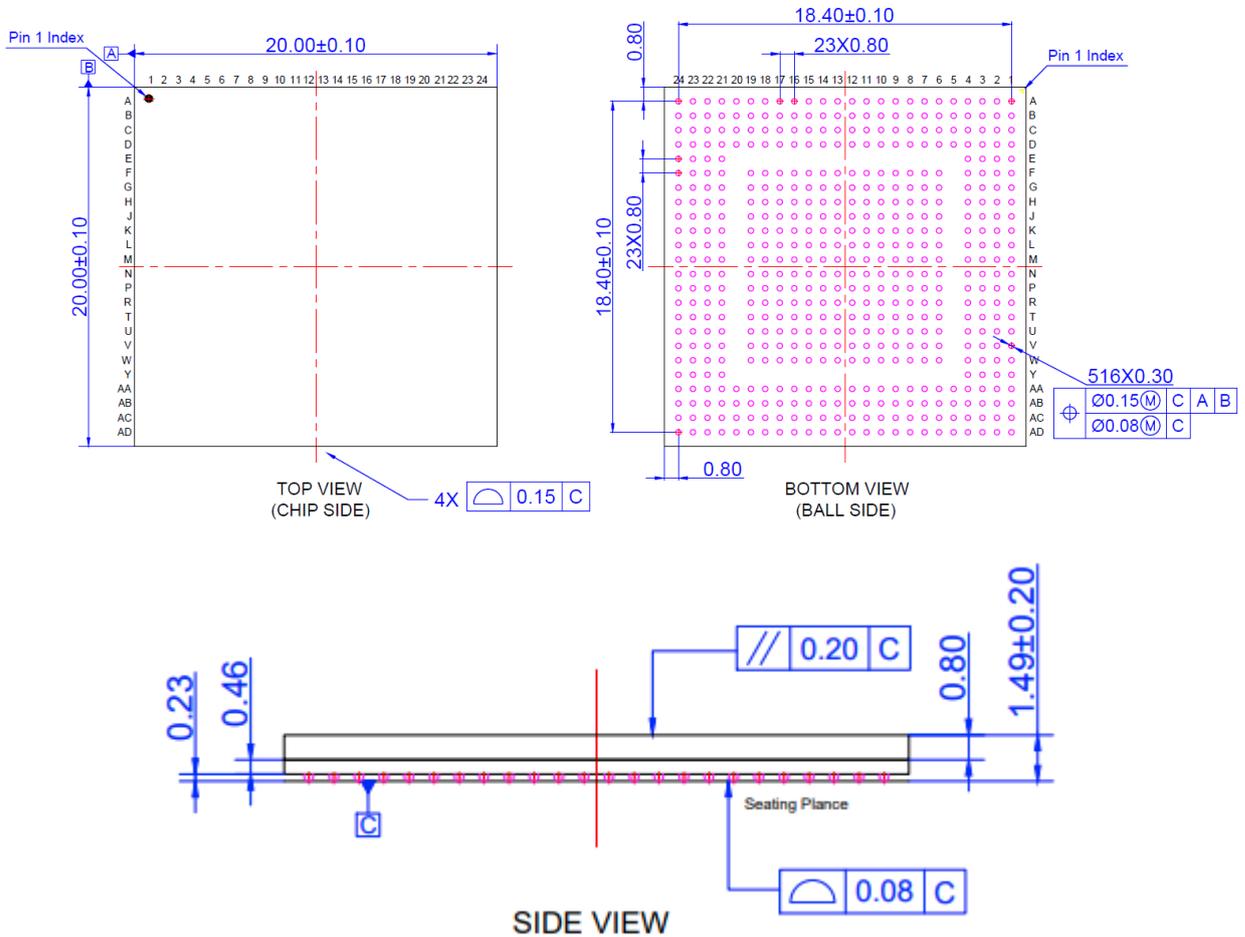## Pinout, Power supplies & mechanics

Mechanics

Figure 6 – BGA packaging mechanical outline
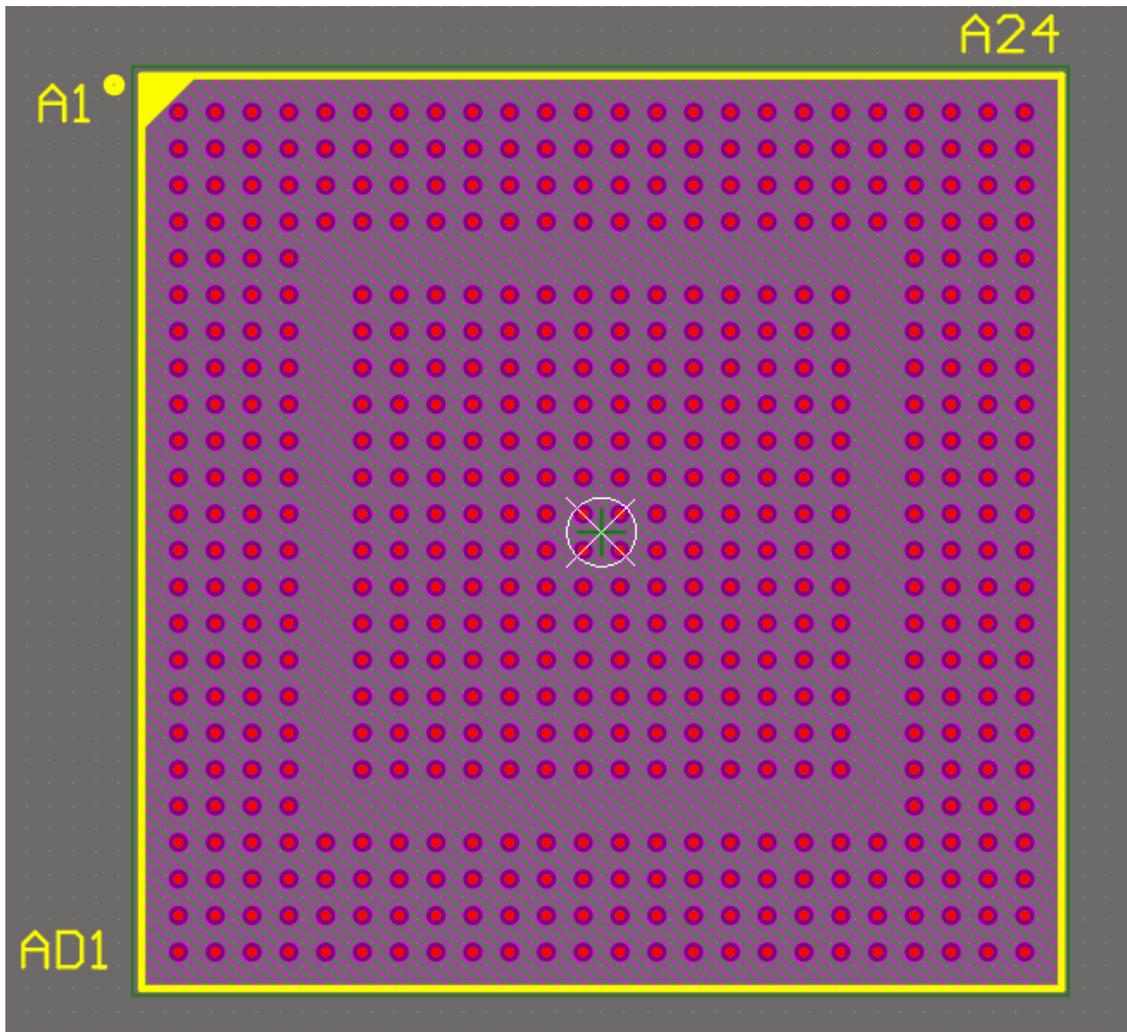
Altium Footprint

Figure 7 – Altium footprint

The footprint of the ASIC package is available for board design under Altium. The ballout follows the configuration in Figure 8 and Figure 9.

BGA package Ball-out

	1	2	3	4	5	6	7	8	9	10	11	12
A	IN<53>	IN<55>	IN<57>	IN<59>	IN<61>	IN<63>	IN<62>	POWER_ON	SDA	CLK_SM_I2C	VALEVENT_N	VALEVENT_P
B	IN<51>	IN<52>	IN<54>	IN<56>	IN<58>	IN<60>	IBO_DISC	IBO_PA	RESETB_SC	SCL	VCASC_RX	GND
C	IN<49>	IN<50>	IBI_DISC	NC	NC	NC	NC	NC	NC	NC	NC	GND
D	IN<47>	IN<48>	IBO_PROBE	NC	NC	NC	NC	NC	NC	NC	NC	GND
E	IN<45>	IN<46>	IBM1_DISC	NC								
F	IN<43>	IN<44>	I_OFFSET_DISC	NC		P2V5	P2V5	P2V5	VDD	VDD	VDD	GND
G	IN<41>	IN<42>	VCASC_DISC	NC		P2V5	P2V5	P2V5	VDD	VDD	VDD	GND
H	IN<39>	IN<40>	IBO_OTA_10BDAC	NC		VDD	VDD	NC	GND	GND	GND	GND
J	IN<37>	IN<38>	IBI_OTA_10BDAC	NC		VDD	VDD	NC	GND	GND	GND	GND
K	IN<35>	IN<36>	VREF_10BDAC	NC		VDD	VDD	NC	GND	GND	GND	GND
L	IN<33>	IN<34>	VSLOPE_10BDAC	NC		P2V5	P2V5	NC	GND	GND	GND	GND
M	ANALOG_PROBE2	IN<32>	VTH	NC		P2V5	P2V5	NC	GND	GND	GND	GND
N	ANALOG_PROBE1	IN<30>	VBG_1V	NC		P2V5	P2V5	NC	GND	GND	GND	GND
P	IN<31>	IN<28>	VBG	NC		P2V5	P2V5	NC	GND	GND	GND	GND
R	IN<29>	IN<26>	IBO_BG	NC		VDD	VDD	NC	GND	GND	GND	GND
T	IN<27>	IN<24>	IBI_BG	NC		VDD	VDD	NC	GND	GND	GND	GND
U	IN<25>	IN<22>	VCP_PROBE	NC		VDD	VDD	NC	GND	GND	GND	GND
V	IN<23>	IN<20>	VCN_PROBE	NC		P2V5	P2V5	P2V5	VDD	VDD	VDD	GND
W	IN<21>	IN<18>	IBI_P_PROBE	NC		P2V5	P2V5	P2V5	VDD	VDD	VDD	GND
Y	IN<19>	IN<16>	IBI_N_PROBE	NC								
AA	IN<17>	IN<14>	IBI_PA	NC	NC	NC	NC	NC	NC	NC	NC	GND
AB	IN<15>	IN<12>	VDAC_PA	NC	NC	NC	NC	NC	NC	NC	NC	GND
AC	IN<13>	IN<10>	IN<8>	IN<6>	IN<4>	IN<2>	ICASC_PA	IBD_PA	NC	NC	NC	GND
AD	IN<11>	IN<9>	IN<7>	IN<5>	IN<3>	IN<1>	IN<0>	IB_7B	IN_CTEST	IBM2_DISC	SROUT_PROBE	SRIN_PROBE
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 8 – LIROC Ball-out west part

12	13	14	15	16	17	18	19	20	21	22	23	24	
VALEVENT_P	RSTB_IC	NOR64	TRIG_P<62>	TRIG_N<62>	TRIG_P<63>	TRIG_N<63>	TRIG_P<61>	TRIG_N<61>	TRIG_P<52>	TRIG_N<52>	TRIG_P<53>	TRIG_N<53>	A
GND	NC	NC	TRIG_P<60>	TRIG_N<60>	TRIG_P<56>	TRIG_N<56>	TRIG_P<59>	TRIG_N<59>	TRIG_P<50>	TRIG_N<50>	TRIG_P<51>	TRIG_N<51>	B
GND	NC	NC	TRIG_P<58>	TRIG_N<58>	TRIG_P<54>	TRIG_N<54>	TRIG_P<57>	TRIG_N<57>	TRIG_P<48>	TRIG_N<48>	TRIG_P<49>	TRIG_N<49>	C
GND	NC	NC	NC	NC	NC	NC	TRIG_P<55>	TRIG_N<55>	TRIG_P<46>	TRIG_N<46>	TRIG_P<47>	TRIG_N<47>	D
									TRIG_P<44>	TRIG_N<44>	TRIG_P<45>	TRIG_N<45>	E
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TRIG_P<42>	TRIG_N<42>	TRIG_P<43>	TRIG_N<43>	F
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TRIG_P<40>	TRIG_N<40>	TRIG_P<41>	TRIG_N<41>	G
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<38>	TRIG_N<38>	TRIG_P<39>	TRIG_N<39>	H
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<36>	TRIG_N<36>	TRIG_P<37>	TRIG_N<37>	J
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<34>	TRIG_N<34>	TRIG_P<35>	TRIG_N<35>	K
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<32>	TRIG_N<32>	TRIG_P<33>	TRIG_N<33>	L
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	CHIP_ID<0>	errorb_sc	M
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	CHIP_ID<3>	CHIP_ID<2>	CHIP_ID<1>	N
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<30>	TRIG_N<30>	TRIG_P<31>	TRIG_N<31>	P
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<28>	TRIG_N<28>	TRIG_P<29>	TRIG_N<29>	R
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<26>	TRIG_N<26>	TRIG_P<27>	TRIG_N<27>	T
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TRIG_P<24>	TRIG_N<24>	TRIG_P<25>	TRIG_N<25>	U
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TRIG_P<22>	TRIG_N<22>	TRIG_P<23>	TRIG_N<23>	V
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TRIG_P<20>	TRIG_N<20>	TRIG_P<21>	TRIG_N<21>	W
									TRIG_P<18>	TRIG_N<18>	TRIG_P<19>	TRIG_N<19>	Y
GND	NC	NC	NC	NC	NC	NC	TRIG_P<9>	TRIG_N<9>	TRIG_P<16>	TRIG_N<16>	TRIG_P<17>	TRIG_N<17>	AA
GND	NC	NC	TRIG_P<4>	TRIG_N<4>	TRIG_P<8>	TRIG_N<8>	TRIG_P<7>	TRIG_N<7>	TRIG_P<14>	TRIG_N<14>	TRIG_P<15>	TRIG_N<15>	AB
GND	NC	NC	TRIG_P<2>	TRIG_N<2>	TRIG_P<6>	TRIG_N<6>	TRIG_P<5>	TRIG_N<5>	TRIG_P<12>	TRIG_N<12>	TRIG_P<13>	TRIG_N<13>	AC
SRIN_PROBE	RSTB_PROBE	CLK_PROBE	TRIG_P<0>	TRIG_N<0>	TRIG_P<1>	TRIG_N<1>	TRIG_P<3>	TRIG_N<3>	TRIG_P<10>	TRIG_N<10>	TRIG_P<11>	TRIG_N<11>	AD
12	13	14	15	16	17	18	19	20	21	22	23	24	

Figure 9 - LIROC ball-out East part

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LIROC pinout

Net Name	BGA Ball	Type
ANALOG_PROBE1	N1	Bias
ANALOG_PROBE2	M1	
CHIP_ID<0>	M23	I/O Digital Single Ended
CHIP_ID<1>	N24	
CHIP_ID<2>	N23	
CHIP_ID<3>	N22	
CLK_PROBE	AD14	
CLK_SM_I2C	A10	
DVDD	F13	Power Supply - DVDD
DVDD	F14	
DVDD	F15	
DVDD	F16	
DVDD	F17	
DVDD	F18	
DVDD	F19	
DVDD	G13	
DVDD	G14	
DVDD	G15	
DVDD	G16	
DVDD	G17	
DVDD	G18	
DVDD	G19	
DVDD	H18	
DVDD	H19	
DVDD	J18	
DVDD	J19	
DVDD	K18	
DVDD	K19	
DVDD	L18	
DVDD	L19	
DVDD	M18	
DVDD	M19	
DVDD	N18	
DVDD	N19	
DVDD	P18	
DVDD	P19	
DVDD	R18	
DVDD	R19	

Net Name	BGA Ball	Type
DVDD	T18	
DVDD	T19	
DVDD	U18	
DVDD	U19	
DVDD	V13	
DVDD	V14	
DVDD	V15	
DVDD	V16	
DVDD	V17	
DVDD	V18	
DVDD	V19	
DVDD	W13	
DVDD	W14	
DVDD	W15	
DVDD	W16	
DVDD	W17	
DVDD	W18	
DVDD	W19	
ERRORB_SC	M24	I/O Digital Single Ended
GND	AB12	Ground
GND	AC12	
GND	B12	
GND	C12	
GND	D12	
GND	F12	
GND	G12	
GND	H9	
GND	H10	
GND	H11	
GND	H12	
GND	H13	
GND	H14	
GND	H15	
GND	H16	
GND	H17	
GND	J9	
GND	J10	
GND	J11	
GND	J12	
GND	J13	
GND	J14	

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GND	J15		GND	P12	
GND	J16		GND	P13	
GND	J17		GND	P14	
GND	K9		GND	P15	
GND	K10		GND	P16	
GND	K11		GND	P17	
GND	K12		GND	R9	
GND	K13		GND	R10	
GND	K14		GND	R11	
GND	K15		GND	R12	
GND	K16		GND	R13	
GND	K17		GND	R14	
GND	L9		GND	R15	
GND	L10		GND	R16	
GND	L11		GND	R17	
GND	L12		GND	T9	
GND	L13		GND	T10	
GND	L14		GND	T11	
GND	L15		GND	T12	
GND	L16		GND	T13	
GND	L17		GND	T14	
GND	M9		GND	T15	
GND	M10		GND	T16	
GND	M11		GND	T17	
GND	M12		GND	U9	
GND	M13		GND	U10	
GND	M14		GND	U11	
GND	M15		GND	U12	
GND	M16		GND	U13	
GND	M17		GND	U14	
GND	N9		GND	U15	
GND	N10		GND	U16	
GND	N11		GND	U17	
GND	N12		GND	V12	
GND	N13		GND	W12	
GND	N14		GND	AA12	
GND	N15		IBD_PA	AC8	
GND	N16		IBI_BG	T3	
GND	N17		IBI_DISC	C3	Bias
GND	P9		IBI_N_PROBE	Y3	
GND	P10		IBI_OTA_10BD AC	J3	
GND	P11				

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IBI_PA	AA3	
IBI_P_PROBE	W3	
IBM1_DISC	A13	
IBM2_DISC	E3	
IBO_BG	AD10	
IBO_DISC	R3	
IBO_OTA_10B DAC	B7	
IBO_PA	H3	
IBO_PROBE	B8	
IB_7B	D3	
ICASC_PA	A14	
IN<0>	AD8	
IN<1>	AC7	
IN<2>	AD7	
IN<3>	AD6	
IN<4>	AC6	
IN<5>	AD5	
IN<6>	AC5	
IN<7>	AD4	
IN<8>	AC4	
IN<9>	AD3	
IN<10>	AC3	
IN<11>	AD2	
IN<12>	AC2	
IN<13>	AD1	
IN<14>	AB2	Analog Input
IN<15>	AC1	
IN<16>	AA2	
IN<17>	AB1	
IN<18>	Y2	
IN<19>	AA1	
IN<20>	W2	
IN<21>	Y1	
IN<22>	V2	
IN<23>	W1	
IN<24>	U2	
IN<25>	V1	
IN<26>	T2	
IN<27>	U1	
IN<28>	R2	
IN<29>	T1	

IN<30>	P2	
IN<31>	R1	
IN<32>	N2	
IN<33>	P1	
IN<34>	M2	
IN<35>	L1	
IN<36>	L2	
IN<37>	K1	
IN<38>	K2	
IN<39>	J1	
IN<40>	J2	
IN<41>	H1	
IN<42>	H2	
IN<43>	G1	
IN<44>	G2	
IN<45>	F1	
IN<46>	F2	
IN<47>	E1	
IN<48>	E2	
IN<49>	D1	
IN<50>	D2	
IN<51>	C1	
IN<52>	C2	
IN<53>	B1	
IN<54>	B2	
IN<55>	A1	
IN<56>	B3	
IN<57>	A2	
IN<58>	B4	
IN<59>	A3	
IN<60>	B5	
IN<61>	A4	
IN<62>	B6	
IN<63>	A5	
IN_CTEST	A7	
I_OFFSET_DISC	A6	Bias
P2V5	AD9	
P2V5	F3	
P2V5	F6	Power Supply - P2V5
P2V5	F7	
P2V5	F8	

Signal	Pin	Category
P2V5	G6	
P2V5	G7	
P2V5	G8	
P2V5	L6	
P2V5	L7	
P2V5	M6	
P2V5	M7	
P2V5	N6	
P2V5	N7	
P2V5	P6	
P2V5	P7	
P2V5	V6	
P2V5	V7	
P2V5	V8	
P2V5	W6	
POWER_ON	W7	
RESETB_SC	W8	
RSTB_I2C	A8	
NOR64	B9	
RSTB_PROBE	AD13	I/O Digital Single Ended
SCL	B10	
SDA	A9	
SRIN_PROBE	AD12	
SROUT_PROBE	AD11	
TRIG_N<0>	AD16	
TRIG_N<1>	AD18	
TRIG_N<2>	AC16	
TRIG_N<3>	AD20	
TRIG_N<4>	AB16	
TRIG_N<5>	AC20	
TRIG_N<6>	AC18	
TRIG_N<7>	AB20	
TRIG_N<8>	AB18	I/O Digital Differential (1GHz)
TRIG_N<9>	AA20	
TRIG_N<10>	AD22	
TRIG_N<11>	AD24	
TRIG_N<12>	AC22	
TRIG_N<13>	AC24	
TRIG_N<14>	AB22	
TRIG_N<15>	AB24	
TRIG_N<16>	AA22	
TRIG_N<17>	AA24	

Signal	Pin	Category
TRIG_N<18>	Y22	
TRIG_N<19>	Y24	
TRIG_N<20>	W22	
TRIG_N<21>	W24	
TRIG_N<22>	V22	
TRIG_N<23>	V24	
TRIG_N<24>	U22	
TRIG_N<25>	U24	
TRIG_N<26>	T22	
TRIG_N<27>	T24	
TRIG_N<28>	R22	
TRIG_N<29>	R24	
TRIG_N<30>	P22	
TRIG_N<31>	P24	
TRIG_N<32>	L22	
TRIG_N<33>	L24	
TRIG_N<34>	K22	
TRIG_N<35>	K24	
TRIG_N<36>	J22	
TRIG_N<37>	J24	
TRIG_N<38>	H22	
TRIG_N<39>	H24	
TRIG_N<40>	G22	
TRIG_N<41>	G24	
TRIG_N<42>	F22	
TRIG_N<43>	F24	
TRIG_N<44>	E22	
TRIG_N<45>	E24	
TRIG_N<46>	D22	
TRIG_N<47>	D24	
TRIG_N<48>	C22	
TRIG_N<49>	C24	
TRIG_N<50>	B22	
TRIG_N<51>	B24	
TRIG_N<52>	A22	
TRIG_N<53>	A24	
TRIG_N<54>	C18	
TRIG_N<55>	D20	
TRIG_N<56>	B18	
TRIG_N<57>	C20	
TRIG_N<58>	C16	
TRIG_N<59>	B20	

TRIG_N<60>	B16		TRIG_P<38>	H21	
TRIG_N<61>	A20		TRIG_P<39>	H23	
TRIG_N<62>	A16		TRIG_P<40>	G21	
TRIG_N<63>	A18		TRIG_P<41>	G23	
TRIG_P<0>	AD15		TRIG_P<42>	F21	
TRIG_P<1>	AD17		TRIG_P<43>	F23	
TRIG_P<2>	AC15		TRIG_P<44>	E21	
TRIG_P<3>	AD19		TRIG_P<45>	E23	
TRIG_P<4>	AB15		TRIG_P<46>	D21	
TRIG_P<5>	AC19		TRIG_P<47>	D23	
TRIG_P<6>	AC17		TRIG_P<48>	C21	
TRIG_P<7>	AB19		TRIG_P<49>	C23	
TRIG_P<8>	AB17		TRIG_P<50>	B21	
TRIG_P<9>	AA19		TRIG_P<51>	B23	
TRIG_P<10>	AD21		TRIG_P<52>	A21	
TRIG_P<11>	AD23		TRIG_P<53>	A23	
TRIG_P<12>	AC21		TRIG_P<54>	C17	
TRIG_P<13>	AC23		TRIG_P<55>	D19	
TRIG_P<14>	AB21		TRIG_P<56>	B17	
TRIG_P<15>	AB23		TRIG_P<57>	C19	
TRIG_P<16>	AA21		TRIG_P<58>	C15	
TRIG_P<17>	AA23		TRIG_P<59>	B19	
TRIG_P<18>	Y21		TRIG_P<60>	B15	
TRIG_P<19>	Y23		TRIG_P<61>	A19	
TRIG_P<20>	W21		TRIG_P<62>	A15	
TRIG_P<21>	W23		TRIG_P<63>	A17	
TRIG_P<22>	V21		VALEVENT_N	A11	I/O Digital Differential (50MHz)
TRIG_P<23>	V23		VALEVENT_P	A12	
TRIG_P<24>	U21		VBG	P3	
TRIG_P<25>	U23		VBG_1V	N3	
TRIG_P<26>	T21		VCASC_DISC	G3	
TRIG_P<27>	T23		VCASC_RX	B11	Bias
TRIG_P<28>	R21		VCN_PROBE	V3	
TRIG_P<29>	R23		VCP_PROBE	U3	
TRIG_P<30>	P21		VDAC_PA	AB3	
TRIG_P<31>	P23		VDD	F9	
TRIG_P<32>	L21		VDD	F10	
TRIG_P<33>	L23		VDD	F11	
TRIG_P<34>	K21		VDD	G9	Power Supply - VDD
TRIG_P<35>	K23		VDD	G10	
TRIG_P<36>	J21		VDD	G11	
TRIG_P<37>	J23		VDD	H6	

VDD	H7	
VDD	J6	
VDD	J7	
VDD	K6	
VDD	K7	
VDD	R6	
VDD	R7	
VDD	T6	
VDD	T7	
VDD	U6	
VDD	U7	

VDD	V9	
VDD	V10	
VDD	V11	
VDD	W9	
VDD	W10	
VDD	W11	
VREF_10BDAC	K3	
VSLOPE_10BDAC	L3	Bias
VTH	M3	

Table 5 – LIROC pin list

Power supply

The core of the ASIC is powered by 1.2V and power supplies are separated in several zone for reducing EMC influence from various section of the ASIC. It is recommended to at least separate the digital power supply from the analog power supply and to use decoupling capacitors for stabilizing & filtering the power supply. An example of power supply connection is illustrated in Figure 10.

Pin Name	Pin Type	Description	Connected to
VDD	Power Supply	Analog power supply	1.2V
P2V5	Power Supply	Input stage power supply	1.2V
DVDD	Power Supply	Digital power supply	1.2V
GND	Ground	Ground	0
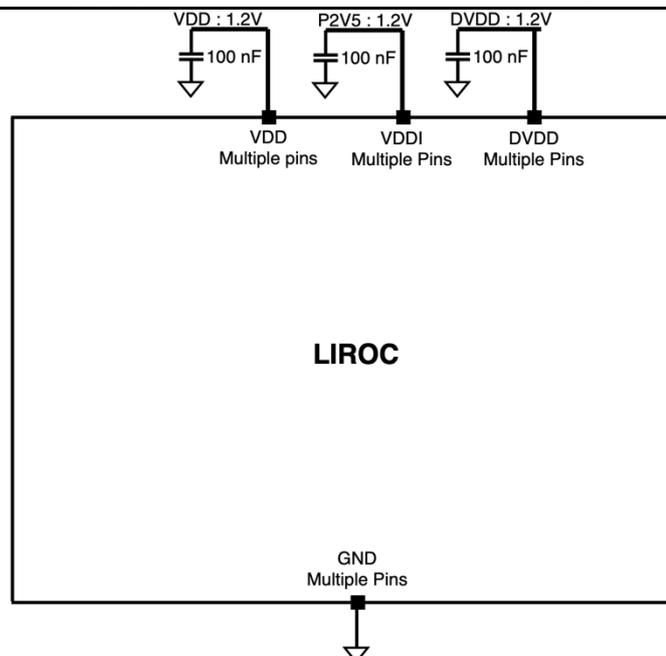
Figure 10 – LIROC power supplies connection

Input connection

The input pins are solely reserved for the detector inputs (SiPM). Short distance of traces for routing the input signal is highly recommended.

Pin Name	Ball Map	Description	Connected to
IN<0:63>	Various location (refer to Table 5)	Connection to detector	Detector anodes or cathodes

For the usage of the SiPM standard output (anode or cathode) is recommended to have a 50 ohm resistor with 100 nF capacitor in series to the ground before connecting the detector output to the ASIC.
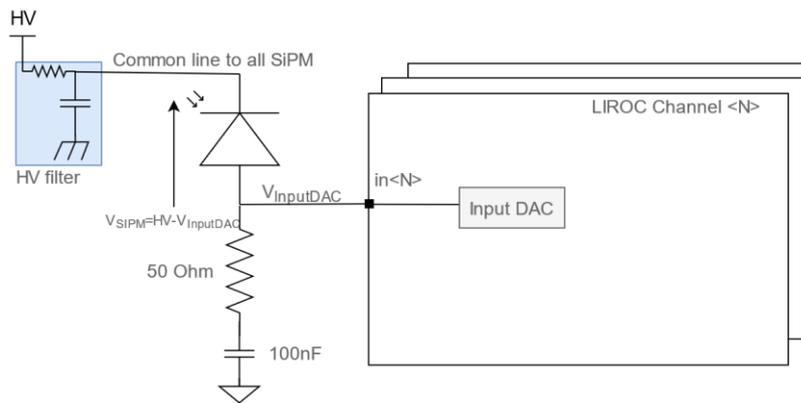
Figure 11 – Example of SiPM connection to LIROC ASIC

Biasing & debugging connections

Biasing pins are mostly optional I/Os which are available for debugging and analog section biasing modification if required. It could be left open or connected to decoupling capacitors in most cases. However, if a biasing modification is required, it is also possible to connect the pin to resistor-based voltage divider (refer Figure 12). The expected DC value of each pin can be found in Table 2. Additionally, the proposed connection for debugging pins (ANALOG_PROBE1/2 & IN_CTEST) is shown in Figure 13.

Pin Name	Ball Map	Description	Connected to
ANALOG_PROBE1	N1	Probe monitoring output for North side (channel 0 - 32)	Analog buffer & oscilloscope
ANALOG_PROBE2	M1	Probe monitoring output for South side (channel 33 - 63)	Analog buffer & oscilloscope
IBD_PA	AC8	Pre-amp differential pair current bias	Not connected, decoupling capacitor and/or voltage divider
IBI_BG	T3	Input stage bandgap bias	Not connected, decoupling capacitor and/or voltage divider
IBI_DISC	C3	Input stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBI_N_PROBE	Y3	Input stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
IBI_OTA_10BDAC	J3	Input stage of OTA trigger threshold bias	Not connected, decoupling capacitor and/or voltage divider
IBI_PA	AA3	Input stage pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
IBI_P_PROBE	W3	Input stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
IBM1_DISC	E3	Medium stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBM2_DISC	AC10	Medium stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBO_BG	R3	Output stage bandgap bias	Not connected, decoupling capacitor and/or voltage divider
IBO_DISC	B7	Output stage discriminator bias	Not connected, decoupling capacitor and/or voltage divider
IBO_OTA_10BDAC	H3	Output stage of OTA trigger threshold bias	Not connected, decoupling capacitor and/or voltage divider
IBO_PA	B8	Output stage pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
IBO_PROBE	D3	Output stage probe amp bias	Not connected, decoupling capacitor and/or voltage divider
IN_CTEST	AD9	Charge injection input	Waveform generator or pulser
I_OFFSET_DISC	F3	Hysteresis discriminator bias	Not connected, decoupling capacitor and/or voltage divider
VBG	P3	Bandgap output	Decoupling capacitor and/or

			voltage divider
VBG_1V	N3	1V low impedance ref output	Decoupling capacitor and/or voltage divider
VCASC_DISC	G3	Discriminator cascode	Decoupling capacitor and/or voltage divider
VCASC_RX	B11	LVDS receiver cascode	Decoupling capacitor and/or voltage divider
VCN_PROBE	V3	Probe amp N cascode	Decoupling capacitor and/or voltage divider
VCP_PROBE	U3	Probe amp P cascode	Decoupling capacitor and/or voltage divider
VDAC_PA	AB3	Pre-amp DC level	Decoupling capacitor and/or voltage divider
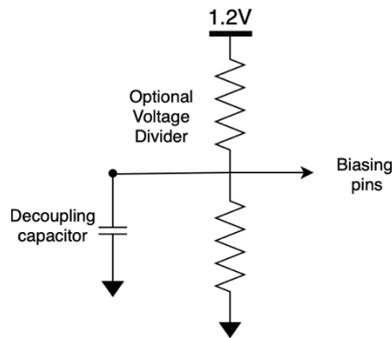
Figure 12 - Proposed connection for biasing points.
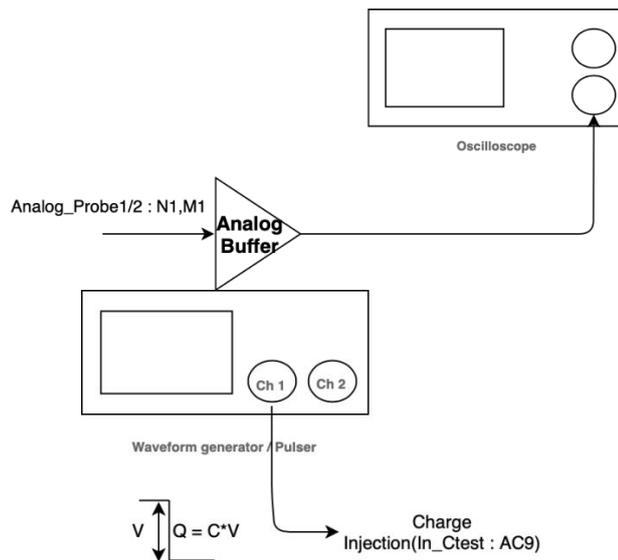
Figure 13 - Proposed connection for ANALOG_PROBE1/2 (Left figure) and IN_CTEST (Right figure)

Digital connections

The digital I/Os are divided into 4 types : open collector, single-ended, bidirectional and differential (CLPS[1]). The proposed connection for bidirectional and differential pins are shown in Figure 14 and for I2C, resets and trigger I/Os is shown in Figure 15. The pins are active high unless it is stated to be active low.

Pin Name	Ball Map	Description	Connected to
CHIP_ID<0:3>	M23,N24, N23, N22	Chip ID for I2C : Single Ended	FPGA or hard wire to user defined chip address
CLK_SM_I2C	A10	Clock for I2C slave core : Single Ended	FPGA
ERRORB_SC	M24	Bit flip error output, low level flag : Open Collector	FPGA with 47k Ohm pull up resistor to 1.2V
POWER_ON	A8	Power ON signal for sequentially powering on/off the whole ASIC : Single Ended	FPGA
RSTB_I2C	A13	Low level reset (min 50ns) for I2C slave core : Single Ended	FPGA
RSTB_PROBE	AD13	Low level reset (min 50ns) for probe (analog debugging & signal monitoring) registers : Single Ended	FPGA
SCL	B10	SCL line for I2C	FPGA with 47k Ohm pull up resistor to 1.2V
RESETB_SC	B9	Low level reset (min 50ns) fo Slow Control registers: Single Ended	FPGA
SDA	A9	SDA line for I2C : Bidir	FPGA with 47k Ohm pull up resistor to 1.2V
SRIN_PROBE	AD12	Input for probe (analog debugging & signal monitoring) registers: Single Ended	FPGA
SROUT_PROBE	AD11	Output for probe (analog debugging & signal monitoring) registers: Single Ended	FPGA
CLK_PROBE	AD14	Clock input for probe (analog debugging & signal monitoring) : Single Ended	FPGA
NOR64	A14	NOR64 output for trigger : Open Collector	FPGA with 47k Ohm pull up resistor to 1.2V
TRIG_N/P<0:63>	Various location (refer to Table 5)	Differential trigger outputs : CLPS	FPGA
VALEVENT_N/P	A11, A12	Differential fast discriminator masking inputs : CLPS	FPGA

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[1] CLPS stand for CERN Low Power Signaling. It is not a fairly common digital I/Os standard. The common voltage is set at 0.6V with signal swing of 300mV.
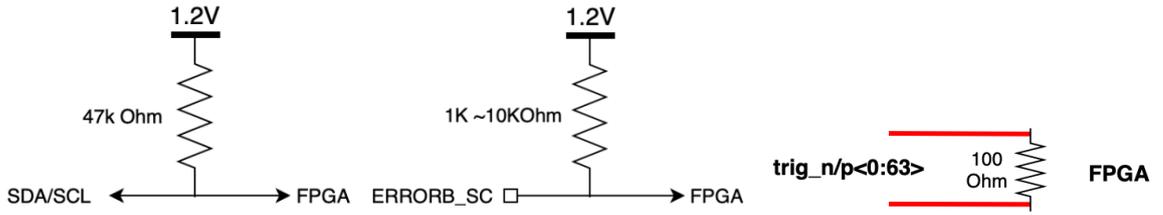
Version 0.2 -29/11/2024

Figure 14 – Left : Proposed connection for SDA/SCL. Middle : ERROB_SC. Right : trig_n/p<0:63> differential connection.
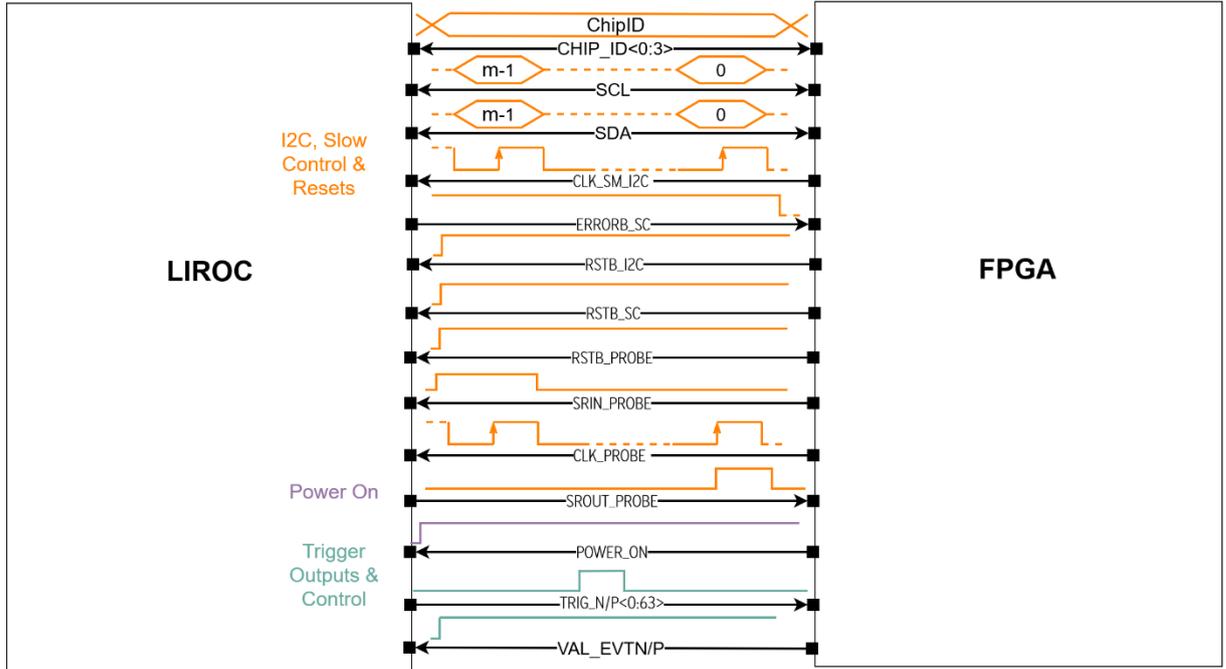

Figure 15 – Proposed connections for I2C, Reset and trigger I/Os

LIROC analog operation

The analog part of LIROC is composed of the dual polarity pre-amplifier followed by a discriminator for input signal discrimination and triggering. The threshold is set with 10-bit DAC (ASIC wide threshold) and followed with 7-bit trimming which is embedded in each channel. Simplified block diagram of the analog section is shown in Figure 16.
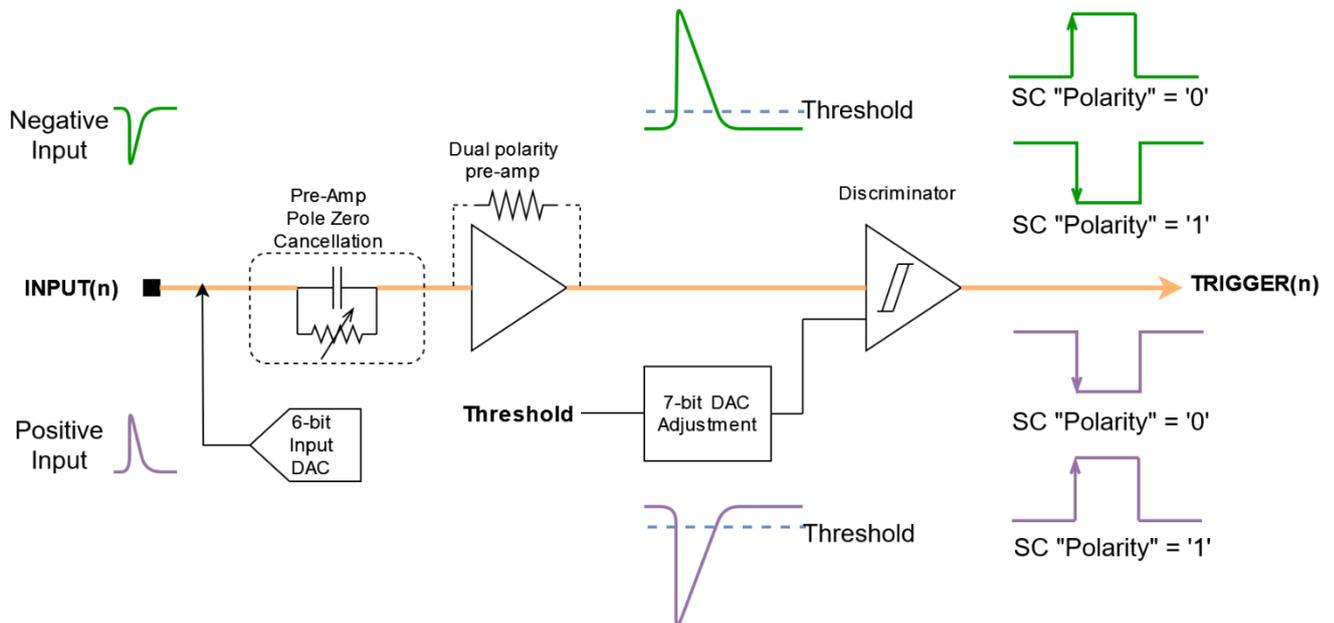
Figure 16 – Analog section block diagram.

The pre-amp employed here is transimpedance amplifier, which will convert current pulses input, and transform the input signal into voltage through a resistor.

Additionally, there is a 6-bit input DAC that can be used for adjusting the SiPM overvoltage non-uniformity. This setting is accessible through the following Slow Control bits and will be effective for each ASIC input:

- DC_PA<5:0> (Address: 0-63; Subadd : 0; Bits : 7-2). Range = 395 ~ 672mV   , Step = 4.4 mV

For the setting the pre-amp Pole Zero Cancellation (PZC), it is done through a RC network with a fixed capacitor of 5pF. The resistor value is variable and can be changed through Slow Control :

- PA_gain<3:0> (Address: 64; Subadd : 0; Bits : 5-2). PA_gain<3> = 16k 0hm, PA_gain<2> = 8kOhm, PA_gain<1> = 4kOhm and PA_gain<0> = 2kOhm. The resulting resistor is parallel combination of these 4 resistors values.

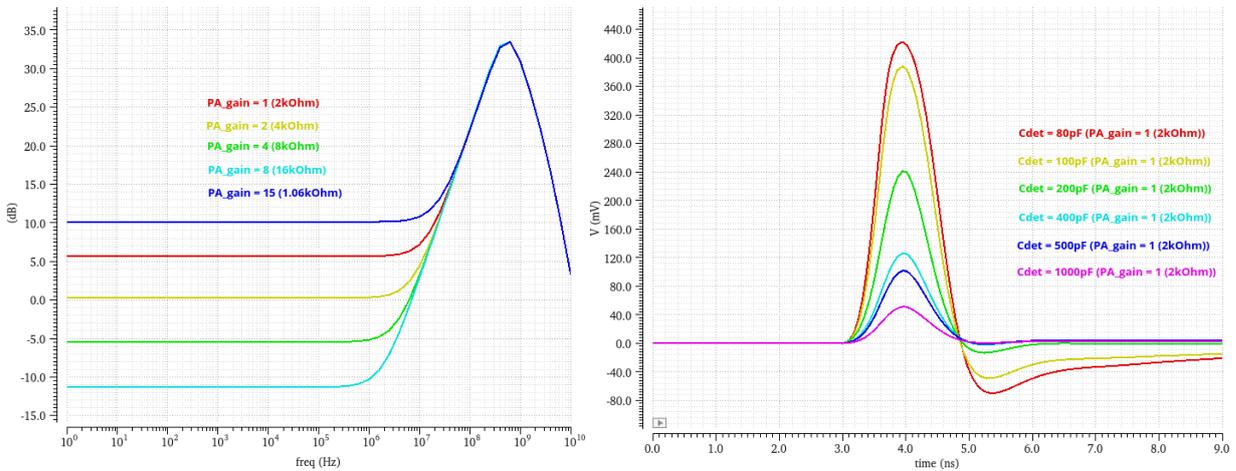Example outputs (simulated) of the PZC are shown in the following figures.

Figure 17 – Pole Zero Cancelation frequency responses (Left) and Transient responses wrt various detector impedance (Right)

Additionally, a pre-amp biasing adjustment is also available. The adjustment will tune the base current applied to the pre-amp. It is accessible to the following Slow Control bits :

- PA_comp<3:0> (Address: 64; Subadd : 1; Bits : 3-0). Range = 52.5uA ~ 0, Step = 3.5 uA, Default value : 45.5uA

The DC level of the pre-amplifier is about 460mV (with default setting) and this signal will be fed directly into a discriminator. In order to set the trigger threshold, a 10-bit DAC used as a common threshold for the discriminator and the settings of this threshold are accessible through the following Slow Control bits:

- DAC<9:8> (Address: 65; Subadd : 1; Bits : 1-0) & DAC<7:0> (Address: 65; Subadd : 2; Bits : 7-0). Range (with default trim) : 298mV~738mV, Step :0.43mV, Default value : 501mV (with default trim)

Additionally, to fine tune this threshold, there is a 7-bit trimming which is available for each channel. The threshold after the trim will be the effective trigger threshold in each channel. This setting is accessible through the following Slow Control bits :

- DAC_local (Address: 0-63; Subadd : 1; Bits : 6-0). Range : 0 ~ -152.4mV , Step : -1.2mV, Default value : 76.8mV

The discriminator embedded is a 3-stage discriminator designed for fast output response. A few settings are available for this discriminator. The first one is for the discriminator output polarity. Depending on the input signal, the discriminator output will be on either the rising edge or the falling edge (refer to Figure 16). This setting is accessible through the following Slow Control bit :

- Polarity (Address: 64; Subadd : 2; Bits : 5). '0' : positive polarity output for negative input signal; '1' : positive polarity output for positive input signal. Default value '1'.

Based on Polarity SC bit choice, the discriminator output will be positive polarity (first edge on the rising) if the input is on the negative polarity and Polarity SC bit = '0'. The discriminator output will be on the negative output (first edge on the falling) if the Polarity SC bit is set to '1' and the input is on the negative polarity. On the other hand, if the input is on

positive polarity, the trigger output will be positive and negative polarity if the Polarity SC bit is set to '1' and '0' respectively.

The discriminator output can be masked, channel-by-channel, using the following Slow Control bit:

- Mask (Address: 0-63; Subadd : 1; Bits : 7). '0' for no mask, '1' for mask.

In order to have ASIC wide trigger masking, an external signal has to be used instead. It is a differential input at the following pin :

- VALEVENT_N/P (Ball map : A11/A12) : Low Level for mask, High Level for no mask.

Other analog settings available are for charge injection and CLPS differential driver tuning. For the charge injection, this Slow Control bit is used to enable or disable this part for each channel :

- Ctest (Address: 0-63; Subadd : 0; Bits : 1). '0' for disable charge injection, '1' for enable charge injection.

The charge injection has to be used in conjunction with a dedicated ASIC input, available at the following pin :

- In_Ctest (Ball map : AC9) : Low Level for negative polarity charge injection, High Level for positive polarity charge injection.

For the differential output driver, users can control the buffer size (EN-CLPS<0:3>, setting overall amplitude), pre-emphasis (EN-pE<0:3>, for edge slope) and pre-emphasis delay (pE-Delay<0:1>, setting the delay for reaching the transmission amplitude) at the following Slow Control bits:

- EN-CLPS <0:3> (Address: 66; Subadd : 0; Bits : 7-4). Range : 58mV ~ 348mV, Step : 19mV, Default value:348 mV
- EN-pE <0:3> (Address: 66; Subadd : 0; Bits : 3-0). Range : 536MV/s ~831MV/s , Step : 18.5MV/s, Default value:748MV/s
- pE-Delay<0:1>, (Address: 66; Subadd : 1; Bits : 7-6). "00" : 122ps; "01" :252ps; "10"|"11" :377ps. Default value : 377ps
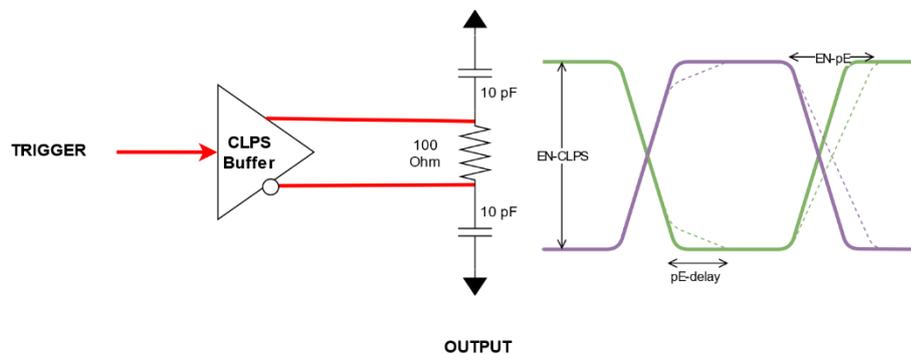

Figure 18 – Setting for CLPS differential buffer outputs

Analog probe

In order to monitor or probing the analog signal, there are two probing point available: Pre-amp and Threshold(Vth). These probing points are accessible through the following interface which will store the channels number within a shift register:

- clk_probe (AD14) – Clock for shifting the register input
- rstb_probe (AD13) – Reset of shift register
- srin_probe (AD12) – Shift register input, data toggled on rising edge of clk_probe
- srout_probe (AD11) – Shift register output, data toggled on the falling edge of clk_probe

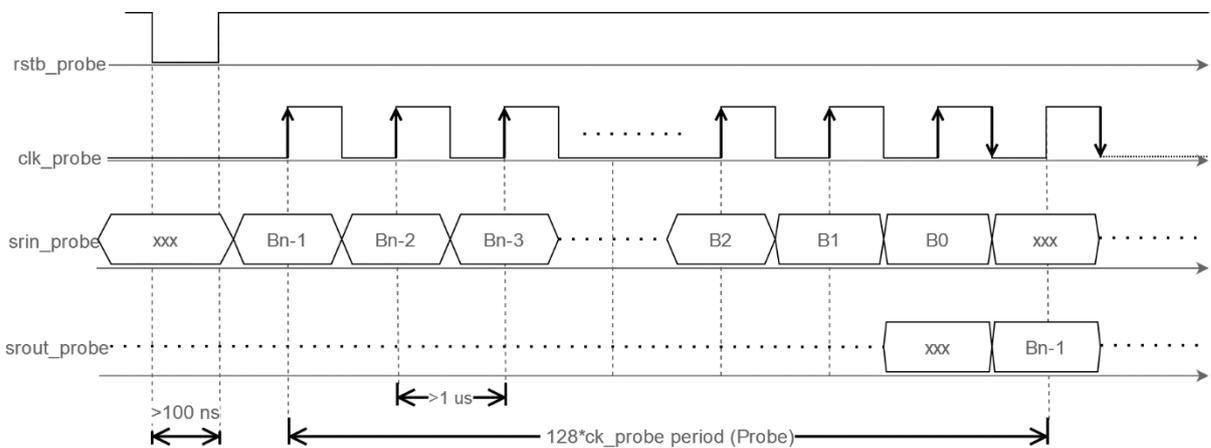The timing diagram is shown in the following figure:

Figure 19 - Probe shift register timing diagram

The bit corresponding to the probe signal is listed in the following table:

Bit	Probe Type	Probe Signal	Probe Output
127	analog	Pre-amp channel<0>	ANALOG_PROBE1(N1)
126	analog	Pre-amp channel<1>	ANALOG_PROBE1(N1)
...	...	...	...
96	analog	Pre-amp channel<31>	ANALOG_PROBE1(N1)
95	analog	Pre-amp channel<32>	ANALOG_PROBE2(M1)
94	analog	Pre-amp channel<33>	ANALOG_PROBE2(M1)
...	...	...	...
64	analog	Pre-amp channel<63>	ANALOG_PROBE2(M1)
63	analog	Threshold channel<0>	ANALOG_PROBE1(N1)
62	analog	Threshold channel<1>	ANALOG_PROBE1(N1)
...	...	...	...
32	analog	Threshold channel<31>	ANALOG_PROBE1(N1)
31	analog	Threshold channel<32>	ANALOG_PROBE2(M1)
30	analog	Threshold channel<33>	ANALOG_PROBE2(M1)
...	...	...	...
0	analog	Threshold channel<63>	ANALOG_PROBE2(M1)

LIROC floorplan & packaging

Preliminary mechanics give a naked die size of 4.72mm*11.12mm including scribe line giving a die area of 52.5 mm2. The ASIC has 516 bump pads which will be bonded to BGA substrate.
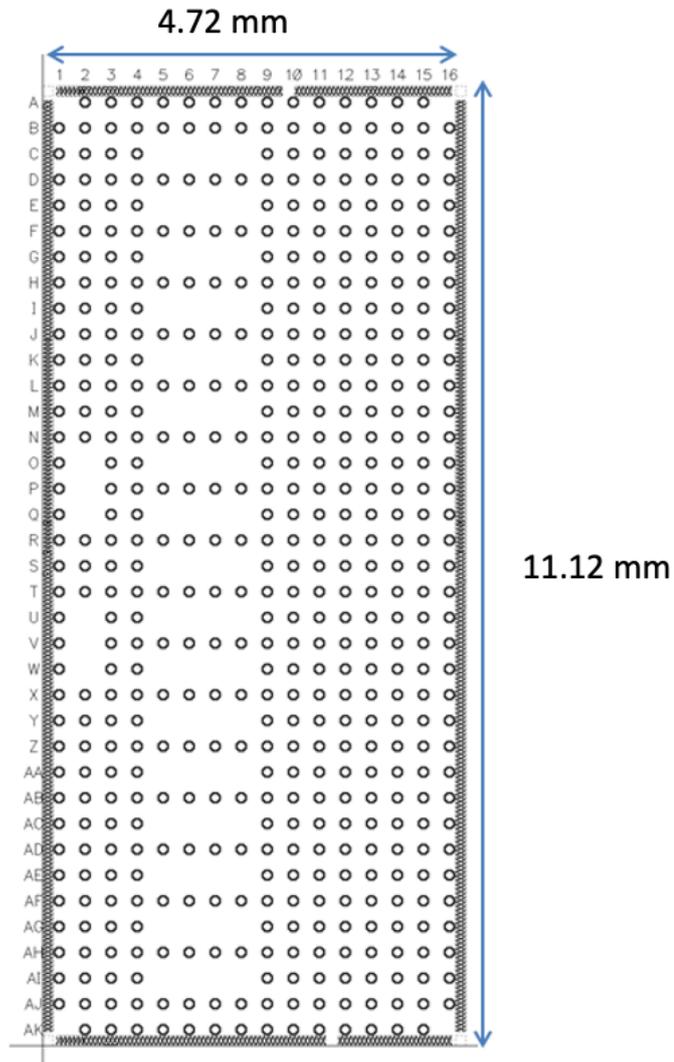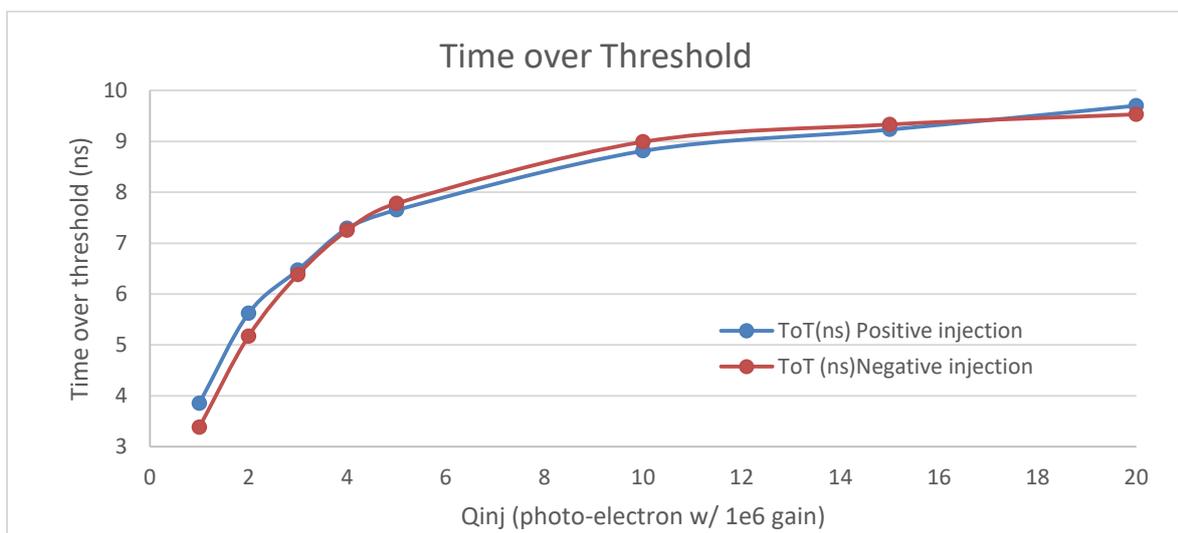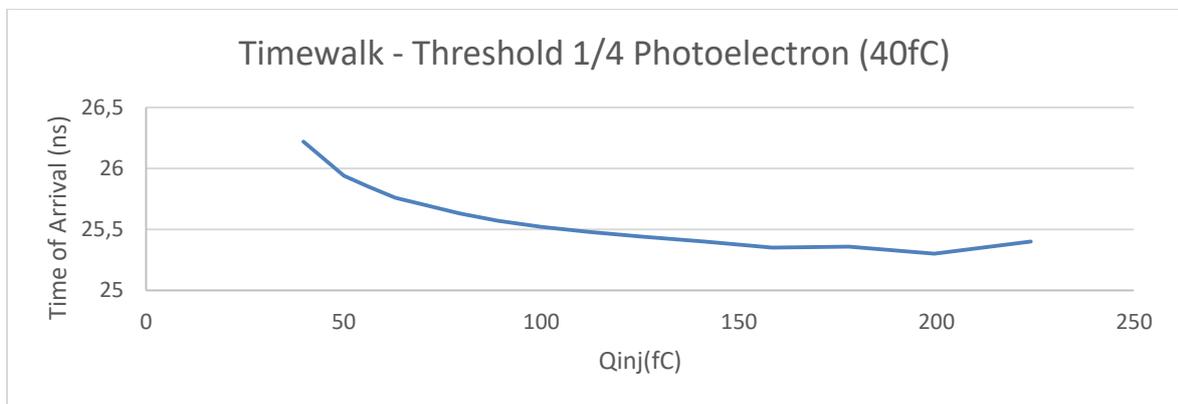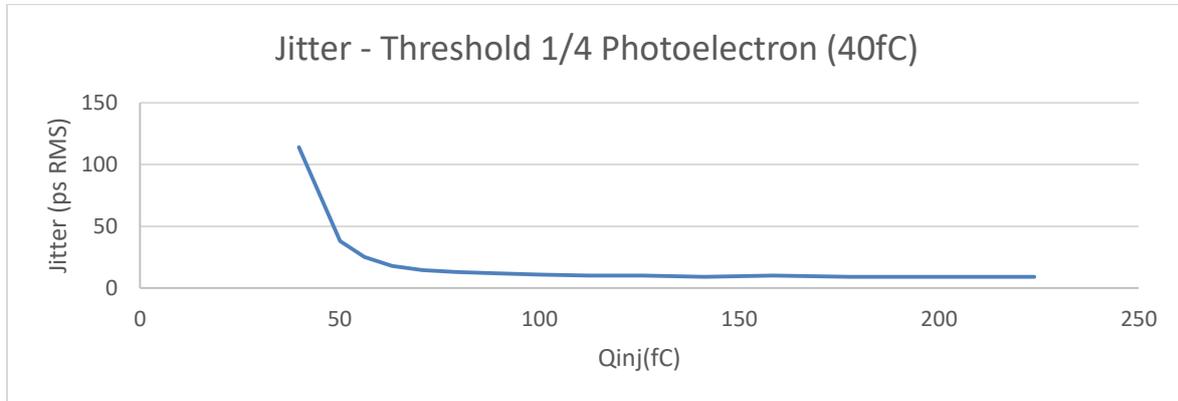

Figure 20 – Preliminary padring and form factor

Version 0.2 –29/11/2024

LIROC timing performances

Trigger outputs of LIROC have been measured and the results are reported in the following figures.

Jitter - Threshold 1/4 Photoelectron (40fC)

Timewalk - Threshold 1/4 Photoelectron (40fC)

Time over Threshold

As reported, the jitter of the trigger outputs are relatively low, about 10ps RMS for input signal starting from 100fC. Additionally this ASIC could be able in TOT mode up to tens of photoelectron.

Datasheet version history

Version	Date	Information
0.1	19/03/2024	Initial release – pre-production measurement
0.3	29/11/2024	Package Correction, supress 'Z' raw for JEDEC Compliance