



Datasheet Petiroc 2A



Petiroc 2A is a 32-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) for particle time-of-flight measurement applications. Petiroc 2A combines a very fast and low-jitter trigger with accurate charge and time measurements.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6 mW/channel, excluding buffers used to output the signals.

The main application of Petiroc 2A is PET time-of-flight but it can also be used for any application that requires both accurate time resolution and precise energy measurement.

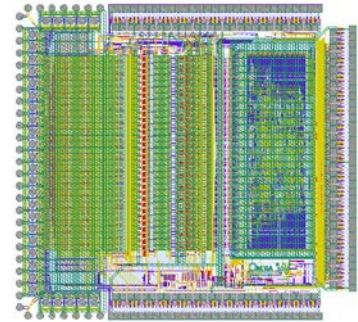


Figure 1 – Petiroc 2A layout

Parameter	Value
Detector Read-Out	SiPM
Number of Channels	32
Signal Polarity	positive or negative
Sensitivity	Voltage input amplifier, 200 Ohm matching
Timing Resolution	~ 18 ps RMS on trigger output (4 photoelectrons injected)
Dynamic Range	160 fC up to 400pC
Packaging & Dimension	LQFP 208 (28x28x1.4 mm) TFBGA 353 (12x12x1.2mm)
Power Consumption	6 mW/channel
Inputs	32 analogue inputs for SiPM connection, no external component required Inputs DC are adjustable to correct SiPM breakdown voltage non uniformity.
Outputs	32-channel trigger outputs ASIC level general trigger (OR of all channel) ASIC level second level general trigger (OR of all channel for energy cut) Charge measurement (10 bits) Time measurement (10 bits TDC interpolating 40MHz coarse time) One multiplexed analogue charge output One multiplexed digital trigger output
Internal Programmable Features	Common trigger threshold adjustment and 6bit-DAC/channel for individual adjustment Shaping time & gain of the charge shaper 32 8bit-input DAC for SiPM HV adjustment over 1V span

Table 1 – ASIC main parameters



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1 General description

1.1 Overall circuit description

Petiroc 2A is a 32-channel front-end ASIC designed in AMS 0.35 μ m SiGe technology. Petiroc 2A is available in LFP208 and TFBGA353 package.

Each of the 32 channels of Petiroc 2A is composed of a low-power input DAC to adjust the high voltage of the SiPM over a 1V range.

A fast trigger line is made of a 1GHz bandwidth preamplifier which is DC coupled to the detector. Each amplifier is followed by a fast discriminator; the output of the discriminator can be latched. A Time to Amplitude Converter (TAC) is embedded in each channel and allows a time measurement with a 37 ps bin. This TAC allows to interpolate timing measurement between within a 25 ns period (40 MHz). This time measurement is then digitized over 10 bits by an internal Wilkinson ADC (ramp converter).

A charge measurement line is composed of a variable time shaper (from 25 ns up to 100 ns) allowing charge measurement up to 2500 pe⁻ (or 400 pC for a SiPM gain of 10⁶) followed by an analogue memory. The shaper is followed by a switched capacitor to store the maximum value of the charge. The Hold signal can be provided externally or internally. The internal hold can be delayed between 25ns and 100ns by an 8-bit resolution delay mechanism. This charge measurement is digitized with a 10-bit Wilkinson ADC.

A discriminator follows each of the charge amplifiers to provide a second level trigger information allowing to event above a certain energy threshold to reject noise.

A common 10-bit DAC followed by an individual 6-bit DAC ensures the trigger level adjustment from 0.5 to a few tenth of photoelectrons. A bandgap provides a stable reference for the different biasing and reference voltages throughout the ASIC. A temperature sensor allows an analogue measurement of the ASIC temperature that will reflect the temperature of the system because Petiroc 2A is aimed to be located close to the SiPMs. The block diagram of Petiroc 2A is shown in Figure 2.

The pin or ball-out numbering used throughout this document can be referred in Table 8, Figure 47, Figure 48, Figure 49 and Figure 50.



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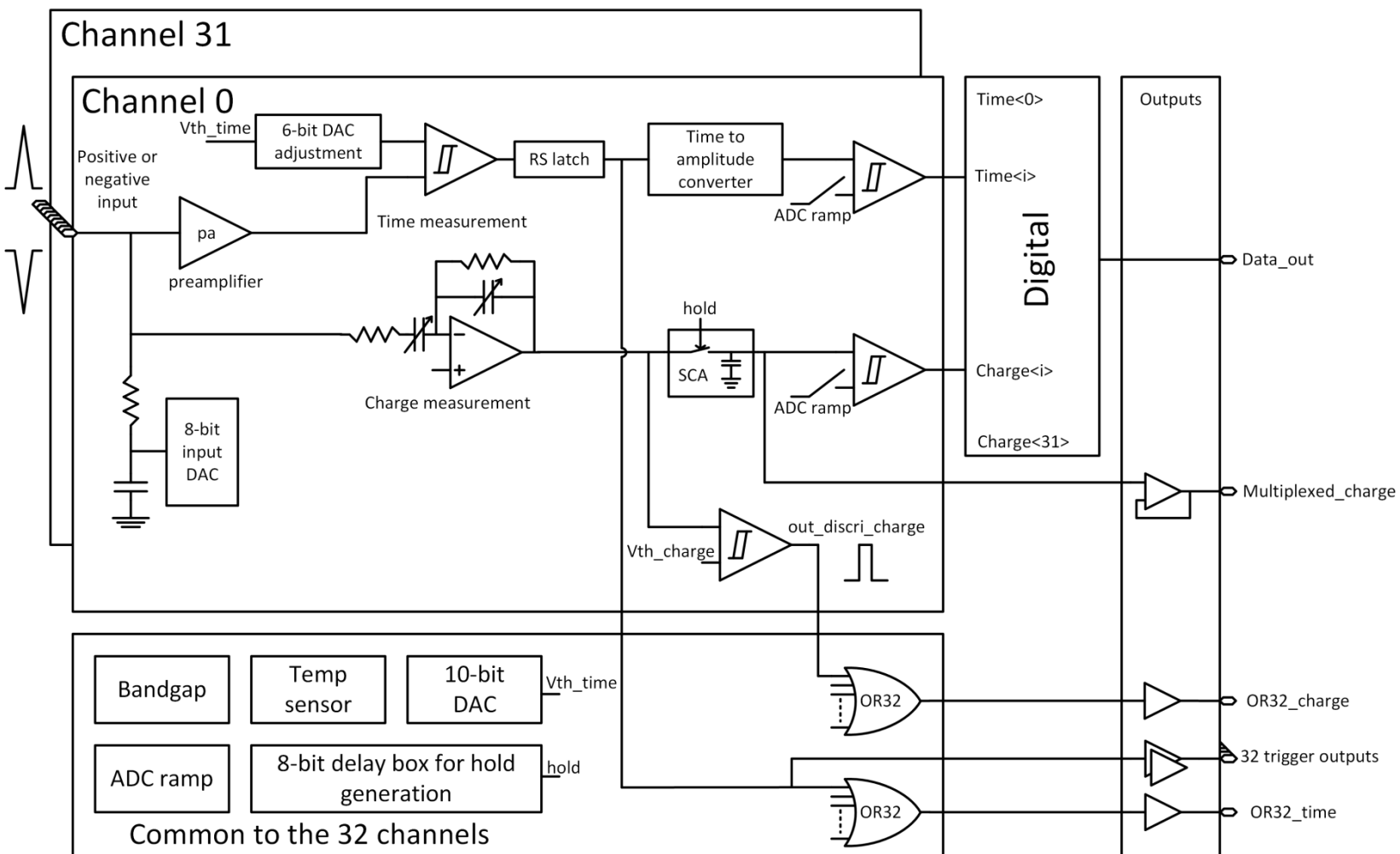


Figure 2 - General ASIC block scheme



1.2 Petiroc 2A operation modes

Petiroc 2A can be used in different configuration mode depending on foreseen application. The circuit can be used in full analogue mode without any internal clocking either as a photon counting device or triggered charge measurement using either output triggers and multiplexed analogue output or fully digitized output data using internal ADC and TDC.

1.2.1 Photon counting mode

In photon counting mode, Petiroc 2A first level threshold can be set below one photoelectron. Channel triggers can either be latched or not (LatchDiscri slow control parameter). In latch mode, the ASIC can be reset with a digital input to be ready for new acquisition (RazChn digital input signal). It is possible to time window the triggers to focus measurement on dedicated moments and reject unwanted event (ValEvt digital input signal). It is possible to mask any channel to reject noisy SiPM using the slow control parameter Mask.

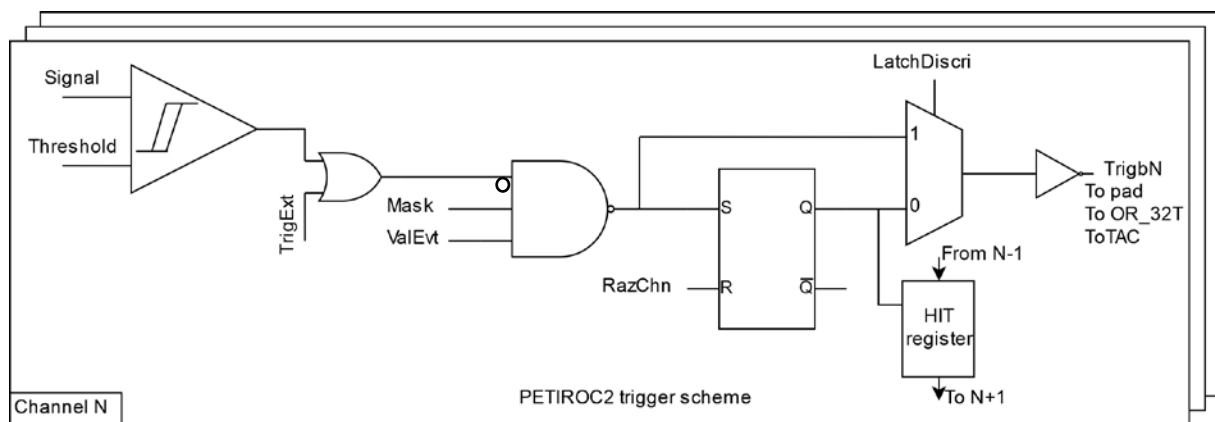


Figure 3 – Petiroc 2A trigger scheme

1.2.2 Analogue time and charge measurement

In analogue mode, no clock is used to run Petiroc 2A. Digital part of the ASIC is turned off and asynchronous digital signals are used to control and extract the data from Petiroc 2A.

An internal multiplexer allows reading sequentially the 32 channels after trigger and hold of maximum value of the charge measurement shaper. On each of the 32 serial reading sequences, the charge and the hit value is output from Petiroc 2A, Charge measurement must be converted using an external ADC.



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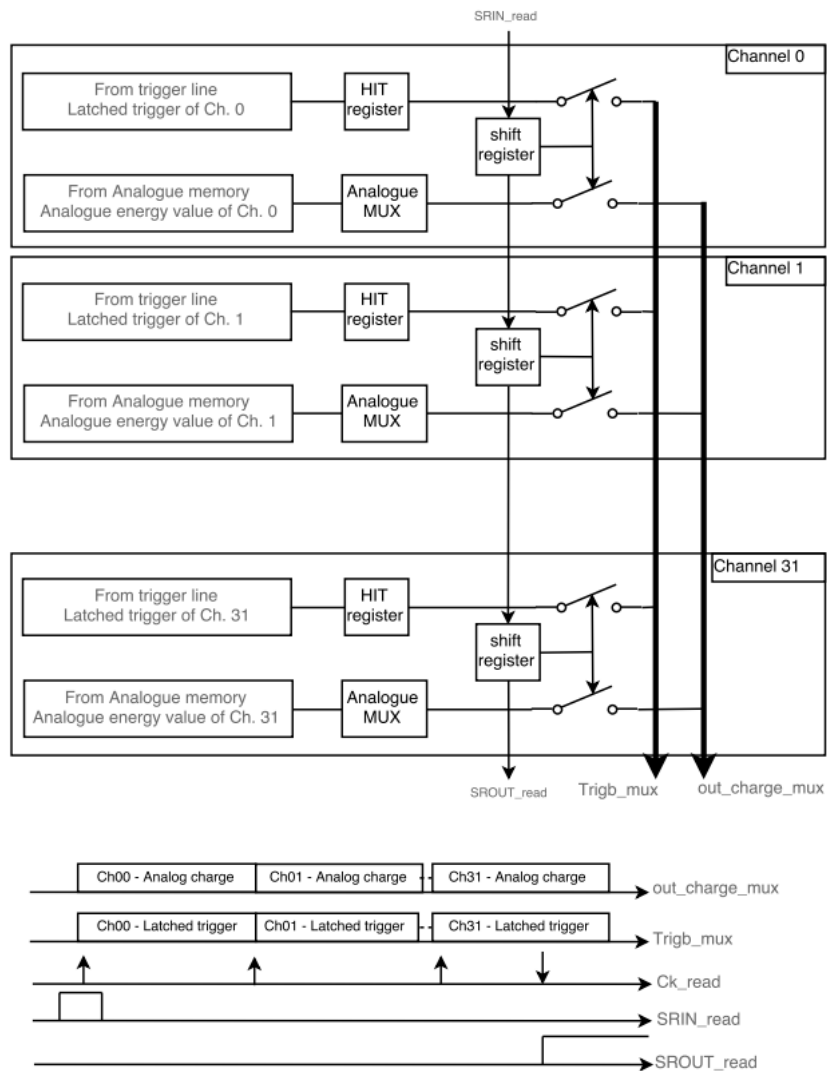


Figure 4 - Analogue read-out of Petiroc 2A

1.2.3 Full digital time and charge measurement

In full digital mode, the ASIC provide all digital data on the dout or dout_n/p pins, the time and charge of all channels are outed following the block scheme shown below. Analogue buffer can be switched off. In full digital mode, the rate is limited to 40kEvent/s due to analogue to digital conversion (12.8 us maximum) and serial data outing (12us).



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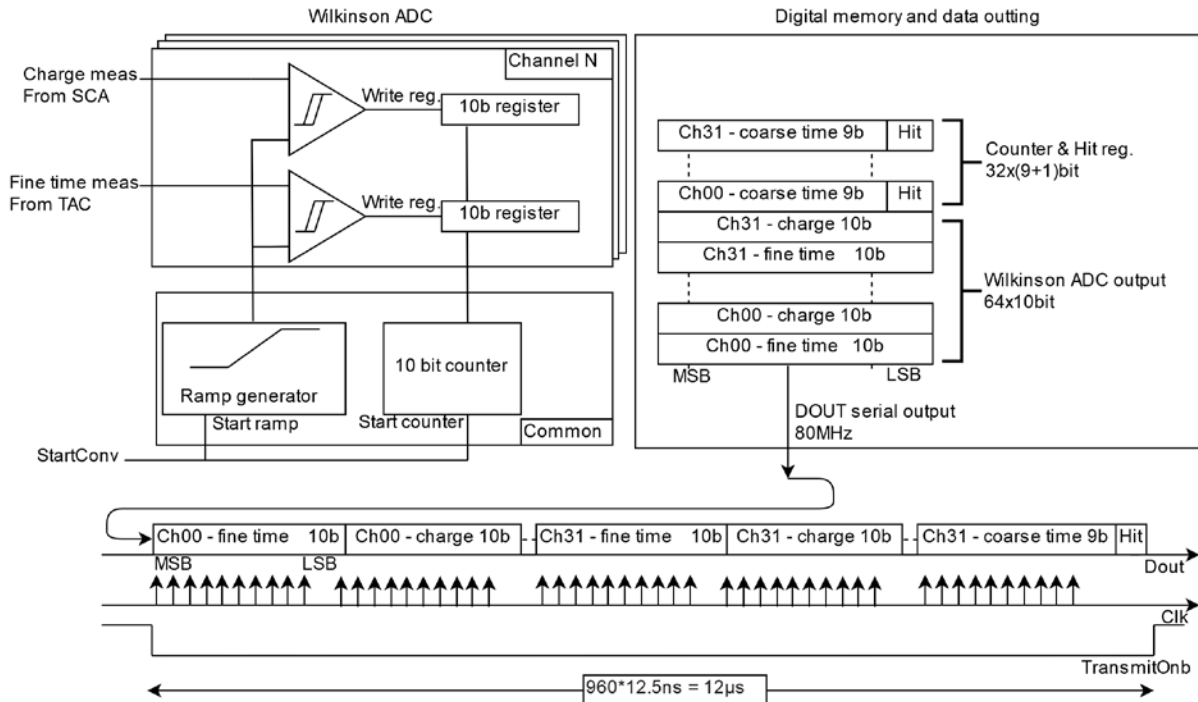


Figure 5 - Digital read-out of Petiroc 2A

2 Maximum ratings

The operating condition of Petiroc 2A should not exceed the parameters listed in Table 2.

Parameter	Note	Minimum	Maximum	Unit
Storage temperature range		-40	125	°C
Operating temperature range		-20	110	°C
Power pin	All VDD power pins (3.3V – vdd_x)	0	3.5	V
Ground pin	All ground (gnd_xx) and vss pins	0	0	V
Analogue input		-0.5	VDD+0.3	V
Digital input LVCMOS		-0.5	VDD+0.3	V
Digital input LVDS		-0.5	VDD+0.3	V

Table 2 - Maximum rating operation condition

Petiroc 2A electrostatic discharge (ESD) protection is HBM (Human Body Model) compatible on every pin.



3 ASIC Front-end

The ASIC front-end is composed of the input DACs, high-bandwidth pre-amplifier & Time trigger for time measurement and CRRC shaper, analog memory and Charge trigger for charge measurement.

3.1 SiPM High voltage trimming

At the input of the ASIC, an input DAC (Refer to Figure 2 – 8-bit input DAC) is available for each channel. This DAC can be used to trim the high voltage (HV) applied to the SiPM by either increasing (for negative HV) or decreasing (for positive HV) the effective value applied to each detector channel. This feature will allow user to adjust the detector gain non-uniformity especially when using the chip with SiPM array. The input DACs can be controlled through Slow Control registers (refer to Table 4) from Bits #32 to #327. The DAC input is binary-coded decimal on 8 bits and its electrical characteristics are the following:

- Output : 1-2 V, Range : ~1 V
- Min value (DAC code = 0) : ~1 V
- Max value (DAC code = 255) : ~2V
- LSB : ~4.11 mV/DAC unit

Refer to Section 6.1 for ASIC connections to detectors. It is not recommend to disable the input DAC (Slow Control bits cmd input DAC chx ='0') as it will clamp the pre-amp input level to the ground.

3.2 Preamplifier

The pre-amplifier, denoted as "pa" in Figure 2, is a high bandwidth (GBW > 1 GHz) inverting voltage amplifier with a fixed gain of 40 which is suitable for amplifying fast signal such as SiPM outputs. Should user would like to reduce the gain, a quick hot fixes on how it can be done, is listed in Section 10 – item 1. User should take into account the inversion of the output signal and its baseline presence when setting the threshold for Time trigger.

3.2.1 Time Trigger

Time trigger is one of the most crucial features of the ASIC where the usage of this trigger is twofold:

- To time stamp the incoming input signal by producing "fine" time measurement within a 25 ns window
- To provide a delayed signal for holding and sampling shaper waveform for charge measurement (Section 3.3)

The triggering scheme is depicted in Figure 6.

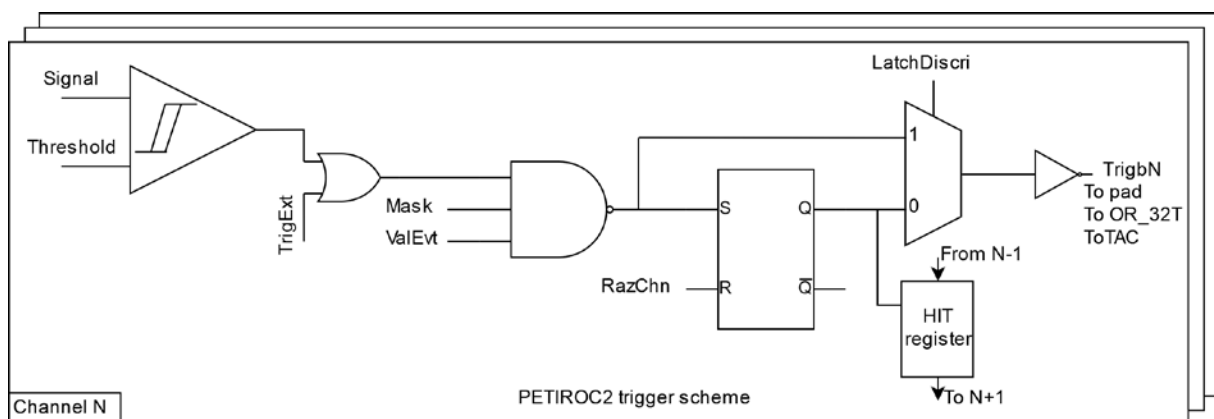


Figure 6 - Time triggering scheme in Petiroc 2A.



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As shown in the figure, the pre-amplifier signal arrives where "Signal" input is placed, and then compared to the "Threshold" at the discriminator inputs. The discriminator outputs will go through a series of logic gates before it can be used for other usage.

It should be noted this Time trigger threshold is a combination of 2 type of DACs :

- 10-bit common value from a dual outputs DAC (vth_time) :
 - o Slow Control bits #564(MSB) - #573(LSB) – BCD coded
 - o Output : 0.89 – 1.89 V with ~0.92mV/DAC Unit
- 6-bit channel specific trimming based on the value of 10-bit common DAC :
 - o Slow Control bits #360 - #551 with 6 bits per channel – BCD coded
 - o Range : ~100 mV with ~1.5 mV/DAC Unit
- Effective threshold value for each channel will be the following :
Time Threshold = 0.89 V + (10-bit DAC value*0.92 mV) – (6-bit DAC value * 1.5 mV)

For controlling the trigger outputs, combinations of the Slow Control parameters and input pins are required :

Input pins:

- val_evt – (pin 116/118 or T19/T22) → This signal will mask all trigger output when set a low level (LVDS input). ValEvt on Figure 6.
- trig_ext – (pin 87 or AC 16) → This signal will override all trigger outputs when no trigger is fired internally. TrigExt on Figure 6.
- raz_chn – (pin 109/111 or W22/T19) → This signal will takeover the internal "Razchn" signal shown in Figure 6 : Will reset the trigger outputs in "latch" mode or pull down the trigger outputs when in non-latch mode. Can be used only in conjunction with Slow Control #620='0'.

Slow Control parameters (Refer to Table 4 for more info) :

- mask_discri_time_chx (bits #328 - #359) – mask the trigger output individually for each channel. '1' value will mask the trigger. Mask on Figure 6.
- cmd_polarity (bit #598) – selecting the correct trigger output polarity based on input signal. '0' for negative input signal, '1' for positive input signal (Figure 7).
- LatchDiscri (bit #599) – this bit will set the trigger in latch mode ('1') or direct output ('0'). Trigger is required to be latched (Slow Control #599='1') in order to use the internal time & charge measurement.



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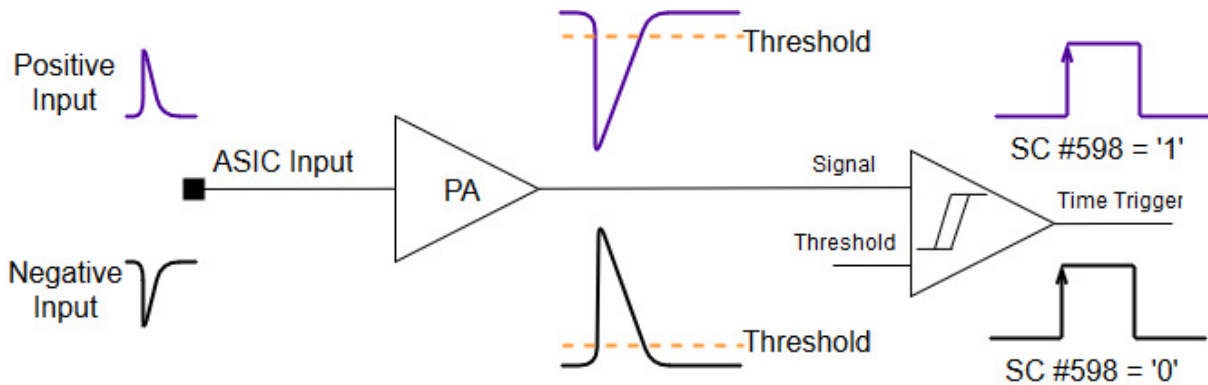


Figure 7 - Time trigger polarity

The trigger outputs are available directly on the ASIC pins at several locations (refer to Table 8 for more information) :

- 32 trigger outputs – trigb<0-31> - several pin locations : direct trigger output (latch or non- latch mode) for each channel (Active Low).
- Trigger multiplexer output – trig_mux – pin 120 or R22 : A multiplexer for 32 triggers (Active High). Channel selection for the output is done via Read registers (Section 5.4).
- NOR32 for Time Trigger – NOR32_time – pin 123 or P19 : A 32-input NOR gate for the time triggers in the ASIC (Active Low).

Additionally other Slow Control parameters such as Dis_triggers (bit #637), Dis_trig_mux(bit#634) and EN_NOR32_Time(bit #635) will affect the outputs behaviors on ASIC pins of the 32 triggers, trigger multiplexer and Time trigger NOR32 output respectively. Refer to Table 4 for more information.

It should be noted that Time Trigger has to be configured in latch mode (Slow Control bit #599 =1) and Razchn left to be generated internally in order to use the internal time and charge measurement in this ASIC (Refer to Section 4.2 for more info on the read out operation). However in the case of event rejection and internal ASIC measurement is not required, trigger latch has to be reset externally through the raz_chn (pin 109/111 or W22/T19).

3.3 Charge measurement shaper

A CRRC shaper (Figure 8) is connected directly to each input of the ASIC. The capacitors C1 and C2 (feedback) can be changed using the Slow Control parameters. With the default setting, $R1C1$ is equal to $20k \cdot 1.25pF = 25ns$ and $R2C2 = 250k \cdot 100fF = 25ns$ giving a shaping time of 25ns and a gain for a dirac input of 12.5. The Slow Control bits required for controlling C1 and C2 are listed in Table 3.

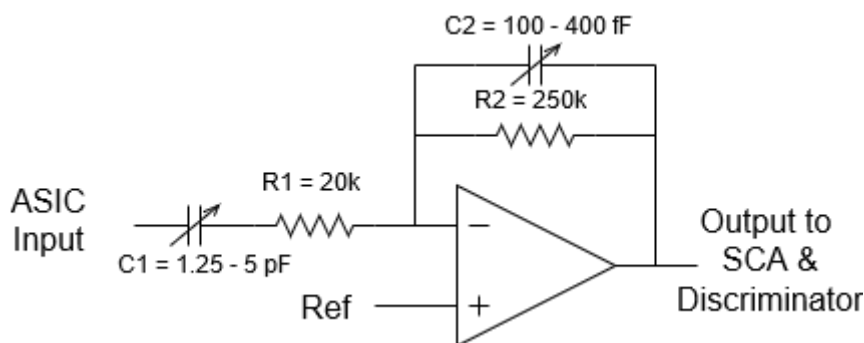


Figure 8 - CRRC shaper for charge measurement



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Slow Control Bit #609 – cf<1> 2.5 pf	Slow Control Bit #610 – cf<0> 1.25 pf	C1	R1	Tau: R1*C1
0	0	1.25 pF	20 kOhm	25 ns
0	1	2.5 pF	20 kOhm	50 ns
1	0	3.75 pF	20 kOhm	75 ns
1	1	5 pF	20 kOhm	100 ns

Slow Control Bit #607 – cf<3> 100 fF	Slow Control Bit #608 – cf<2> 200 fF	C2	R2	Tau: R2*C2
0	0	100 fF	250 kOhm	25 ns
0	1	300 pF	250 kOhm	75 ns
1	0	200 pf	250 kOhm	50 ns
1	1	400 pF	250 kOhm	100 ns

Table 3 - C1 & C2 Slow Control parameters for CRRC shaper

The output of the shaper is sent to a Switched Capacitor Array (SCA) along with a Track/Hold stage. The hold signal is generated internally from a delayed NOR32_time (Time Trigger) discriminator output. This “delay” resolution is 8-bit which can be set through Slow Control parameters bits #580 to #589. Characteristics of the trigger “delay” are the following:

- Slow Control bits : #589(MSB) - #580(LSB) – BCD coded
- Output delay : 27 – 115 ns with ~0.34ns/Delay Unit

The illustration of delayed trigger usage as hold signal for sampling the shaper output is shown in Figure 9. Once user have selected the appropriate “delay” (usually around the shaper peaking time), the shaper’s amplitude will be stored in the SCA and the can be converted to digital data via internal ADC of this ASIC.

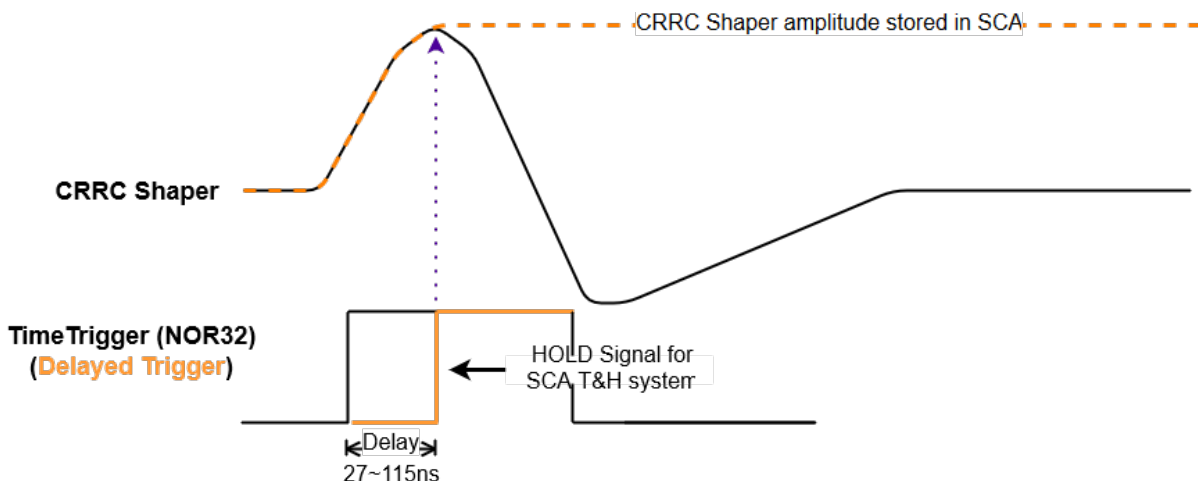


Figure 9 – Illustration of CRRC Shaper SCA track & Hold mechanism



3.3.1 Charge Trigger

In parallel with the SCA, the shaper output is sent to a charge discriminator whose threshold (Charge Threshold) is set by a common 10-bit DAC (vth_charge) the value of which can be changed with the Slow Control parameters (bits #554 to #563). Characteristic of this DAC is the following:

- Slow Control bits #554(MSB) - #563(LSB) – BCD coded
- Output : 1.01 – 2.01 V with ~0.92mV/DAC Unit

Charge trigger polarity and also channel-by-channel masking can be set through Slow Control parameters (Refer to Table 4 for more info) :

- mask_discri_charge_chx (bits #0 - #31) – mask the trigger output individually for each channel. '1' value will mask the trigger.
- cmd_polarity (bit #598) – selecting the trigger output polarity based on input signal. '0' for negative input signal, '1' for positive input signal.

The output of each discriminator is sent to an Open Collector output buffer in order to generate a NOR32 output (NOR32_charge - pin 122 or R19).



4 ASIC Back-end

4.1 Time measurement

Time-of-arrival of photon is done in two-step in Petiroc 2A. A coarse-time counter is clocked at 40 MHz. A ramp-based Time-to-Amplitude converter (TAC) is used to interpolate the “fine time” between two coarse time edges. This fine time interpolation principle is illustrated in Figure 11.

On each channel, the fine time measurement occurs as the following:

- The TAC ramp start is triggered by the discriminator (asynchronous signal) – Time Trigger
- The TAC ramp is stopped by the coarse counter clock (synchronous signal) running at 40 MHz. A metastability system allow to wait next clock tick if the discriminator signal is too close to the coarse time counter to remove metastability
- The TAC ramp final analogue level is converted by the Wilkinson ADC (Ramp ADC) during analogue to digital conversion phase in parallel with the 32 charge measurement

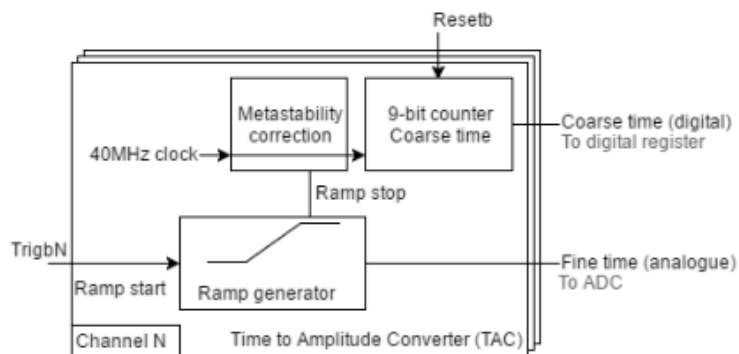


Figure 10 - Time measurement bloc scheme in Petiroc 2A



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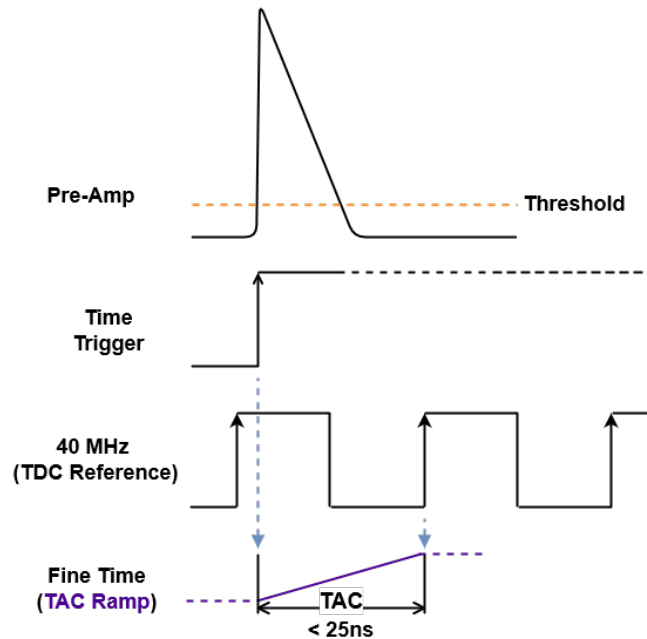


Figure 11 - Illustration of fine time measurement in Petiroc 2A

4.2 Digital read-out

The digital part manages the coarse time tagging, the internal ADC and the readout process.

For the time and also charge measurements, the following inputs are required on the digital side:

- 160 MHz clock (ck_160n/p - LVDS input at pin 106/107 or AA22/Y22)
- 40 MHz clock (ck_40n/p - LVDS input at pin 113/114 or V22/U22) – Synchronized to 160 MHz
- Reset input at high level (rstb - LVCMOS input at pin 137 or K19) – The initial reset phase (low level) duration could be in the order of a few hundred ns, then reset input should be set at high level all time during operation.
- Start conversion signal (start_conv - LVCMOS input at pin 126 or P22) – A high level pulse (> 100 ns) will initiate the analog-to-digital conversion for Fine time and Charge signal. This asynchronous signal has to be asserted after the ASIC triggers fired and all the analog signals are correctly sampled internally (refer to Figure 14).

The coarse time counter starts just after the release of the reset. The fine time and the coarse time information are needed to recover the real time of a hit channel.

First, start_conv input starts the analog to digital conversion and then it reads-out the data. The memory mapping of the transmitted data is given hereafter:



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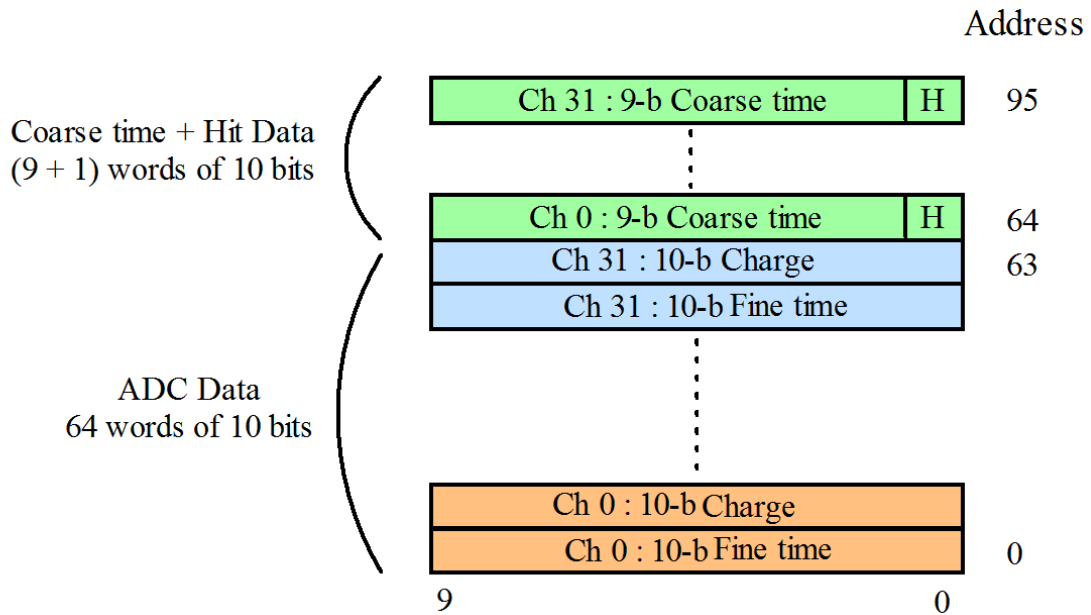


Figure 12 - Memory mapping

It is composed of 64 words of 10 bits from the ADC for the charge and the fine time measurements and 32 words of (9+1) bits from the 9-bit coarse time counter and the Hit information. Then, the readout frame is composed of 960 bits. All the data are encoded in gray format.

The readout process is done address 0 first and MSB first, so the first bit out is bit 9 of Channel 0 charge. The data are sent over the dout pin in single ended (dout – Open Collector output - pin 139 or J19) or in differential mode (doutn/p - LVDS outputs -pins 141/143 or K22/J22). The data on dout are valid when the transmission on (transmit_onb – Open Collector output - pin 145 or H22) is at a '1' logic level.

The data is transmitted at 80 MHz (160MHz system clock divided by 2 internally) or 12.5 ns per bit duration.

The schematic of the digital-to-analog conversion and readout system is provided in Figure 13.



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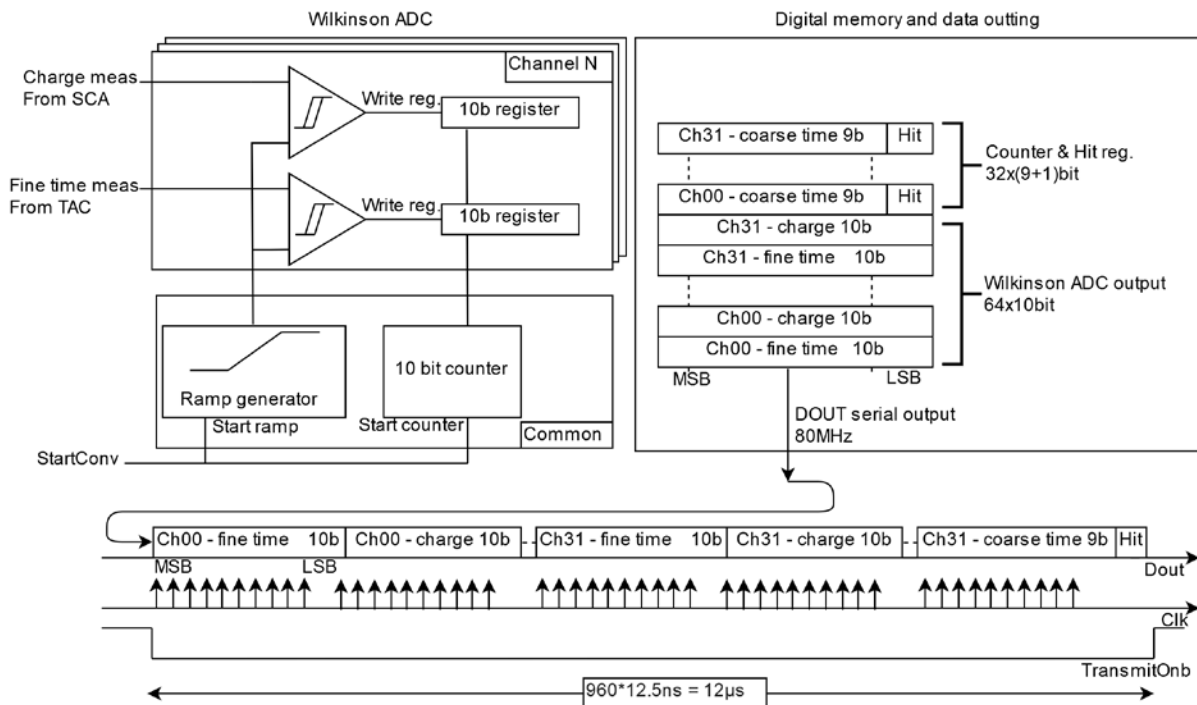


Figure 13 - Petiroc 2A digital read-out scheme

Illustration of the readout sequences for Petiroc 2A is shown in Figure 14. As stated at the beginning of this section, the readout will start once user sends Start Conversion (start_conv) input. As this signal is an asynchronous input, users will be interested to know when the ASIC is ready to convert the internal analog signals (Fine Time and Charge). In this case, various trigger outputs (trigb<0..31>, nor32_time & nor32_charge) can be used for triggering the readout sequences on the FPGA side and eventually assert the Start_Conv signal to the ASIC.

As the internal analog-to-digital conversion relies heavily on the trigger generation, especially Time trigger, user will have to ensure the trigger outputs are correctly configured and in latch mode (refer to Section 3.2.1) :

ASIC input :

- val_evt – (pin 116/118 or T19/T22) : This signal can be used as an acquisition window due to the LVDS input usage and its ability to mask trigger quickly. Set to '1' for validating the trigger outputs during the operations.

Slow Control parameters (Refer to Table 4 for more info) :

- mask_discri_time_chx (bits #328 - #359) – mask the trigger output individually for each channel. '1' value will mask the trigger. Mask on Figure 6.
- cmd_polarity (bit #598) – selecting the correct trigger output polarity based on input signal. '0' for negative input signal, '1' for positive input signal (Figure 7).
- DIS_razchn_int (bit #619) & DIS_razchn_ext (bit #620) – These bits are required to be set accordingly (bit #619 = '0' and #620 = '0') so that the internal "Razchn" or channel "reset" signal to reset the trigger latches. External "razchn" can be used only for specific cases : e.g. event rejection and no internal channel "reset" occurs.
- LatchDiscri (bit #599) – Using the internal time and charge measure, time trigger is required to be set in latch mode ('1'). Once the digital readout is done, the digital core will reset this latch for next measurement through "Razchn" signal.



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Once the readout is done, the acquired data can be converted to their respective measurements:

$$\text{Absolute Timing} = (\text{Coarse time} + 1) \times (\text{ck_40 period}) - (\text{Fine time})$$

With ck_40 is the TDC reference clock running at 40MHz and Fine time is about 37 ps/ADC Unit.

On the other hand, the charge will depend directly the on the shaping time selected for the CRRC shaper. The ADC used for the charge measurement has a dynamic range of 1 V with minimum of 1 V input and LSB of ~1 mV. The exact measurement of the ADC output vs equivalent input charge is presented in Section 7.7.



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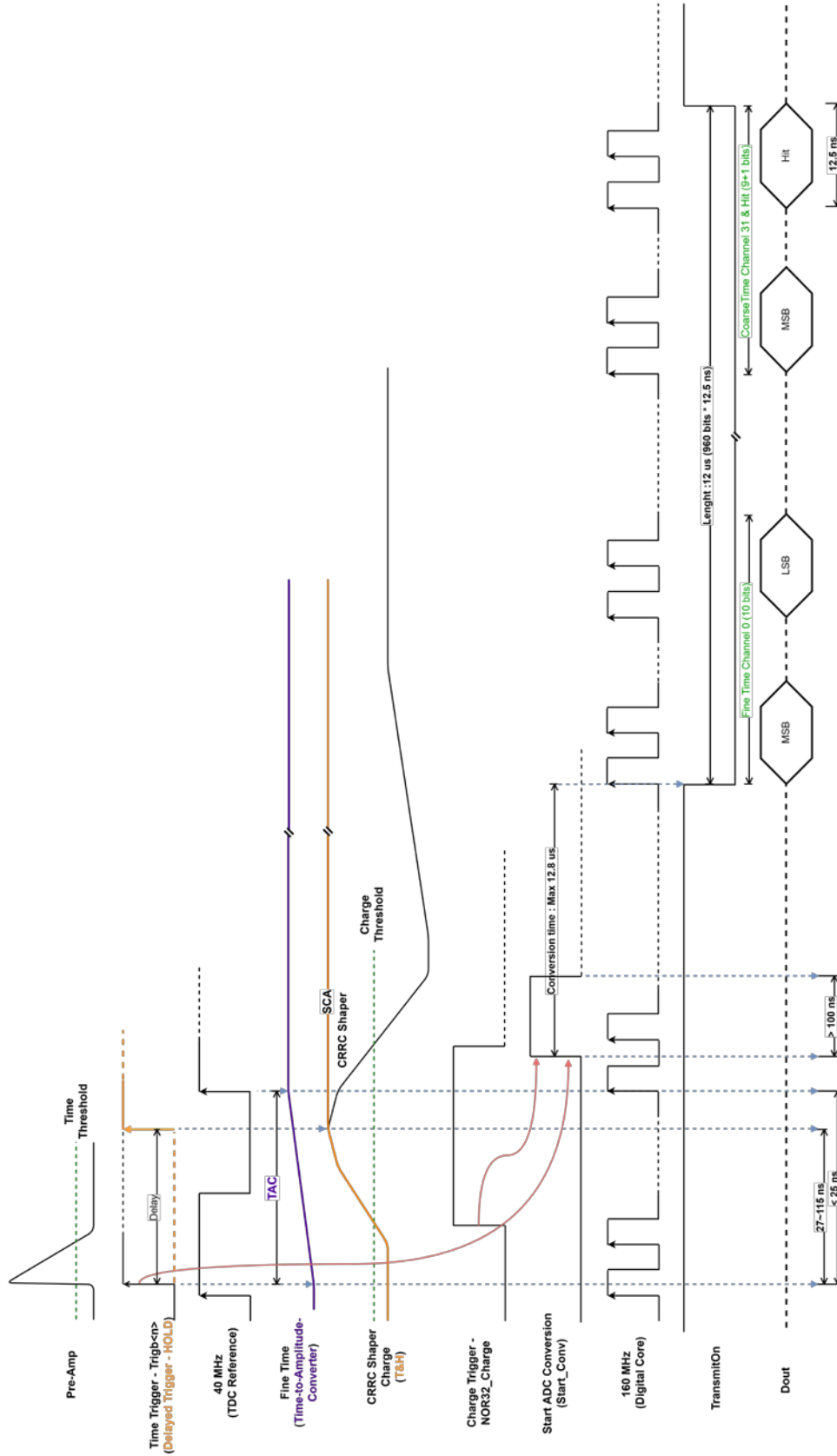


Figure 14 - Timing diagram of Petiroc 2A readout sequences



5 Petiroc 2A programmable parameters

Petiroc 2A is a programmable ASIC which is accessible through a set of I/Os (Figure 15). The program bit stream is called Slow Control as it allows the ASIC to be programmed with a set of parameter. The same interface for programming Slow Control register is also shared with Probe registers (Section 5.3) which is used for monitoring and debug. Finally, there is another set of register called Read register (Section 5.4) which is used for "analog" readout. This register has its own programming interface except for the register reset.

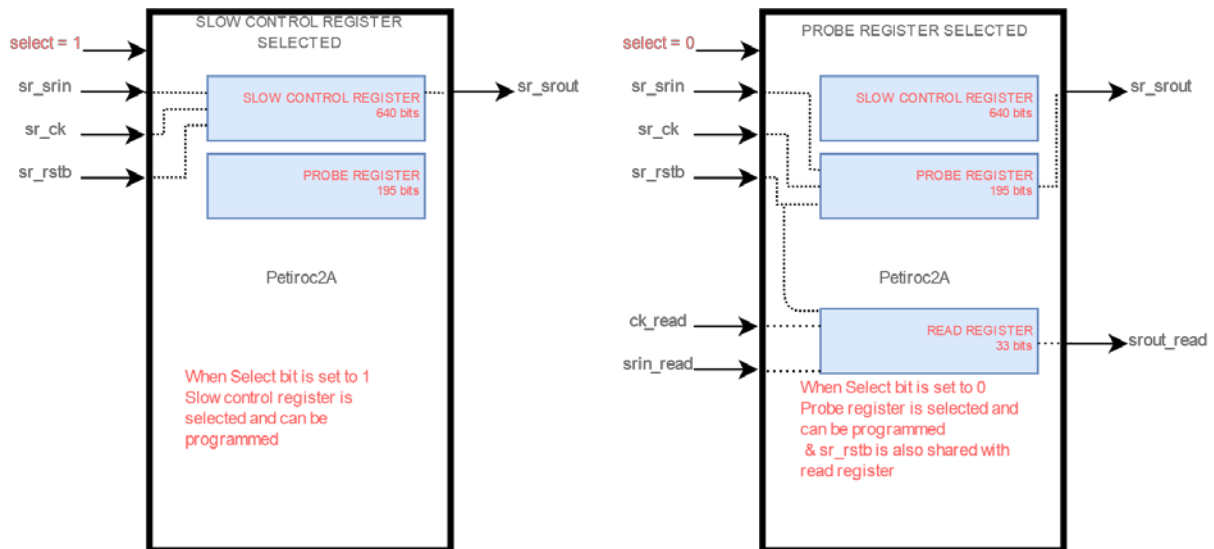


Figure 15 - Programmable parameters interface of the ASIC

5.1 General description

The Slow Control is a shift-register composed of 640 flip flops (first bit is B_0 = maskb_discri_charge_ch0 and last is B_{639} = EN_transmit). A timing diagram for a typical usage of the Slow Control register is illustrated in Figure 16. An input called select (pin 146 or H19) is used for selecting between Slow Control or Probe (refer to Section 5.3) registers. Asserting this input to high level ('1') will assign all the associated I/Os to Slow Control register.

The reset input (sr_rstb – pin 150 or F22) can be asserted asynchronously at low level. Although short pulses (e.g. 20 ns) is enough for resetting the register, it is recommended to assert this signal for at least 100 ns. The reset will configure the chip to default configuration (refer to Table 4) which is usable for a quick evaluation of the ASIC.

For configuring this chip with custom setting, the bit stream has to be shifted into the chip in similar way of using a shift register. Bit stream or data on sr_in (pin 154 or E22) input are sampled on rising edge of the clock (sr_ck – pin 148 or G22). Data are shifted at each clock cycle as seen on Figure 16. Typically the Slow Control clock frequency is recommended to be between 1 MHz to 5 MHz. The data has to be presented at the input so that the setup/hold (<5ns) time is respected. An easy way to respect this timing is to present the input at falling edge of the Slow Control clock and let the data to be sampled at the next rising edge of this clock.



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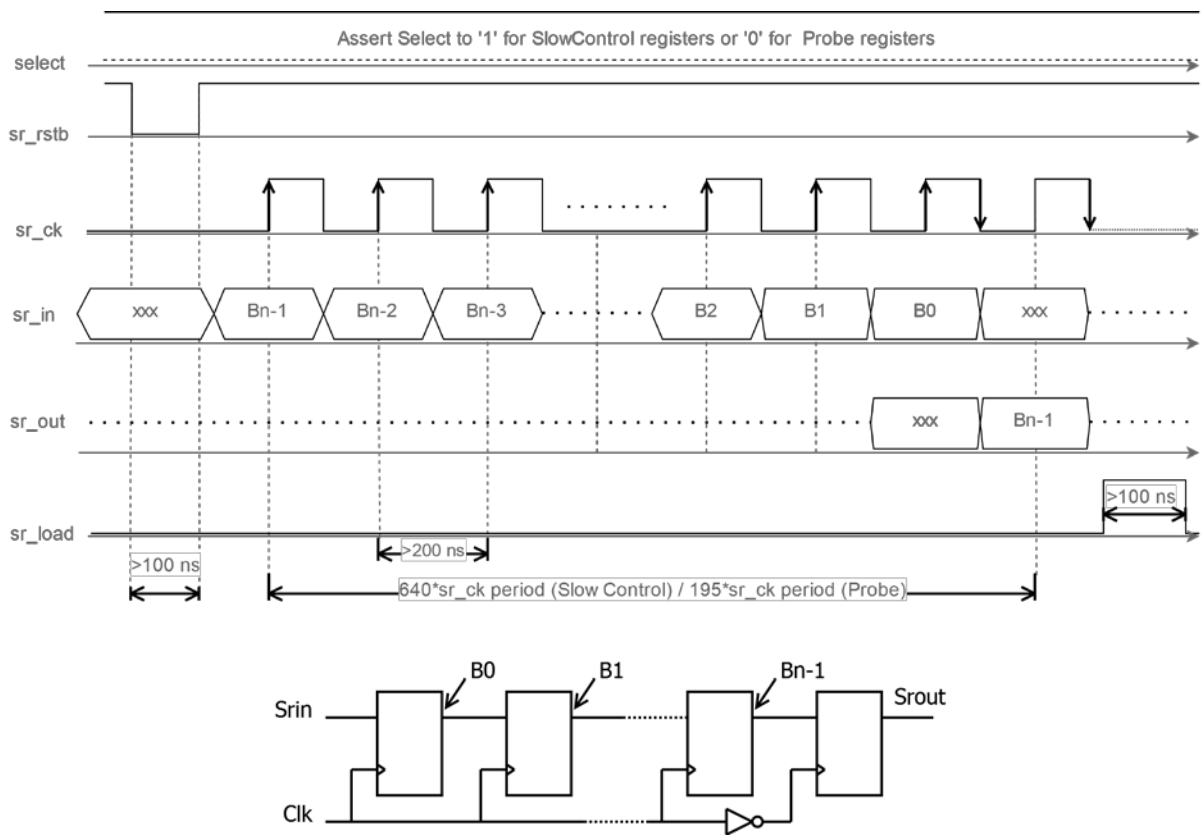


Figure 16 - Slow Control (and Probe) timing diagram and explanation.

Between the shift register output (sr_out – pin 152 or G19) and the output of the last slow control register’s flip flop, another flip flop clocked on falling edge implies that the last sr_out signal bit will be set on clock falling edge.

Only for validating the input DAC settings (Section 3.1 - SiPM High voltage trimming), an asynchronous high-level load signal (sr_load – pin 160 or B22) has to be asserted. For best practice, this signal is asserted at the end of Slow Control bits shift in for at least 100 ns.

Slow Control register can easily be daisy chained to allow a single serial programming stream to program several Petiroc 2A. This feature is very useful in case of large number of ASIC to program.



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5.2 Slow control register parameters

The 640 parameters in Petiroc 2A are described in the table below.

SC name	SC description	Bit #	Default value	ASIC operation mode		
				Photon Counting	Analog time & charge meas.	Full digital & charge meas.
mask_discri_charge_ch0	Mask of the charge discriminator (refer Section 3.3.1)	0	0, no mask	0	0	0
...	
mask_discri_charge_ch31		31	0, no mask	0	0	0
b0 input DAC ch0	LSB input DAC ch0 (refer to Section 3.1)	32	0	User custom value	User custom value	User custom value
...			
b7 input DAC ch0	MSB input DAC ch0 (refer to Section 3.1)	39	0			
cmd input DAC ch0	Enable input DAC for ch0	40	1 (active)	1	1	1
b0 input DAC ch1	LSB input DAC ch1 (refer to Section 3.1)	41	0	User custom value	User custom value	User custom value
...			
b7 input DAC ch1	MSB input DAC ch1 (refer to Section 3.1)	48	0			
cmd input DAC ch1	Enable input DAC for ch1	49	1	1	1	1
...
b0 input DAC ch31	LSB input DAC ch31 (refer to Section 3.1)	311	0	User custom value	User custom value	User custom value
...			
b7 input DAC ch31	MSB input DAC ch31 (refer to Section 3.1)	318	0			
cmd input DAC ch31	Enable input DAC for ch31	319	1	1	1	1
b0 input DAC dummy ch	LSB input DAC for dummy ch	320	0	User custom value	User custom value	User custom value
...			
b7 input DAC dummy ch	MSB input DAC for dummy ch	327	0			
mask_discri_time_ch0	Mask of the time discriminator (refer to Section 3.2.1)	328	0, no mask	0	0	0
...	
mask_discri_time_ch31		359	0, no mask	0	0	0
b0 6bDAC Ch0	LSB for 6-bit Time Threshold trimming – CH0 (refer to Section 3.2.1)	360	0 (Def =000000)	User custom value	User custom value	User custom value
...			
b5 6bDAC Ch0	MSB for 6-bit Time Threshold trimming – CH0 (refer to	366	0			



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Section 3.2.1)						
...
b0 6bDAC Ch31	LSB for 6-bit Time Threshold trimming – CH31 (refer to Section 3.2.1)	367	0		User custom value	User custom value
...		User custom value	User custom value
b5 6bDAC Ch31	MSB for 6-bit Time Threshold trimming – CH31 (refer to Section 3.2.1)	551	0		User custom value	User custom value
EN_10bit_DAC	Enable 10bit DAC	552	1 (ON)	1	1	1
PP_10bit_DAC	Power Pulsing mode 10b DAC	553	0 (ON)	0	0	0
b9_vth_discr charge	MSB for 10-bit DAC for Charge Threshold (refer Section 3.3.1)	554	0 (Def = 0100000000)		Not required	User custom value
...		Not required	User custom value
b0_vth_discr charge	LSB for 10-bit DAC for Charge Threshold (refer Section 3.3.1)	563	0		Not required	User custom value
b9_vth_time	MSB for 10-bit DAC for Time Threshold (refer to Section 3.2.1)	564	0 (Def = 0100000000)		User custom value	User custom value
...		User custom value	User custom value
b0_vth_time	LSB for 10-bit DAC for Time Threshold (refer to Section 3.2.1)	573	0		User custom value	User custom value
EN_ADC	Enable for internal ADCs	574	1 (ON)	0	0	1
PP_ADC	Power Pulsing mode for internal ADCs	575	0 (ON)	0	0	0
sel_startb_ramp_ADC_ext	Select internal or external ADC ramp start command	576	0 (internal ramp start)	0	0	0
usebcompensation	ADC ramp compensation	577	0	0	0	0
EN bias DAC_delay	Enable for Time trigger delay mechanism (DAC stage)	578	1 (ON)	0	1	1
PP bias DAC_delay	Power pulsing for Time trigger delay mechanism (DAC stage)	579	0 (ON)	0	0	0
EN bias ramp_delay	Enable for Time trigger delay mechanism (ramp)	580	1 (ON)	0	1	1



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	generation)					
PP bias ramp_delay	Power pulsing mode for trigger delay mechanism (ramp generation)	581	0 (ON)	0	0	0
b0 DAC delay	LSB for Time Trigger delay (refer to Section 3.3)	582	0 (Default =00000000)	Not required	User custom value	User custom value
b1 DAC delay	Bit(1) of Time Trigger delay (refer to Section 3.3)	583	0			
...	...					
b7 DAC delay	MSB for Time Trigger delay (refer to Section 3.3)	589	0			
EN_discri_delay	Enable for Time trigger delay mechanism (Discriminator)	590	1 (ON)	0	1	1
PP_discri_delay	Power pulsing mode for Time trigger delay mechanism (Discriminator)	591	0 (ON)	0	0	0
EN_temp_sensor	Enable for internal temperature sensor	592	1 (ON)	0	0	0
PP_temp_sensor	Power pulsing mode for internal temperature sensor	593	0 (ON)	0	0	0
EN_bias_pa	Enable for preamplifier stage	594	1 (ON)	1	1	1
PP_bias_pa	Power pulsing mode for preamplifier stage	595	0 (ON)	0	0	0
EN_bias_discri	Enable for Time Trigger discriminator	596	1 (ON)	1	1	1
PP_bias_discri	Power pulsing mode for Time Trigger discriminator	597	0 (ON)	0	0	0
cmd_polarity	Trigger polarity selection according to input polarity (refer to Section 3.2.1)	598	0 (negative input signals)	User choice	User choice	User choice
LatchDiscri	Latch mode for Time Trigger (refer to Section 3.2.1)	599	0 (no latch)	0	1	1
EN_bias_6bit_DAC	Enable for 6-bit Time Threshold trimming	600	1 (ON)	1	1	1
PP_bias_6bit_DAC	Power pulsing mode for 6-bit Time Threshold trimming	601	0 (ON)	0	0	0



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EN_bias_tdc	Enable for time-to-digital converter	602	1 (ON)	0	0	1
PP_bias_tdc	Power pulsing mode for time-to-digital converter	603	0 (ON)	0	0	0
ON/OFF input DAC	Enable for input DACs	604	1 (ON)	1	1	1
EN_bias_charge	Enable for charge measurement CRRC shaper	605	1 (ON)	0	1	1
PP_bias_charge	Power pulsing mode for charge measurement CRRC shaper	606	0 (ON)	0	0	0
Cf<3> 100fF	CRRC shaper feedback capacitor : C2 (Figure 8) - Value : Table 3	607	0, DEF= 250k, 100fF	Not required	User choice	User choice
Cf<2> 200 fF		608	0, DEF= 250k, 100fF			
Cf<1> 2.5pF		609	0, DEF= 20K, 1.25pF			
Cf<0> 1.25pF		610	0, DEF= 20K, 1.25pF			
EN_bias_sca	Enable for CRRC shaper analog memories and T&H	611	1 (ON)	0	1	1
PP_bias_sca	Power pulsing mode for CRRC shaper analog memories and T&H	612	0 (ON)	0	0	0
EN_bias_discri_charge	Enable for Charge Trigger discriminator	613	1 (ON)	0	1	1
PP_bias_discri_charge	Power pulsing mode for Charge Trigger discriminator	614	0 (ON)	0	0	0
EN_bias_discri_ADC_time	Enable for Time ADC discriminator	615	1 (ON)	0	0	1
PP_bias_discri_ADC_time	Power pulsing mode for Time ADC discriminator	616	0 (ON)	0	0	0
EN_bias_discri_ADC_charge	Enable for charge ADC discriminator	617	1 (ON)	0	0	1
PP_bias_discri_ADC_charge	Power pulsing mode for Charge ADC discriminator	618	0 (ON)	0	0	0
DIS_razchn_int	Disable internal Razchn	619	0(Enable)	0	1	0
DIS_razchn_ext	Enable external Razchn	620	1 (Disable)	1	0	0
SEL_80M	Select 160MHz clock from input or	621	1 (160MHz/2 stage)	Not required	Not required	1



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	through division by 2 stage					
EN_80M	Enable 160MHz clock division by 2 → 80MHz (for readout)	622	1 (enable division)	Not required	Not required	1
EN_slow_lvds_rec	Enable for LVDS receiver for Razchn external and ValEvt	623	1 (ON)	1	1	1
PP_slow_lvds_rec	Power pulsing mode for LVDS receiver for Razchn external and ValEvt	624	0 (ON)	0	0	0
EN_fast_lvds_rec	Enable for clocks LVDS receiver	625	1 (ON)	0	0	1
PP_fast_lvds_rec	Power pulsing mode for clocks LVDS receiver	626	0 (ON)	0	0	0
EN_transmitter	Enable for LVDS transmitter	627	1 (ON)	0	0	1
PP_transmitter	Power pulsing mode for LVDS transmitter	628	0 (ON)	0	0	0
ON/OFF_1mA	Current strength for LVDS transmitter 1mA+1mA	629	1 (ON)	0	0	1
ON/OFF_2mA	Current strength for LVDS transmitter 1mA+2mA	630	1 (ON)	0	0	1
NC		631	0	0	0	0
ON/OFF_ota_mux	Enable preamplifier output buffer	632	1 (ON)	0	1	0
ON/OFF_ota_probe	Enable analog signal monitoring output buffer	633	0 (OFF)	0	0	0
DIS_trig_mux	Enable Time Trigger multiplexer	634	0 (Enable)	User choice	User choice	User choice
EN_NOR32_time	Enable Time Trigger NOR32 output	635	1 (Enable)	User choice	User choice	User choice
EN_NOR32_charge	Enable Charge Trigger NOR32 output	636	1 (Enable)	0	User choice	User choice
DIS_triggers	Enable Time Trigger 32 channel outputs	637	0 (Enable)	0	0	0
EN_dout_oc	Enable single ended data output on open collector output	638	1 (Enable)	0	0	User choice
EN_transmit	Enable transmit on data on open collector output	639	1 (Enable)	0	0	1

Table 4 – Slow Control register parameters



5.3 Probe register parameters

A probe register is integrated for debugging or for user to see internal ASIC test points. Two main probe outputs are available: one for digital signal (digital_probe, pin 155 or D22), one for analogue signal (analog_probe, pin 165 or A19). Additionally, an output for measuring input DAC is also available (out_inpDAC_probe, pin 48 or AB6). It should be noted that, only one analogue and one digital signal can be probed at a time. The purpose of that probing system is for development and debugging and should not be used in system configuration, except if an internal signal is required for a specific application.

This probe register is based on the same flip-flop architecture as the Slow Control registers described previously. It shares the same data input pin (sr_in), output pin (sr_out), reset pin (sr_rstb) and clock pin (sr_clk) as the Slow Control registers. A select signal allows choosing the register to be used. When select is set to "1", the Slow Control register is selected, when select is set to "0", the probe register is selected. The timing diagram shown Figure 16 is valid for probe register except for the usage of "load_sr" input which is only required for Slow Control.

Signal name	Probe	Comments	Probe outputs	Bit #
out_inpDAC_probe	32	Output of the 32 channels 8-bit input DAC	Analog out_inpDAC probe (pin 48 or AB6)	0
out_time/vth_discri	64	32 channels preamp output and Time threshold including the 6-bit trimming	Analog probe (pin 165 or A19)	32
out_time_dummy	1	Preamp output of the dummy channel	Analog probe (pin 165 or A19)	96
out_ramp_tdc	32	output of the 32 TAC ramps	Analog probe (pin 165 or A19)	97
out_discri_charge/ out_charge	64	output of the 32 ch Charge trigger and CRRC shapers	Digital probe (pin 155 or D22)	129
startRampbADC_int	1	Internal start of the ADC ramp	Digital probe (pin 155 or D22)	193
holdb	1	Internal hold signal (delayed Time trigger). Active Low	Digital probe (pin 155 or D22)	194

Table 5 – Probe register parameters

5.4 Read register for analogue readout

Petiroc 2A can be used in several read-out mode. In analogue charge measurement mode, the 32 analogue outputs are outted using an analog multiplexer. The read register is used to multiplex and output the charge measurement after the Switched Capacitor Array of each of the 32 channels as well as the output of the temperature sensor (out_charge_mux, pin 168 or A18) and the multiplexed Time trigger outputs (trig_mux, pin 120 or R22). Reading out the signal has to be done sequentially and only one channel can be readout at one time for each output. Therefore the input of the register has to be presented at high level only for 1 clock cycle and each clock rising edge will activate a channel output starting from channel 0.

The interface this register not shared with other register except for the reset :

- Reset : rstb_read (from sr_rstb) – pin 150 or F22 → This low-level asynchronous input (> 20 ns) will reset the register to zero and deactivate all channel outputs.
- Data in: srin_read – pin 173 or E15 → Active only for 1 clock cycle and data is sampled on the clock rising edge
- Clock : ck_read – pin 172 or A17 → The clock frequency is dominated by analog output buffer settling time : 100 – 200 ns. Frequency lower than 5 MHz is preferable.



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- Data out : srou_read – pin 171 or E16 → Data output is presented on the clock falling edge. So that when daisy chaining with other chip, setup/hold violation can be avoided especially if the data is sampled on clock rising edge.

The read registers can be daisy chained as well as the analog outputs.

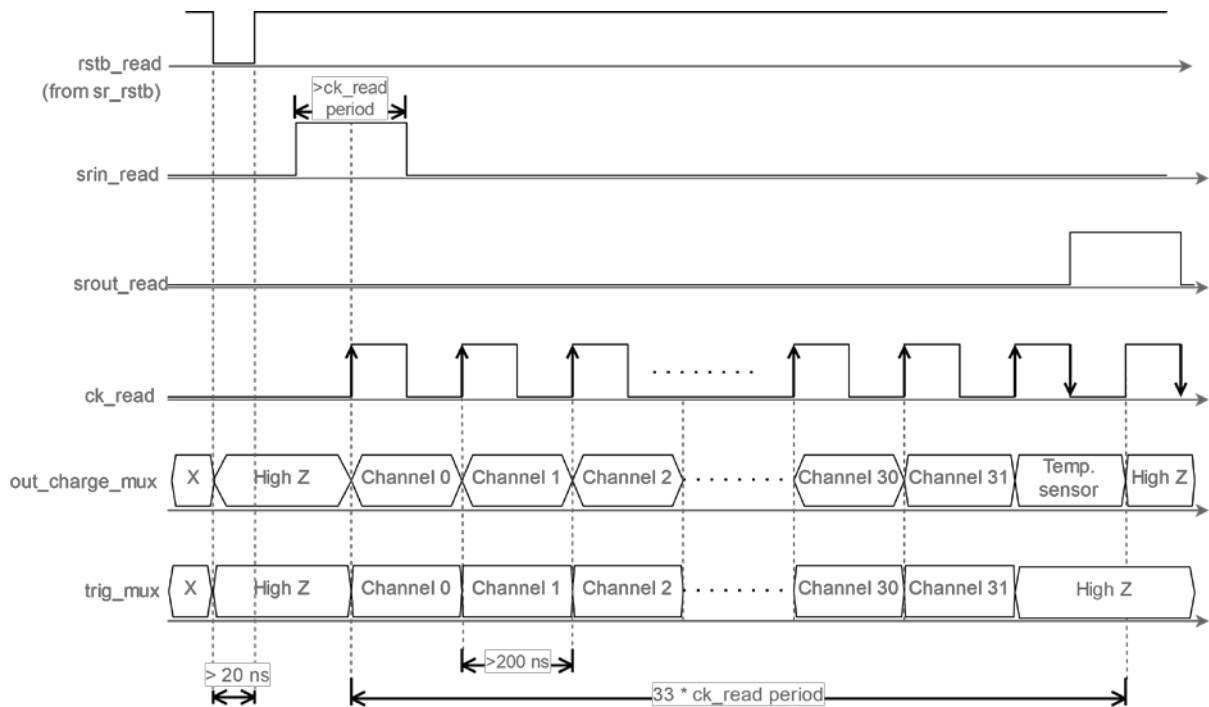


Figure 17 - Read register timing diagram

Signal name	Comments	Charge output	Bit #
out_sca	32 Multiplexed output of the 32 SCA of CRRC shaper (Section 3.3)	Analog (out_charge_mux)	0
out_temp_sensor	1 Temperature sensor	Analog (out_charge_mux)	32

Signal name	Comments	Digital output	Bit #
trigb	32 Multiplexed output of the 32 trigger outputs	Digital (trig_mux)	0 - 32

Table 6 – Read register parameters



5.5 Power Pulsing

Each unused stage can be disabled to reduce power consumption. This is controlled by the Slow Control bits called "EN_bloc-name" (EN= enable). Moreover, each chip stage can be switched off dynamically thanks to the "power_on" command (pwr_on_x provided by pin 88/90/92/94 or W15/W16/AC19/W17– refer to Table 8 and Figure 50). This mode is the power pulsing function (Figure 18): for each stage, the slow control bit called "PP_bloc-name" (PP=Power Pulsing) allows bypassing this feature by forcing it ON. (Refer to the truth table – Table 7).

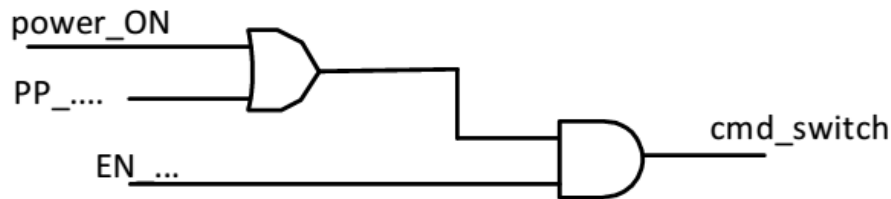


Figure 18 - Power Pulsing control logic

En_...	Parameter	PP_...	Parameter	Power_ON_x pin	Cmd_switch	Comments
0	X	X	X	X	0	Stage disabled – Forced OFF
1	1	1	X	X	1	Stage disabled – Forced ON
1	0	0	1/0	1/0	1/0	Power pulsing mode

Table 7 – Power Pulsing logic truth table



6 ASIC I/Os connections

6.1 Front-end connection

The preamplifier is a voltage amplifier. A 200 ohm in series with a 100pF is integrated inside the chip for each channel. This resistor value can be reduced by adding smaller resistor value (between ASIC input and ground) for each input channel. The SiPM detector can be connected directly to the input of the chip. An illustration of the front-end connections is shown in Figure 19 (for SiPM positive polarity signal).

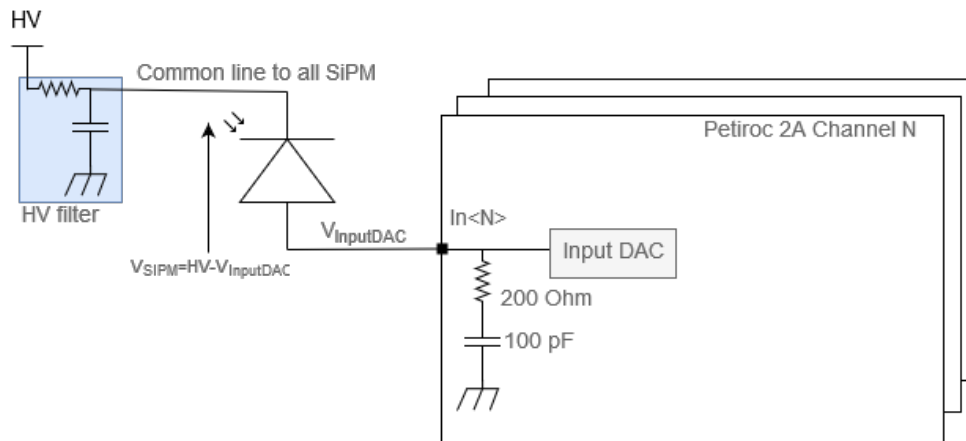


Figure 19 -Petiroc 2A inputs connections to the SiPM

6.2 Backend connection

The connections of the 32 triggers (Trigb <0:31>) and NOR outputs are shown in Figure 20. The output corresponds to the direct discriminator output or to the latched discriminator output depending on the value of the slow control parameter "LatchDiscri" (Bit #599 - Table 4). They are outed through an embedded output buffer. High level (One) and Low level (Zero) voltage value are set on system design with driver power pins VHigh (VH) and VLow (VL). No external component is required. It is strongly recommended to always set Vlow(VL) to ground.

A multiplexed trigger output (Trig_MUX) is available on pin 120 or R22 when the slow control parameter "DIS_trig_mux" (Bit #634 - Table 4) is set to 0. Just like for the triggers, this output is also sent through a buffer powered by VH and VL. Refer to Figure 22 for trigger multiplexer connection and to Section 5.4 for the readout.

The NOR32_time signal is a 32-input NOR of the Time triggers and it is active low as soon as one of the 32 Time trigger fires. This signal is available on pin 123 or P19. It is outputted through an Open Collector (OC) buffer. A 200k Ohm resistor is connected internally between the drain of the OC buffer transistor and the VH power supply (3.3V). The user can add a smaller resistor (down to 50 Ohm – 1 kOhm recommended) outside the chip if needed.

In a similar way for charge triggers, a 32-input NOR is also available at NOR32_charge (pin 122 or R19). This 32NOR output is also active low if any of 32 channels charge trigger is active. A 200k Ohm resistor is also available internally at the buffer output and VH power supply (3.3V). User can add external resistor down to 50 Ohm (1 kOhm recommended) in parallel to the internal resistor if required.



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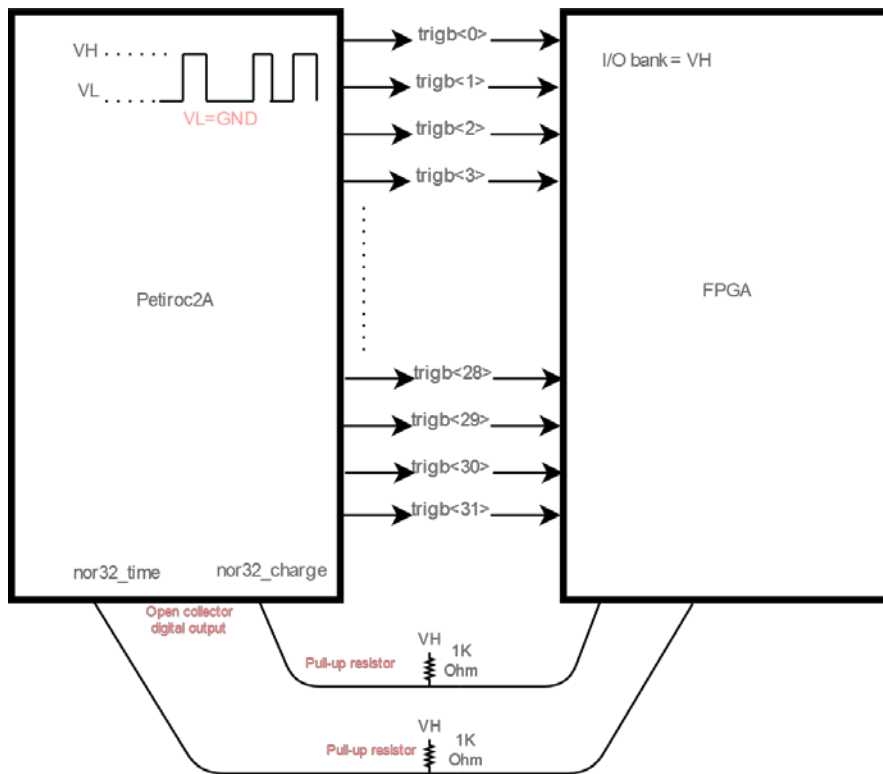


Figure 20 - Triggers and NOR32 connections to FPGA

The Charge measurement and Time measurement for each channel are coded internally over 10 bits. The data transmission I/Os connections are shown in Figure 21. These coded data are available on dout (pin 139 or J19). They are outputted through an internal Open Collector buffer. As there is no internal resistor, an external resistor (100 Ohm) must be added between this pin and the power supply if this output is used. Alternatively, user can also use the corresponding LVDS data outputs which are available on pin 141 or K22 (dout_n) and pin 143 or J22 (dout_p). In this case, a 100 ohm termination resistor must be added between these differential outputs on the receiver side.

During the transmission of the coded data, a transmit_ONb signal is generated by the chip. This signal is available on pin 145 or H22. It is buffered internally by an Open Collector buffer. As there is no internal resistor, an external resistor (100 Ohm) must be added.



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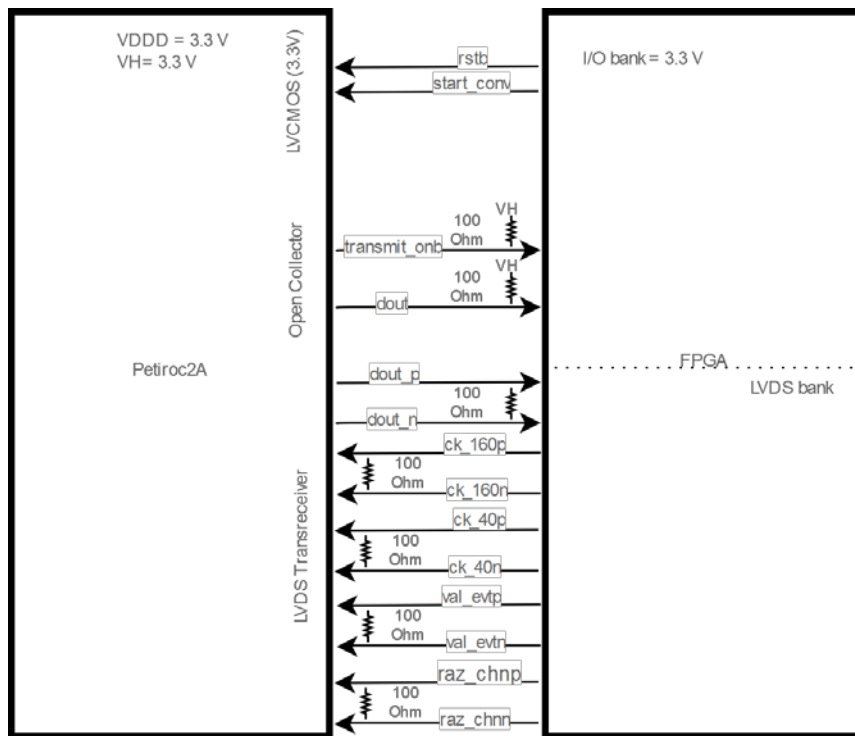


Figure 21 - Data transmission I/Os connections between Petiroc 2A and FPGA

Other digital control signals such as digital core reset and start conversion are available at `rstb` (pin 137 or K19) and `start_conv` (pin 126 or P22) respectively. These are standard point-to-point connections which can be connected directly FPGA with 3.3V I/O bank. For LVDS differential inputs such as Channel reset (`raz_chnn/p` : pin 109/111 or W22/U19) and Event validation (`val_evtn/p` : pin 116/118 or T19/T22), a 100 ohm resistor must be placed near to the ASIC between the differential inputs. As for the clocks, 160MHz (`ck_160n/p` : pin 106/107 or AA22/Y22) and 40 MHz (`ck_40n/p` : pin 113/114 or V22/U22), a 100 ohm resistor must be placed close to the ASIC between the LVDS differential inputs for the clocks. Refer to Section 4.2 for data transmission description.

The connections of the read and probe register outputs are shown in Figure 22. A multiplexed charge output as well as the output of the temperature sensor is available at `out_charge_mux` (pin 168 or A18). This output can be connected directly to an ADC, external analog buffer or oscilloscope.

The output of the analog probe is available at `analog_probe` pin 165 or A19. Depending on the probe register, the output of each of the 32 preamplifiers as well as the threshold set for each of the 32 time discriminators, the 32 TDC ramps and the 32 charge outputs can be seen and checked for debug purpose.



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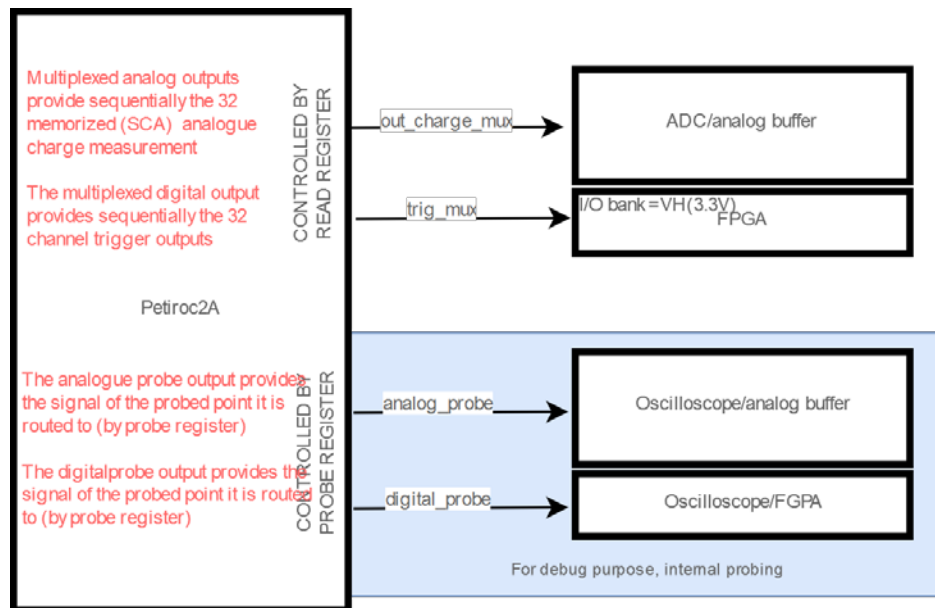


Figure 22 - Probe and analog read connections

The output of the digital probe is available at dig_probe (pin 155 or D22). Depending on the probe register, the 32 charge discriminators as well as the internal StartRampbADC signal and the internal HOLDb signal can be seen and checked for debug purpose.

The connections for controlling the Slow Control, Probe and Read registers are shown in Figure 23. All these pins have to be connected directly from the FPGA bank with 3.3V I/Os. For the accessing the Slow Control/Probe register, these I/Os are required (refer to Section 0 and 5.3) :

- Select register : select – pin 146 or H19
- Reset : sr_rstb – pin 150 or F22
- Data in: sr_in – pin 154 or E22
- Clock : sr_ck – pin 148 or G22
- Data out : sr_out – pin 152 or G19
- Load : sr_load – pin 160 or B21

For accessing the read register, the I/Os required are the following (refer to Section 5.4) :

- Reset :rstb_read (from sr_rstb) – pin 150 or F22
- Data in: srin_read – pin 173 or E15
- Clock : ck_read – pin 172 or A17
- Data out : srou_read – pin 171 or E16



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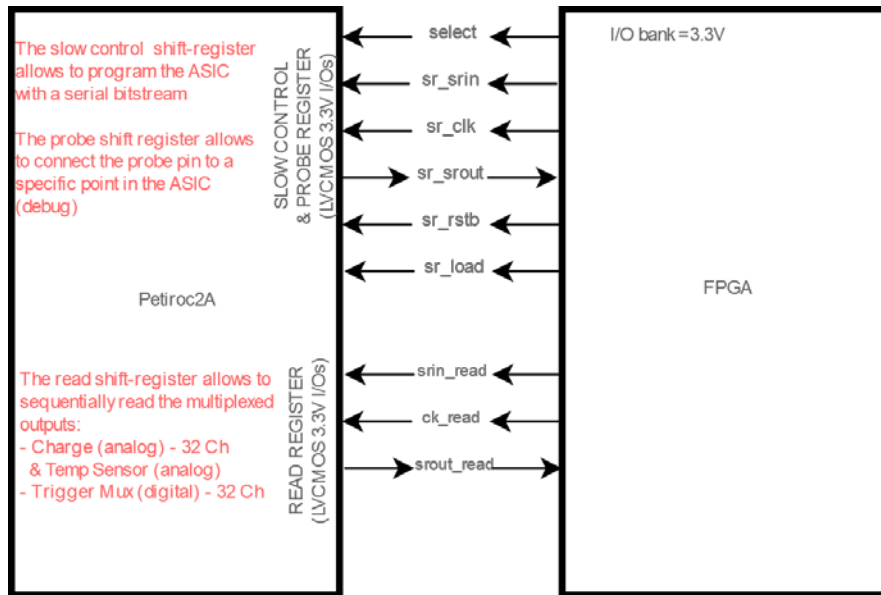


Figure 23 - Slow Control, Probe and Read registers control connections



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6.3 Supplies, references, biases

As shown in the Table 8 describing the pinout of the ASIC in LQFP 208 package, there are specific power supply for each block, noted vdd_cellname. The power supplies are separated inside the chip to avoid couplings. However, all the power supplies can be gathered and connected to a common vdd=3.3V (decoupled with 100nF) **except for vdda_time which must be connected to a specific vdda=3.3V** filtered with a RC filter (1 Ohm, 1µF) and except for the power supplies of the digital blocks vddd and vddd2 which can be connected together to a specific vddd=3.3V (with a 100nF decoupling capacitor).

The power supply VH can be set from 1.2V to 3.3V. VL must be connected to the ground.

As for the ground pins (gnd_cell) and vss (substrate), they need to be connected to the general ground of the board.

The bias voltages (ib_cell) and reference voltages are made internally and are available on pins. Their values are given in Table 8. No external component is necessary on these points. It is possible to add a decoupling capacitance on these points.

As for the TFBGA package, the 3.3V power supplies have been separated in to 3 domains: VDDI, VDDA and VDDD. VDDI is the most sensitive power supply here as it is powering the analog front end pre-amplifiers. For VH & VL, the recommendation is similar to the LQFP package. Lastly, there are 2 NC pins which are recommended to be grounded due to their proximity with the NOR32 outputs of the Time and Charge triggers.

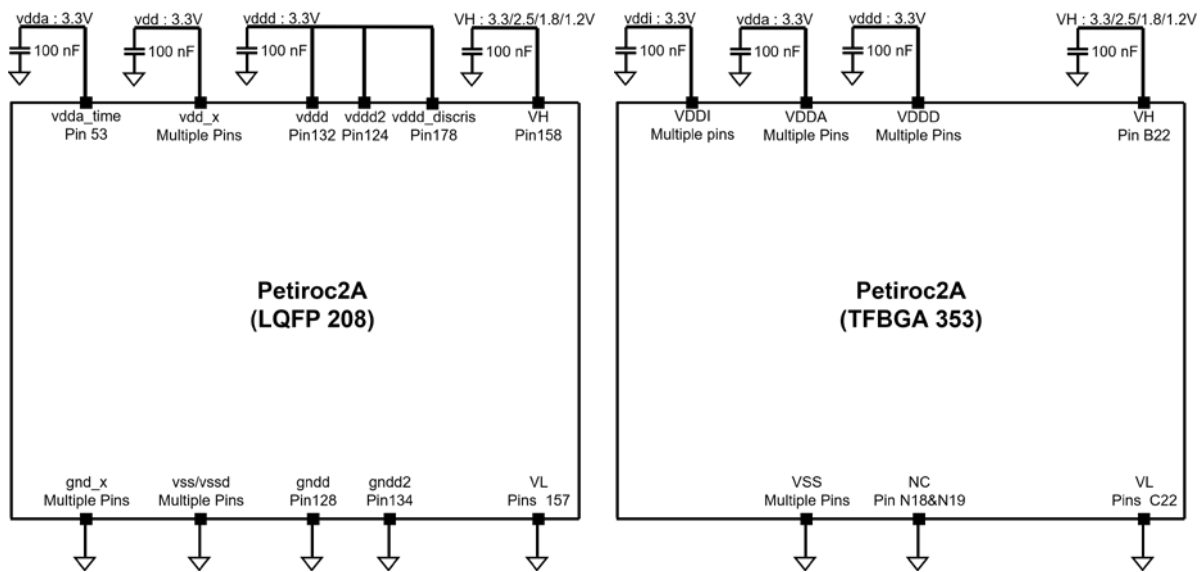


Figure 24 -Power supply recommendations for LQFP 208 (left) and TFGA 353 (right)



7 ASIC performance

7.1 Input DAC

The input DAC of each channel can be set changing the SC parameters (Slow Control bits #32 to #327). This linearity of the 32 channels has been measured. The average value of the slope is 4 mV/DAC unit.

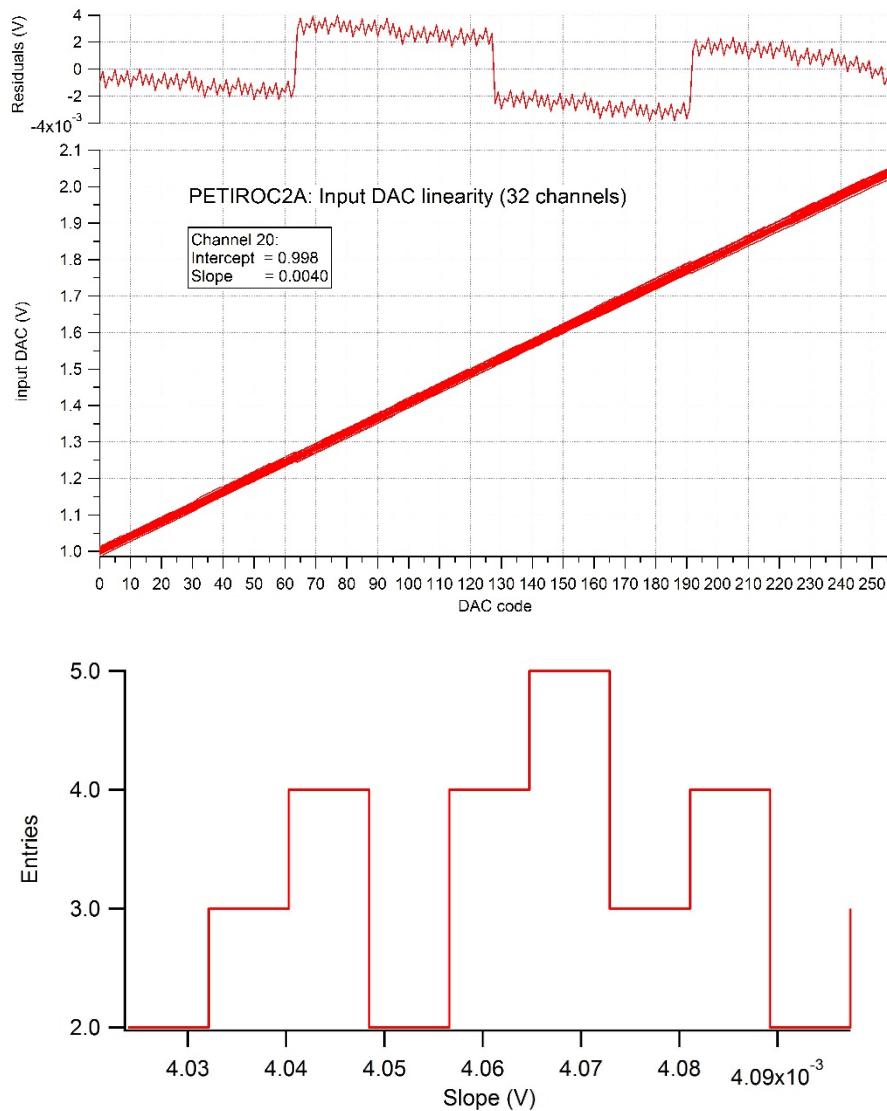


Figure 25 – 32 input DAC linearity with slope and intercept dispersion

7.2 10bit-DAC for time and charge thresholds

Two 10-bit DAC are integrated to set two different thresholds: one for the time discriminator and the other one for the charge discriminator. The time threshold (v_{th_time}) can be set using the Slow Control bits #564 to #573. The charge discriminator threshold can be set using the Slow Control bits #554 to #563.

The linearity of these two DACs has been measured. The time DAC has a slope of around 900 $\mu\text{V}/\text{DAC}$ unit and an intercept of around 900 mV. The charge DAC has a slope of around 900 $\mu\text{V}/\text{DAC}$ unit and an intercept of around 1 V.

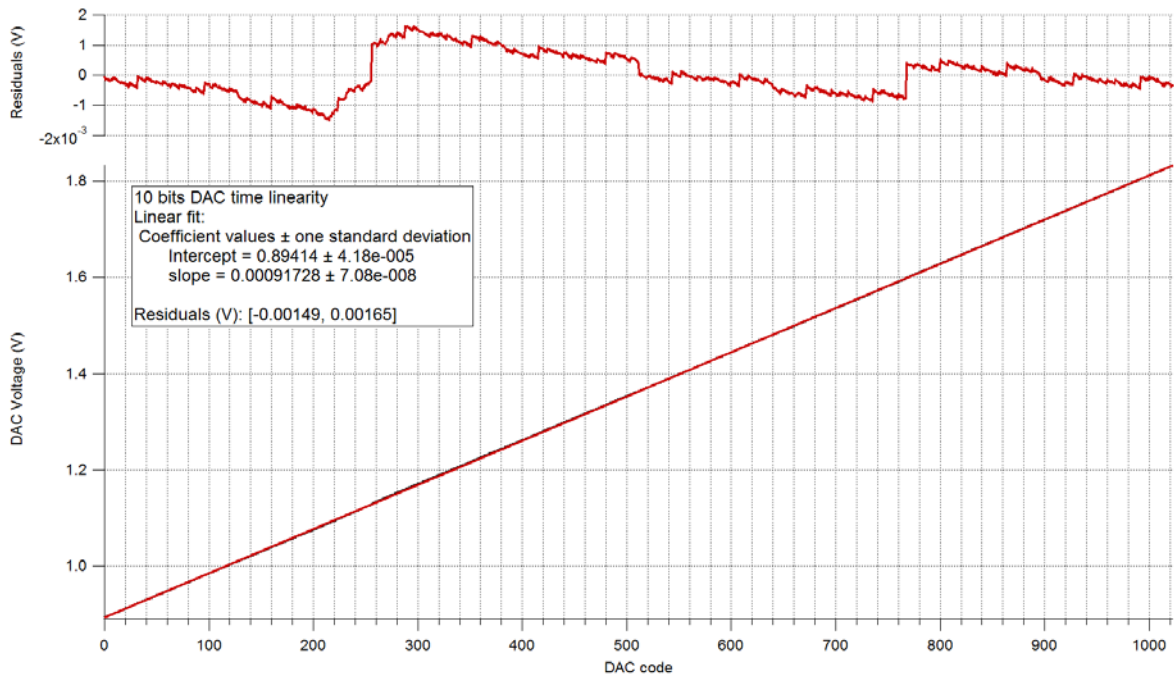


Figure 26 – 10-bit Time DAC linearity

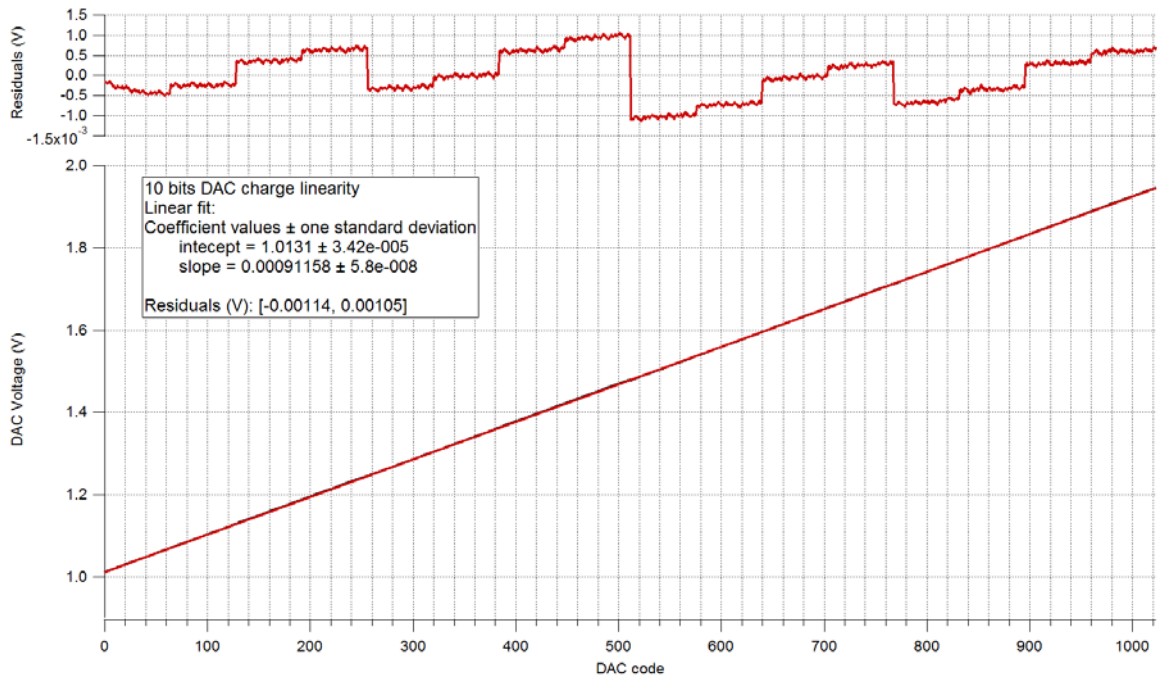


Figure 27 – 10-bit Charge DAC linearity

7.3 6-bit DAC linearity

An individual 6-bit DAC per channel is added at the output of the common 10-bit DAC to perform a fine adjustment of the threshold of each channel (Slow Control bits #360 to #551). The linearity of the 32 6-bit-DAC (vth_discr_time) has been measured. The slope is -1.5 mV/DAC Unit.



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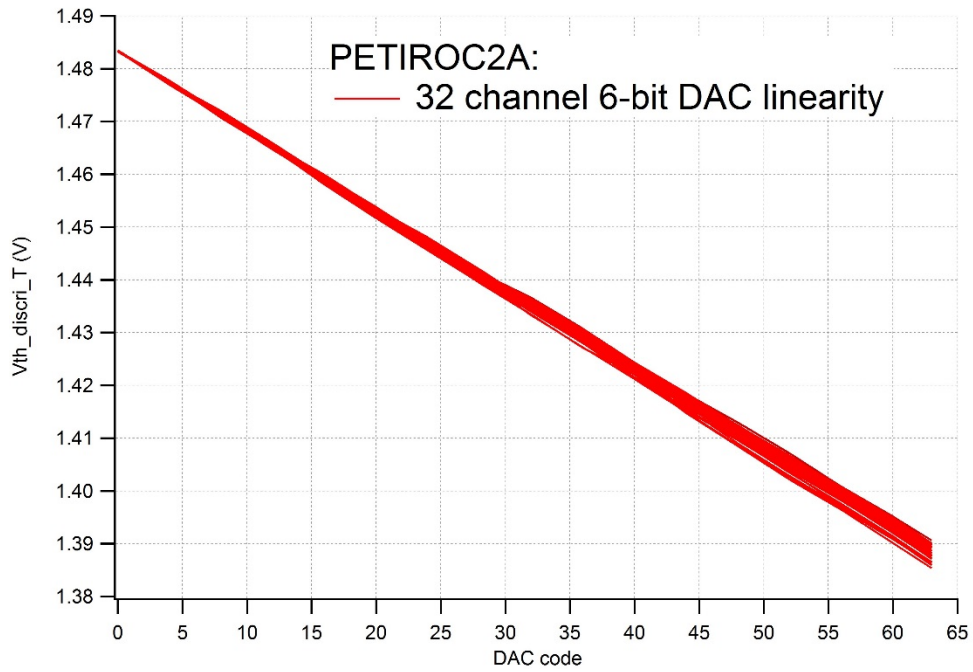


Figure 28 - 6-bit Time threshold trimming linearity



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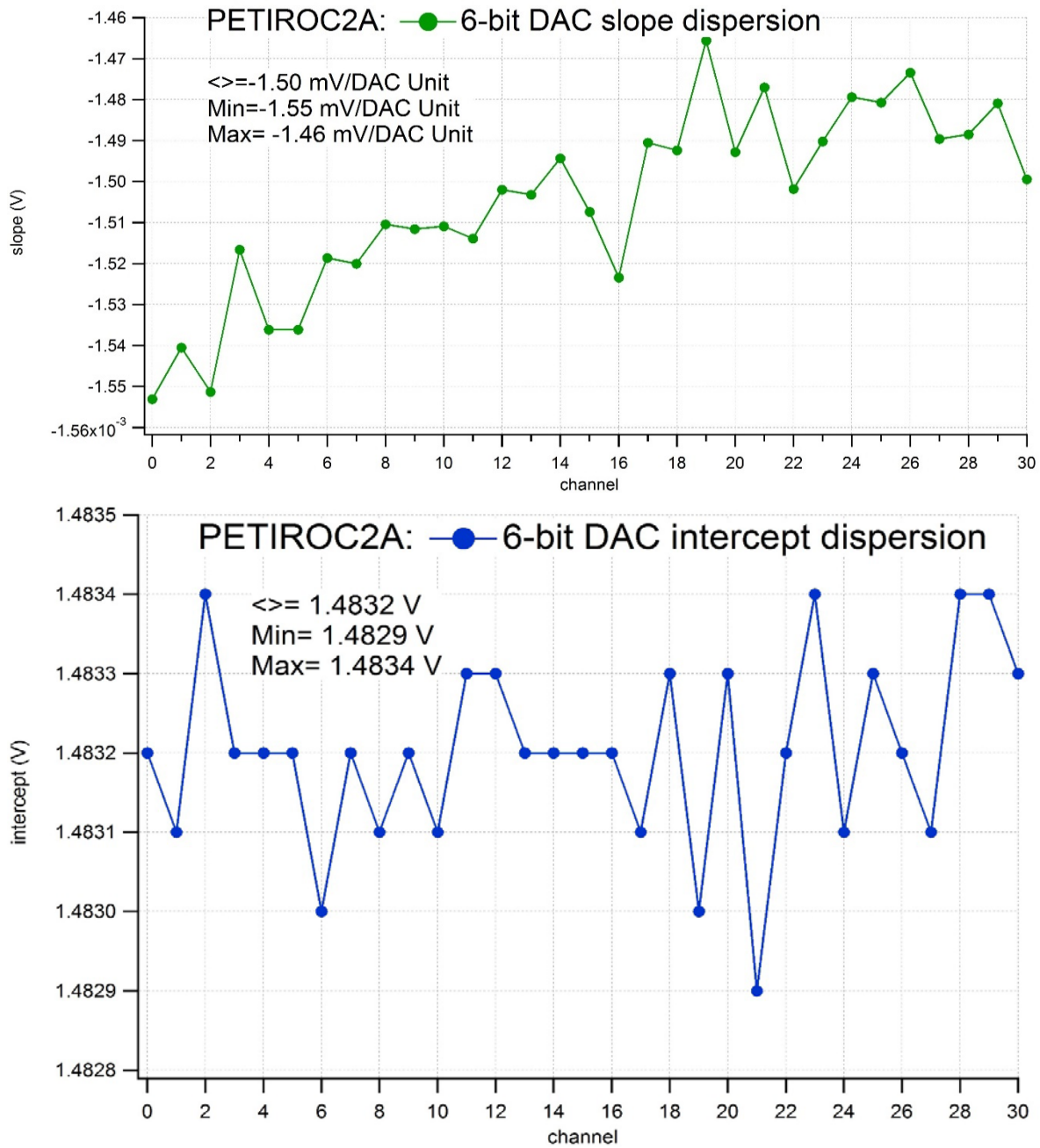


Figure 29 – 32 6bit DAC linearity with slope and intercept dispersion

This 6-bit DAC correction is used to correct the pedestal dispersion between channels. A measurement performed on one chip showed that the dispersion can be reduced within one DAC Unit.

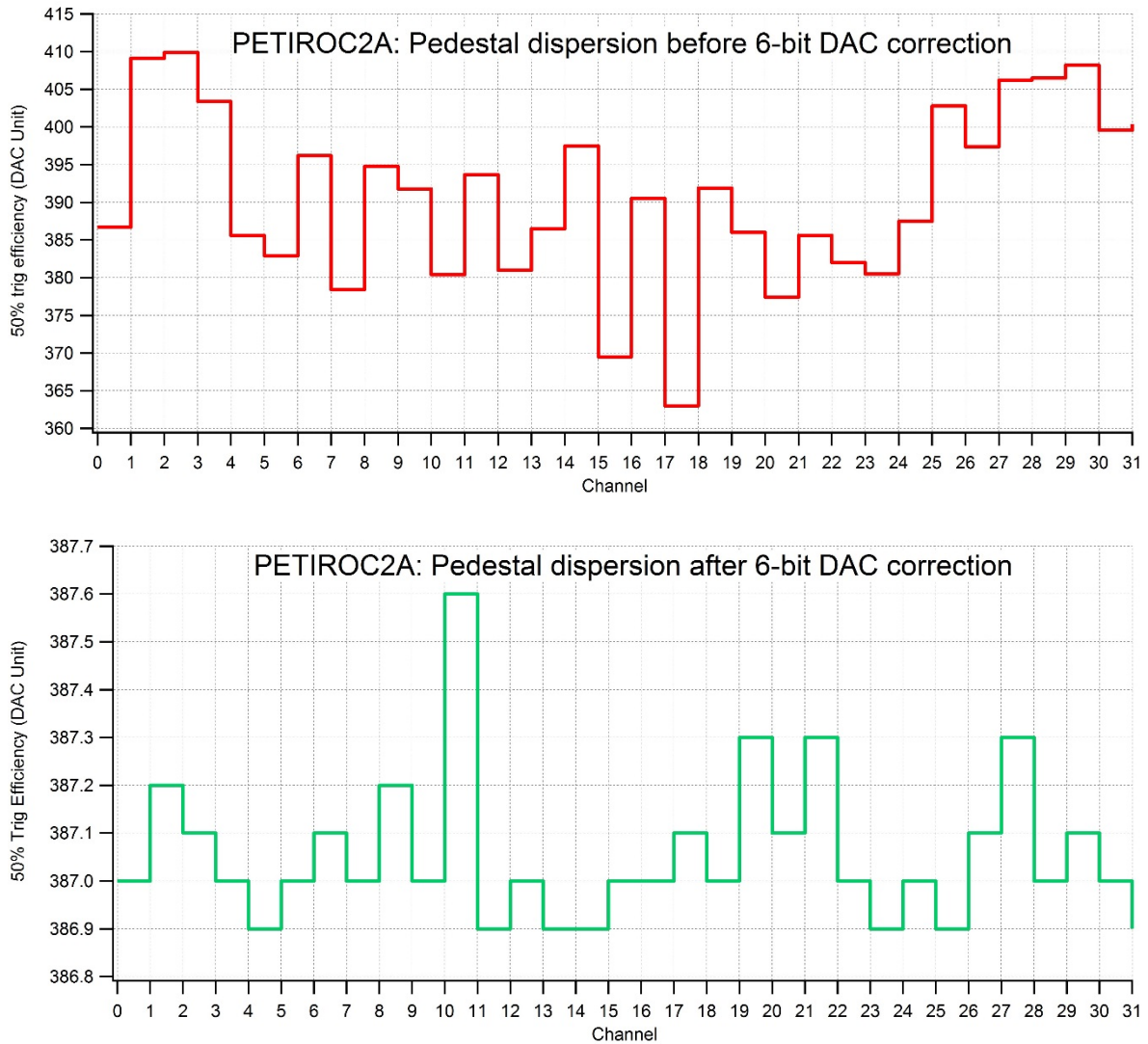


Figure 30 – 50% trigger efficiency point before and after 6-bit DAC correction

7.4 Trigger efficiency measurements

The setup used for the gain and trigger efficiency measurement is shown on Figure 31. One photoelectron corresponds to 160 fC with an injection capacitor of 100pF. The injection capacitor, C_{inj} , simulates the SiPM capacitor.



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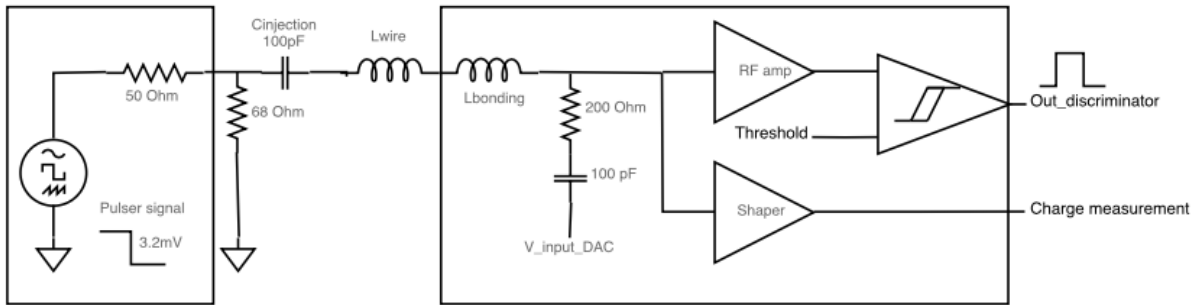
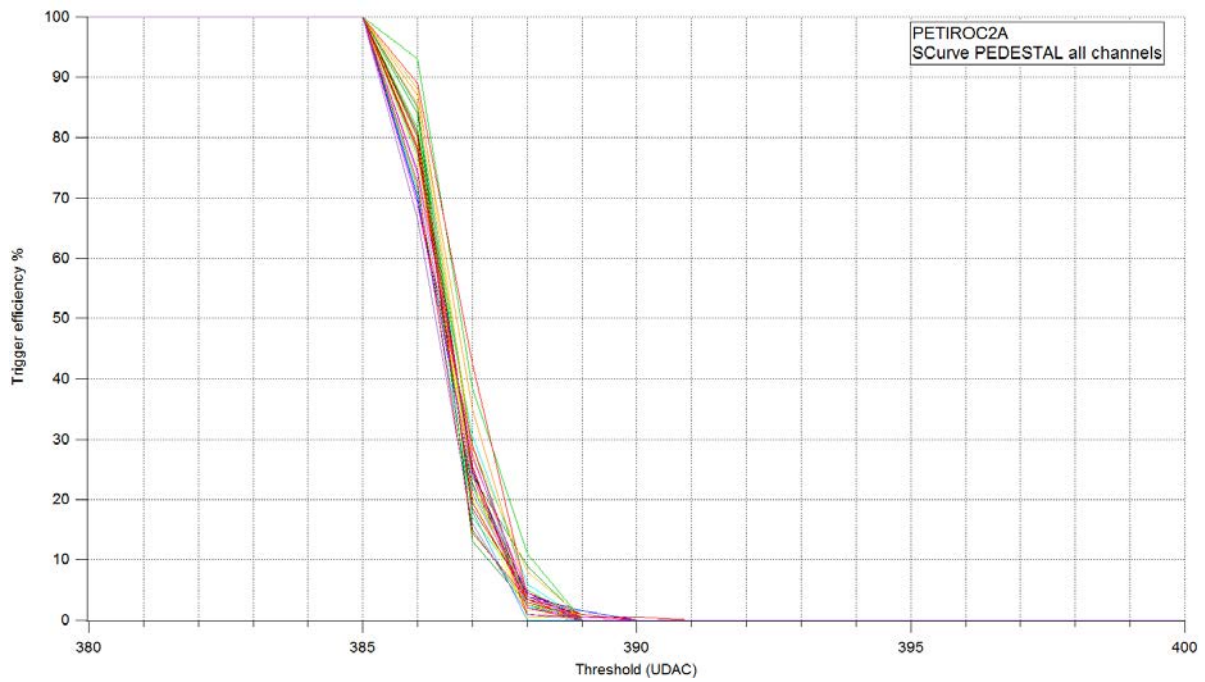


Figure 31 – SETUP for gain measurements

Using the 6-bit DAC correction, Scurves measurements have been performed on the 32 channels when 0 (pedestal), 1, 2 and 3 pe- are injected.





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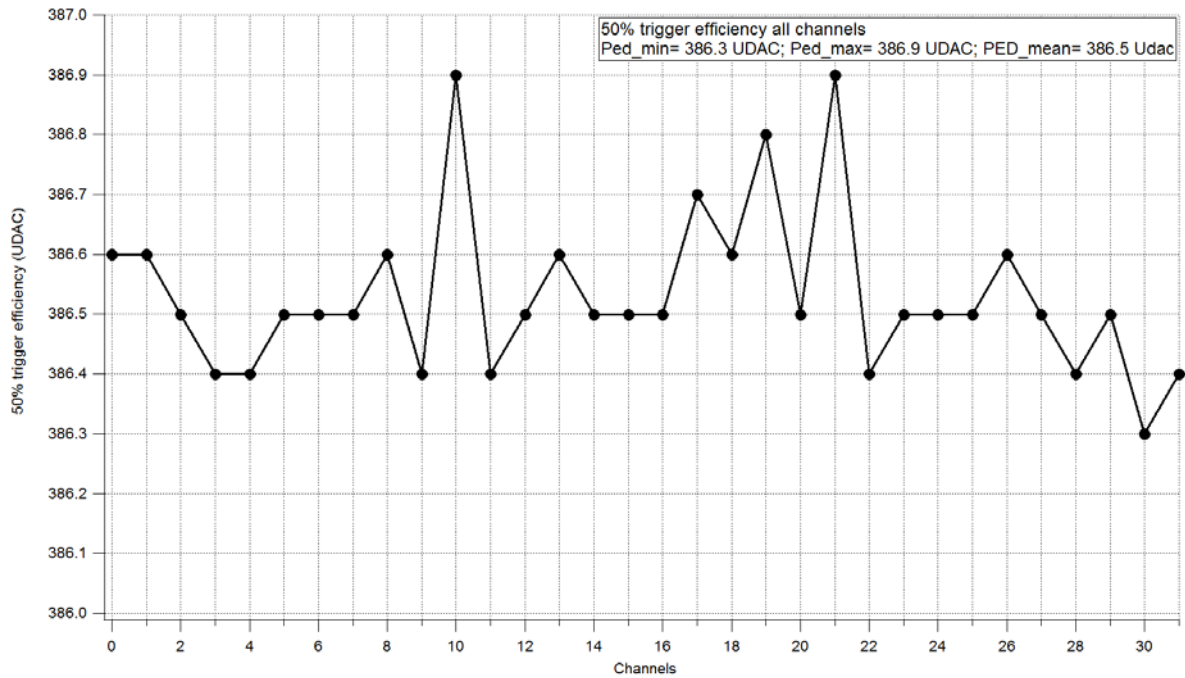
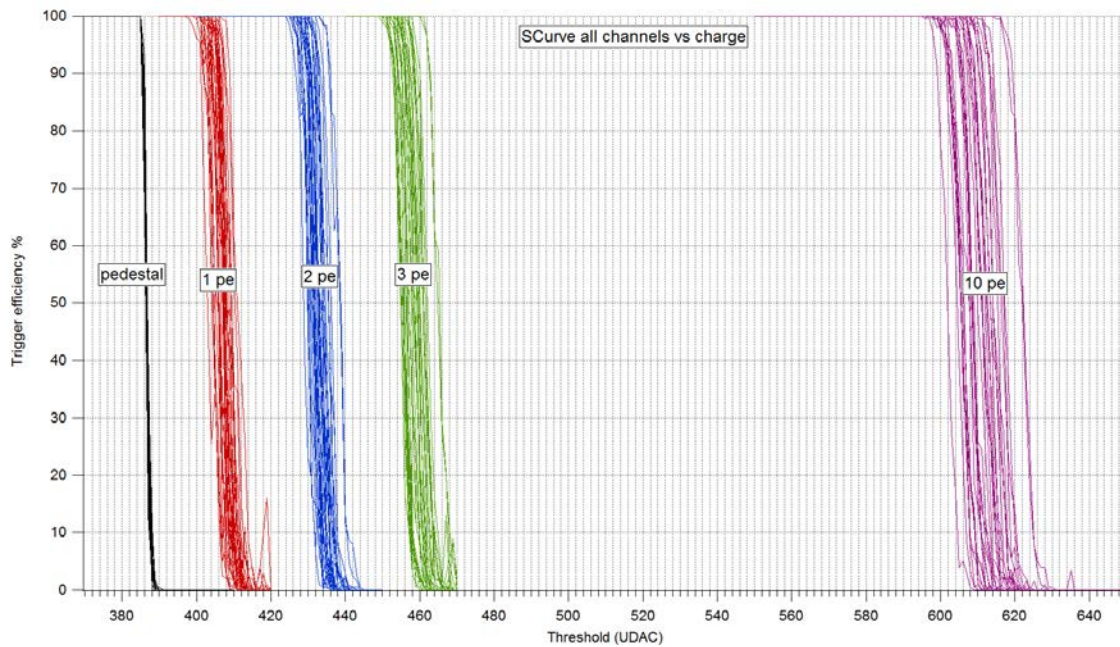


Figure 32 – 32 channel pedestal Scurve and dispersion



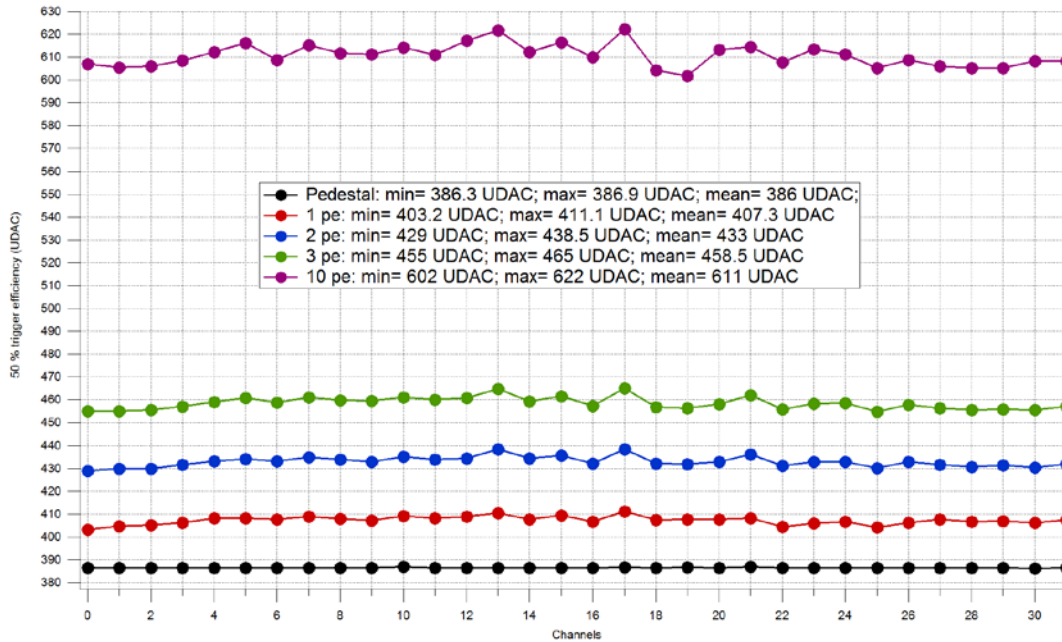


Figure 33 – 32 channel Scures

7.5 8-bit delay system

In fact, an 8-bit DAC is use to set the timing delay of Time trigger between 25 ns to 130ns, which can be selected to match the peaking time/maximum selected for the CRRC slow shaper. The linearity of this DAC has been measured and reported in Figure 34. The slope is around 4 mV/DAC unit and an intercept is around 1 V.

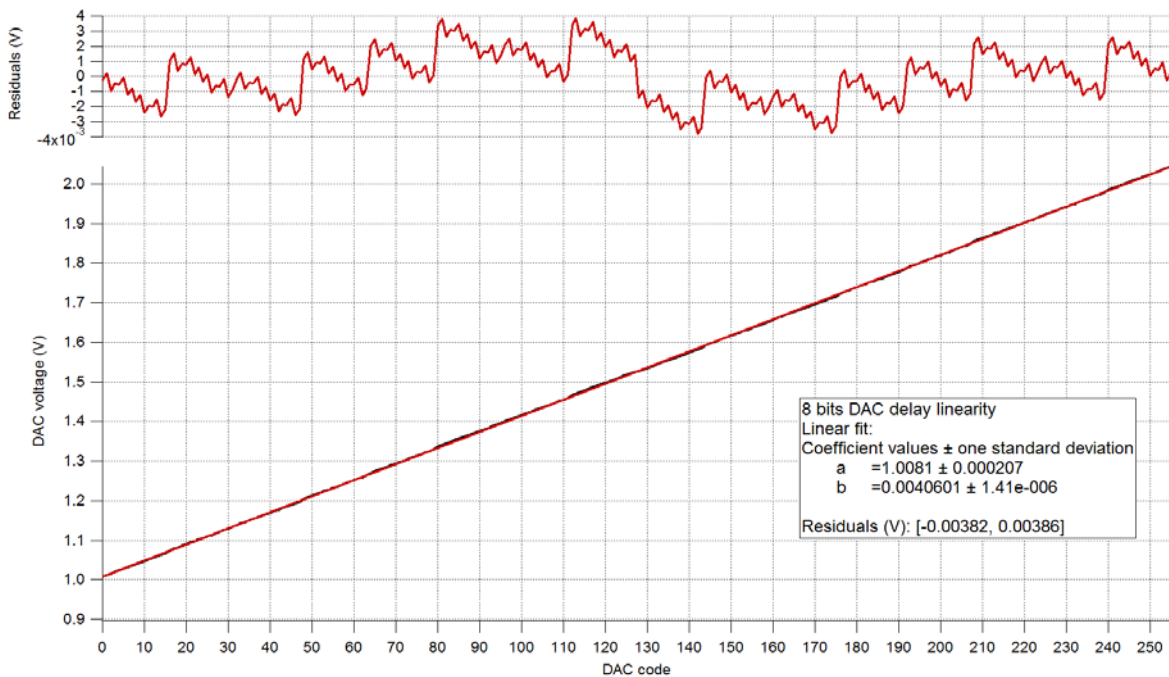


Figure 34 – 8 bit delay DAC linearity



This threshold is sent to a discriminator. The linearity of the delay has been measured equal to 0.34ns/DAC Unit, which is in a good agreement with the simulation.

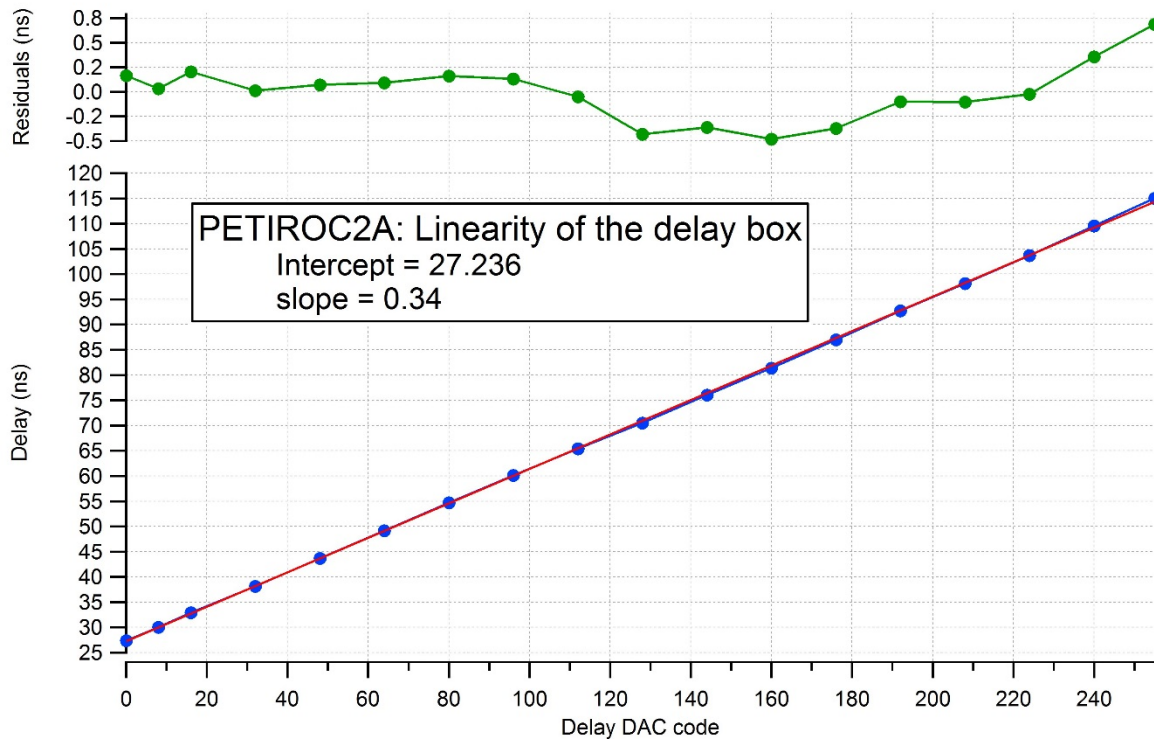


Figure 35 – delay linearity

7.6 Time measurement (Bandwidth and Jitter)

The setup used for time measurements is shown in Figure 36.

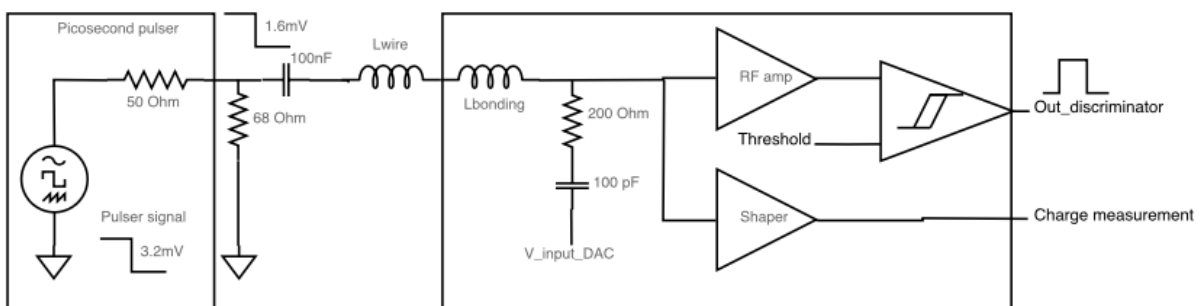


Figure 36 – SETUP for time measurements



The bandwidth at the output of the discriminator has been measured higher than 1.2GHz.

Jitter measurements were performed with a threshold set to 0.5 pe. It is around 10 ps for charge injection bigger than 3 pe- and when the 40MHz and 160MHz clocks are OFF. The 40MHz and 160MHz clocks generate couplings through the substrate and so degrade the jitter performance up to 40ps as shown in the plot below.

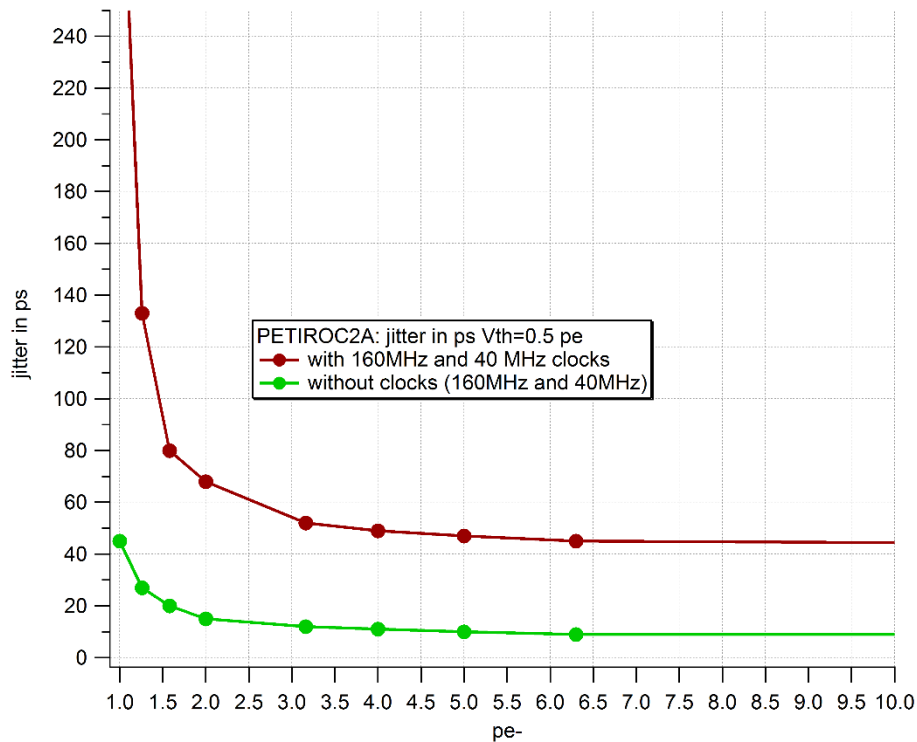


Figure 37 – Trigger Jitter measurement

7.7 Charge measurement

A charge measurement using the internal ADC has been performed with various injection capacitors (100 pF, 200 pF and 500pF) to simulate the SiPM charge @ gain 10^6 . The slow shaper settings for these measurements are: $C_1 = 1.25$ pF, $C_2 = 400$ fF. The linearity with $C_{inj} = 100$ pF is less than ± 3 UADC up to 1600 p.e.; with $C_{inj} = 200$ pF is less than ± 3 UADC up to 2000 p.e.; with $C_{inj} = 500$ pF is less than ± 3 UADC up to 3000 p.e.



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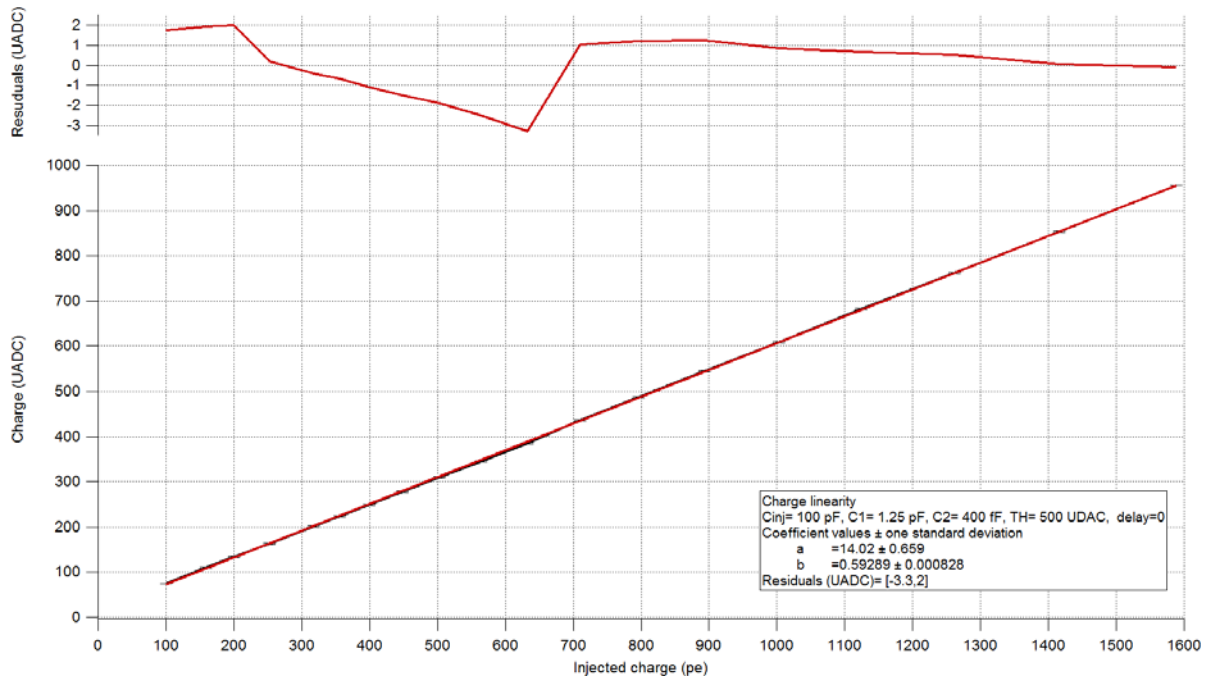


Figure 38 - Charge linearity

Cinj= 100 pF ; C1= 1.25pF ; C2= 400 fF ; TH= 500 UDAC ; DAC_delay=0 UDAC

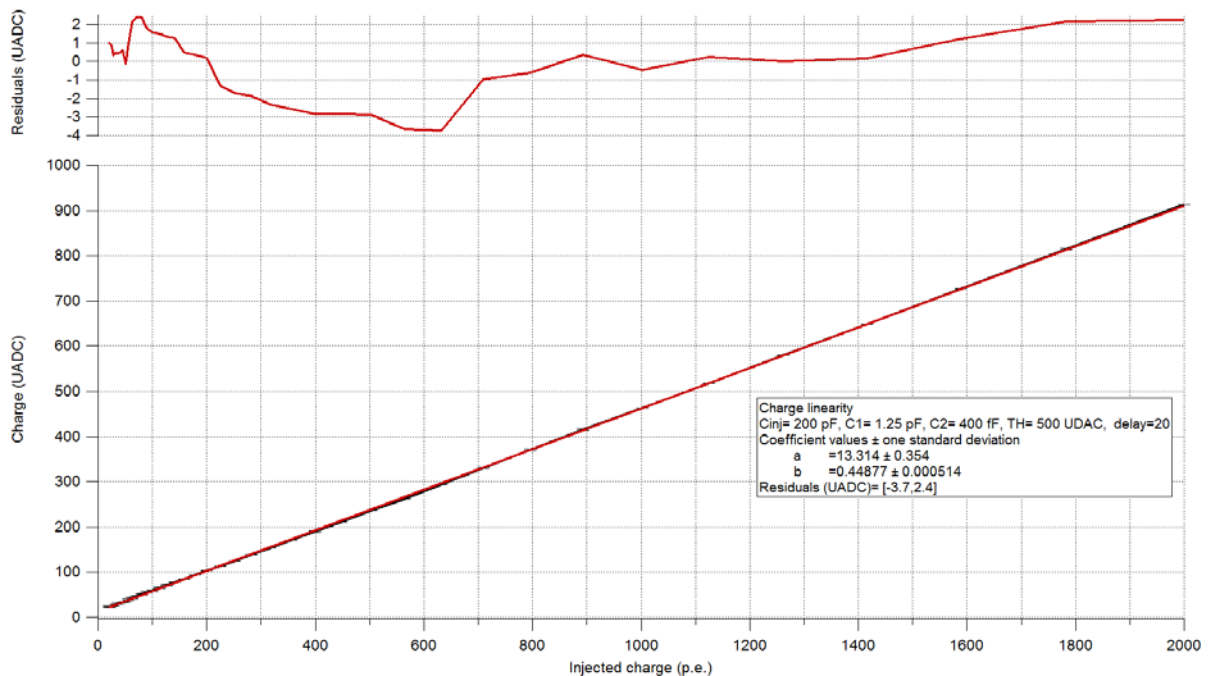


Figure 39 - Charge linearity

Cinj= 200 pF ; C1= 1.25pF ; C2= 400 fF ; TH= 500 UDAC ; DAC_delay=20 UDAC

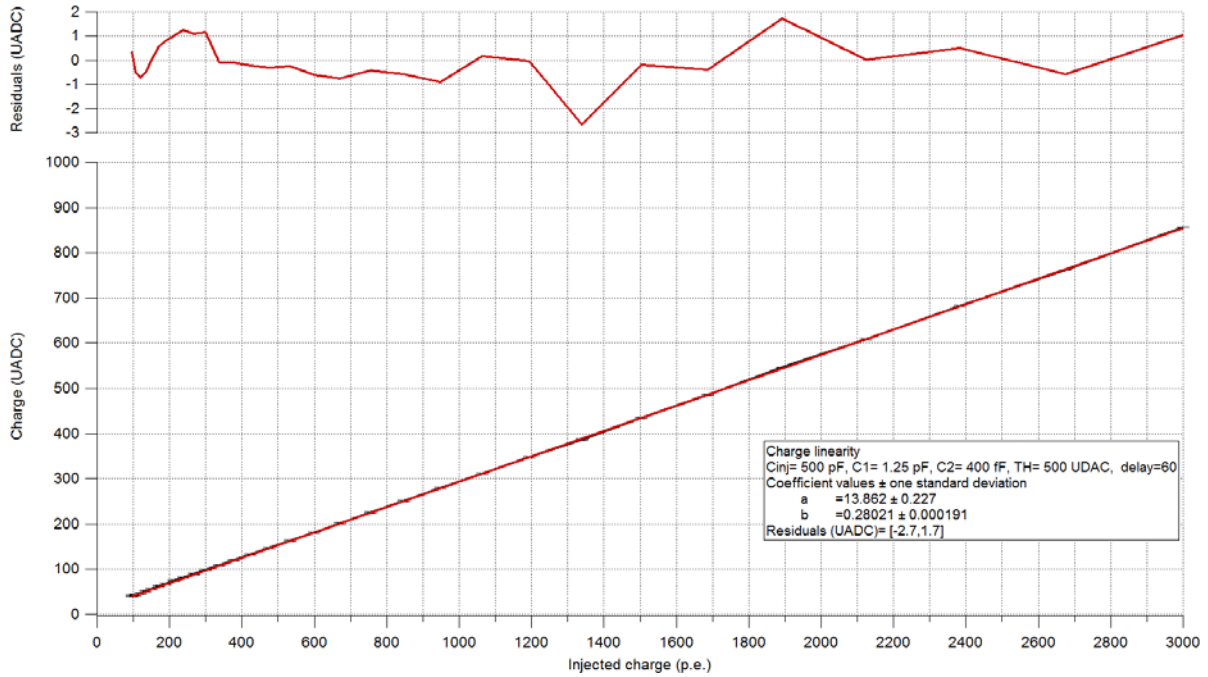


Figure 40 – Charge linearity measurement

Cinj= 500 pF ; C1= 1.25pF ; C2= 400 fF ; TH= 500 UDAC ; DAC_delay=60 UDAC

7.8 TAC measurements

Time to Amplitude measurements have been performed on the 32 channels. The time resolution is 70 ps rms.

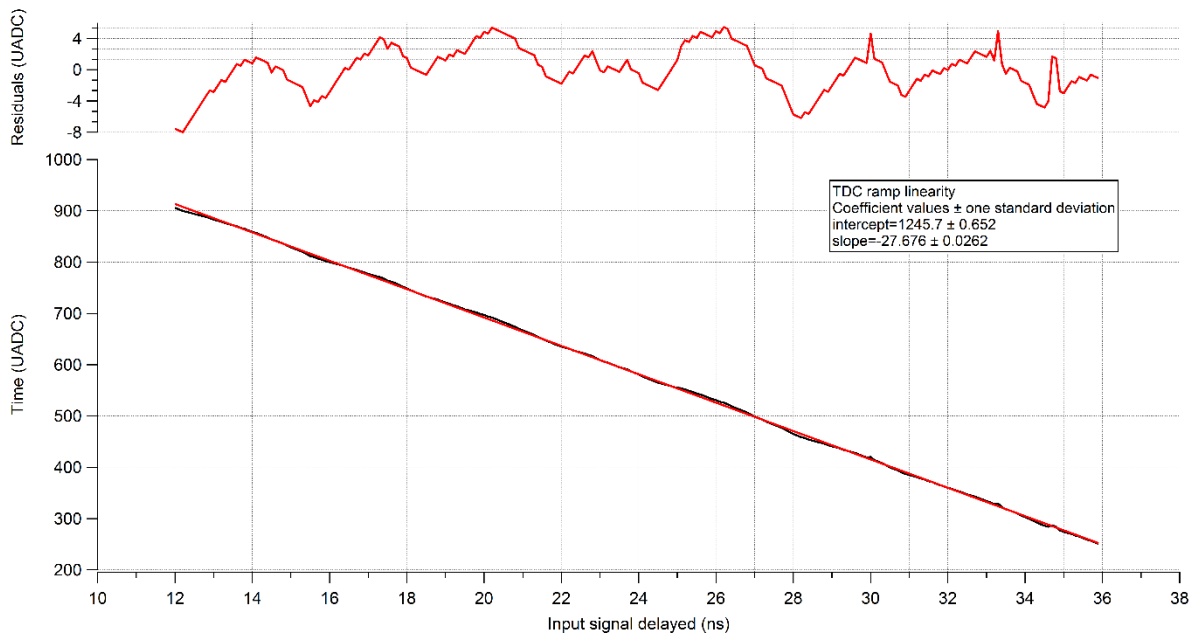


Figure 41 – TAC Ramp linearity



7.9 SiPM measurements

7.9.1 Coincidence Time Resolution

Timing measurement has been carried out in analogue mode (digital conversion disabled and time difference between two channels measured externally) and in full digital conversion mode (charge and time). The time measurement has been measured by using a Na22 source, FBK NUV-HD (4x4 mm², 40um microcell) SiPMs and 2x2x3mm³ LSO:Ce codoped Ca scintillators. In analogue mode (Figure 42), the Coincidence Time Resolution (CTR), is measured around 85.5 ps FWHM. On the other hand, in full digital mode (Figure 43), the measured CTR increased to 127.3 ps FWHM for the events selected around the 511 keV photopeak.

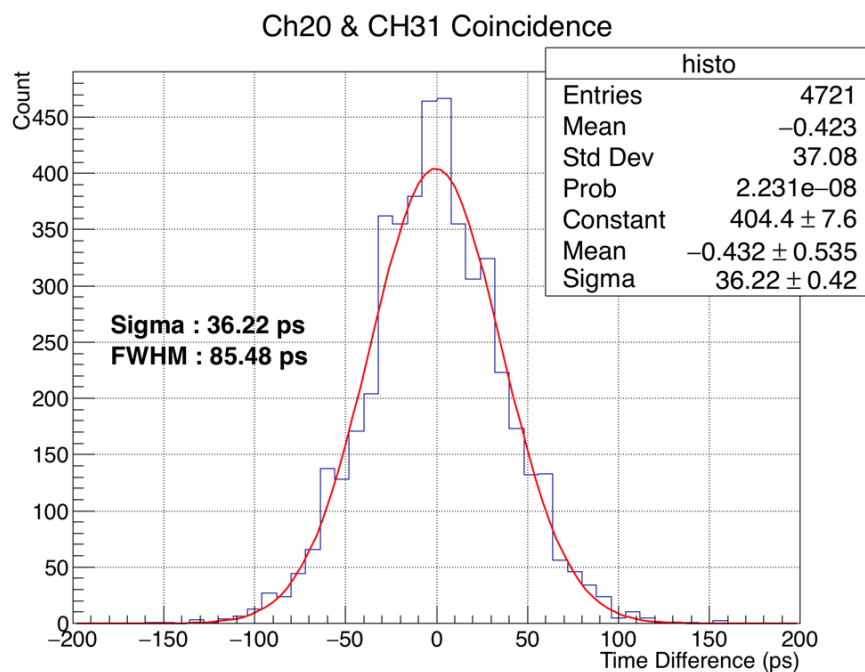


Figure 42 - Coincidence Time Resolution in analogue mode.



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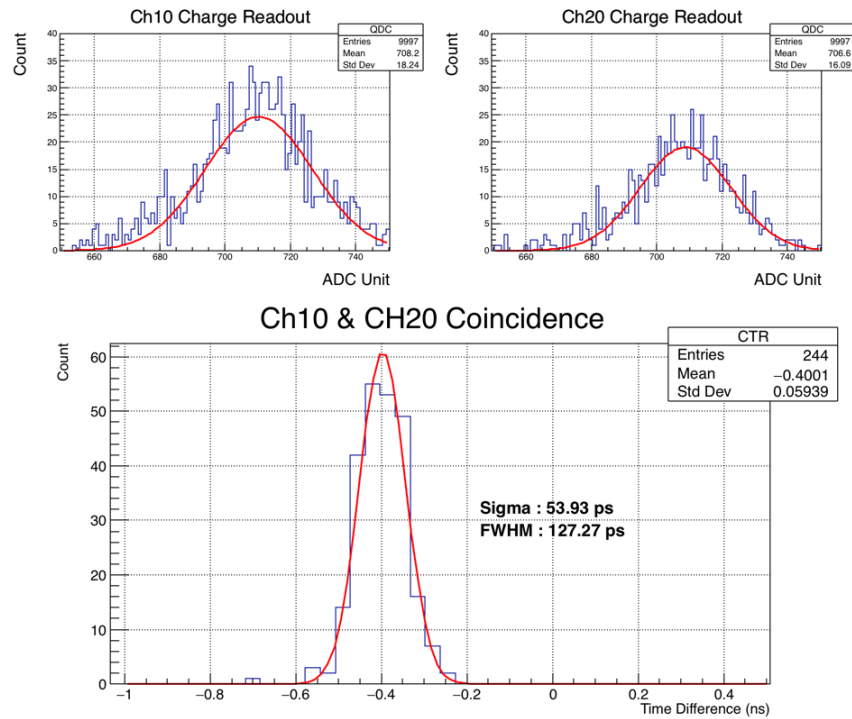


Figure 43 - Coincidence Time Resolution in digital mode (charge and time conversion).



7.9.2 Energy Resolution

Energy measurement has been performed for Na22 source with Hamamatsu MPPC S13360-3050PE (3x3 mm², 50um pixel pitch) SiPM and 3x3x20mm³ LSO:Ce codoped Ca scintillator. Non corrected energy resolution for 511 keV photopeak (Figure 44) is about 10.2%. It is expected that this energy resolution could increase to 12-13% with the correction.

QDC Readout

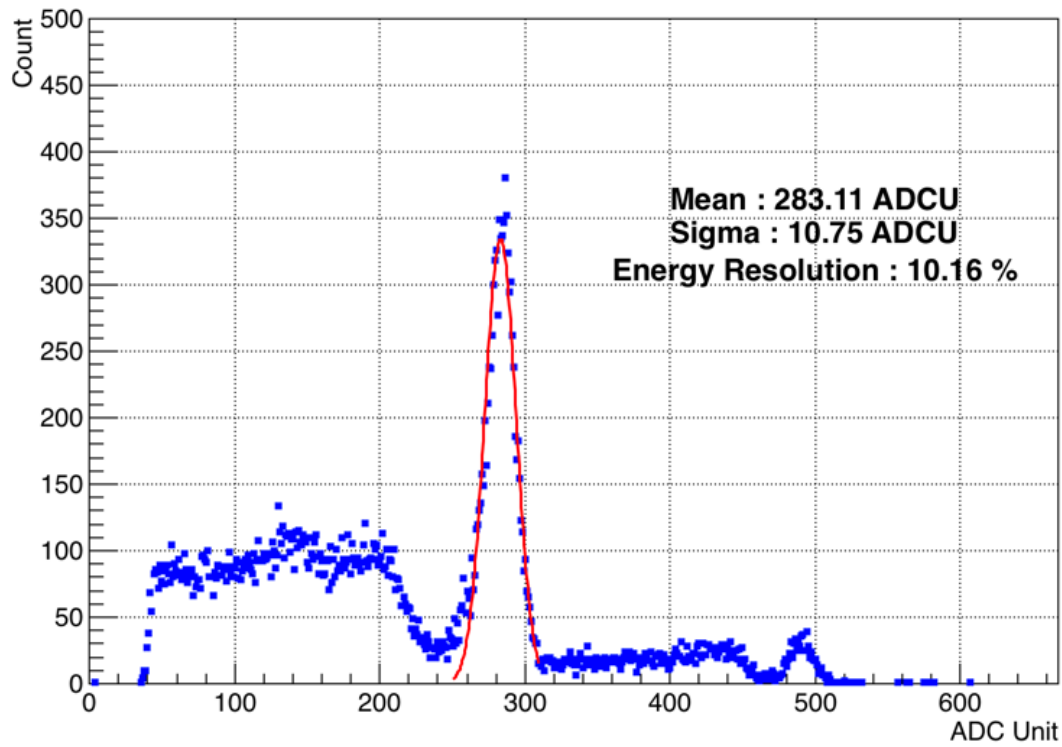


Figure 44 - Energy Resolution (non-corrected) for Na22 at 511 keV.



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8 Petiroc 2A pinout

8.1 QFP 208 package

8.1.1 Package layout & mechanics

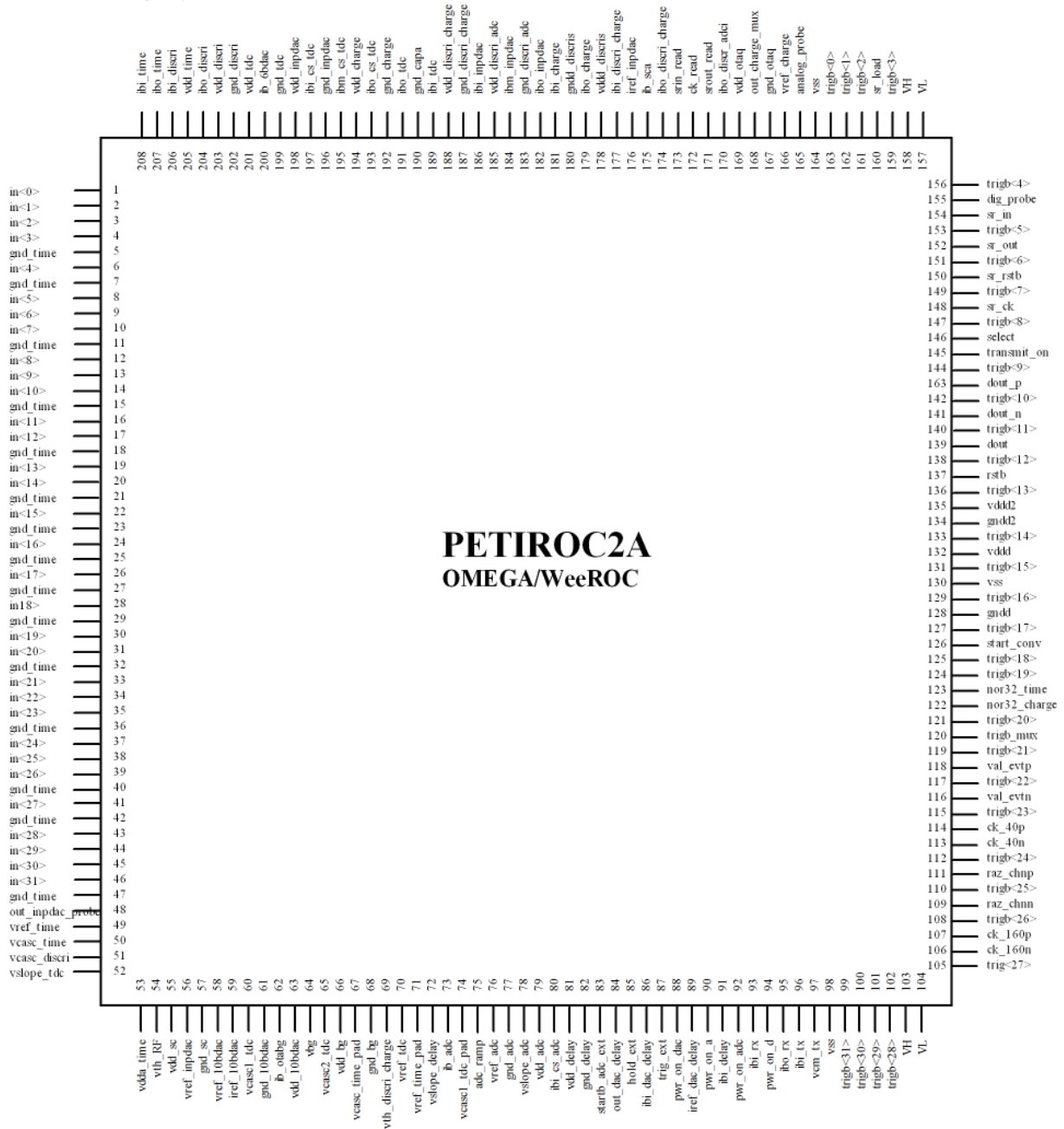


Figure 45 – Pinout of Petiroc 2A



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8.1.2 Pin type description

Pin description without a pin number are connected inside the package or not but are not outted.

Pin#	Pin name	Pin type	Description	Connection
1	in<0>	Analog input	Voltage input for SiPM signal	Connect to SIPM
2	in<1>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
3	in<2>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
4	in<3>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
5	gnd_time	Power	Ground	Connect to ground plane
6	in<4>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
7	gnd_time	Power	Ground	Connect to ground plane
8	in<5>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
9	in<6>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
10	in<7>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
11	gnd_time	Power	Ground	Connect to ground plane
12	in<8>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
13	in<9>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
14	in<10>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
15	gnd_time	Power	Ground	Connect to ground plane
16	in<11>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
17	in<12>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
18	gnd_time	Power	Ground	Connect to ground plane
19	in<13>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
20	in<14>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
21	gnd_time	Power	Ground	Connect to ground plane
22	in<15>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
23	gnd_time	Power	Ground	Connect to ground plane
24	in<16>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
25	gnd_time	Power	Ground	Connect to ground plane
26	in<17>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
27	gnd_time	Power	Ground	Connect to ground plane
28	in<18>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
29	gnd_time	Power	Ground	Connect to ground plane
30	in<19>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
31	in<20>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
32	gnd_time	Power	Ground	Connect to ground plane
33	in<21>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
34	in<22>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
35	in<23>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
36	gnd_time	Power	Ground	Connect to ground plane
37	in<24>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
38	in<25>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
39	in<26>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
40	gnd_time	Power	Ground	Connect to ground plane
41	in<27>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
42	gnd_time	Power	Ground	Connect to ground plane
43	in<28>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM
44	in<29>	Analog. Input	Voltage input for SiPM signal	Connect to SIPM



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45	in<30>	Analog. Input	Voltage input for SiPM signal	Connect to SiPM
46	in<31>	Analog. Input	Voltage input for SiPM signal	Connect to SiPM
47	gnd_time	Power	Ground	Connect to ground plane
48	out_inpDAC_probe	Analog. Output	Probe the input DAC value	Analog buffer or NC
49	vref_time	Analog. Bias	Should be 2.2V	Decoupling 100n or NC
50	vcasc_time	Analog. Bias	2.2V	Decoupling 100n or NC
51	vcasc_discri	Analog. Bias	2.3V	Decoupling 100n or NC
52	vslope_tdc	Analog. Bias	350mV	Decoupling 100n or NC
53	vdda_time	Power	3.3V	Connect to analog vdda
54	vth_RF	Analog. Output		Decoupling 100n or NC
55	vdd_sc	Power	3.3V	vdd
56	vref_inpDAC	Analog. Bias	1V	Decoupling 100n or NC
57	gnd_sc	Power	Ground	Connect to ground plane
58	vref_10bDAC_T	Analog. Bias		Decoupling 100n or NC
59	iref_10bDAC	Analog. Bias	2.25V	Decoupling 100n or NC
60	vcasc1_tdc	Analog. Bias	1.2V	Decoupling 100n or NC
61	gnd_10bDAC	Power	Ground	Connect to ground plane
62	ib_otabg	Analog. Bias		Decoupling 100n or NC
63	vdd_10bDAC	Power	3.3V	
64	vbg	Analog. Output	2.5V	Decoupling 100n
65	vcasc2_tdc	Analog. Bias	1.7V	Decoupling 100n or NC
66	vdd_bg	Power	3.3V	vdd
67	vcasc_time_pad	Analog. Bias	2.2V	Decoupling 100n or NC
68	gnd_bg	Power	Ground	Connect to ground plane
69	vth_discri_charge	Analog. Output		Decoupling 100n or NC
70	vref_tdc	Analog. Bias	900mV	
71	vref_time_pad	Analog. Bias	2.2V	Decoupling 100n or NC
72	vslope_delay	Analog. Bias	250mV	Decoupling 100n or NC
73	ib_ADC	Analog. Bias		
74	vcasc1_tdc_pad	Analog. Bias	1.2V	Decoupling 100n or NC
75	ADC_ramp	Analog. Output		NC
76	vref_ADC	Analog. Bias	730 mV	Decoupling 100n or NC
77	gnd_ADC	Power	Ground	Connect to ground plane
78	vslope_ADC	Analog. Bias	500 mV	Decoupling 100n or NC
79	vdd_ADC	Power	3.3V	Vdd
80	ibi_cs_ADC	Analog. Bias		Decoupling 100n or NC
81	vdd_delay	Power	3.3V	vdd
82	gnd_delay	Power	Ground	Connect to ground plane
83	startb_ADC_ext	Digital Input		Connect to DAQ
84	out_DAC_delay	Analog. Output		
85	hold_ext	Digital Input		Connect to DAQ
86	ibi_DAC_delay	Analog. Bias		
87	trig_ext	Digital Input		Connect to DAQ
88	pwr_on_DAC	Digital Input		Connect to DAQ
89	iref_DAC_delay	Analog. Bias		
90	pwr_on_A	Digital Input		Connect to DAQ
91	ibi_delay	Analog. Bias		Decoupling 100n or NC
92	pwr_on_ADC	Digital Input		



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93	ibi_rx	Analog. Bias		Decoupling 100n or NC
94	pwr_on_D	Digital Input		Connect to DAQ
95	ibo_rx	Analog. Bias		Decoupling 100n or NC
96	ibi_tx	Analog. Bias		Decoupling 100n or NC
97	vcm_tx	Analog. Bias		Decoupling 100n or NC
98	vssd	Power		
99	trigb<31>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
100	trigb<30>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
101	trigb<29>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
102	trigb<28>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
103	VH	Power	High level of dig. Buffer 1.5V (or 3.3V)	Connect to power supply Decoupling 100nF
104	VL	Power	Low level of dig. Buffer -GND	Connect to ground
105	trigb<27>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
106	ck_160n	Digital LVDS input		Connect to DAQ
107	ck_160p	Digital LVDS input		Connect to DAQ
108	trigb<26>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
109	raz_chnn	Digital LVDS input		Connect to DAQ
110	trigb<25>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
111	raz_chnp	Digital LVDS input		Connect to DAQ
112	trigb<24>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
113	ck_40n	Digital LVDS input		Connect to DAQ
114	ck_40p	Digital LVDS input		Connect to DAQ
115	trigb<23>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
116	val_evtn	Digital LVDS input		Connect to DAQ
117	trigb<22>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
118	val_evtp	Digital LVDS input		Connect to DAQ
119	trigb<21>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
120	trig_mux	Digital output		VH VL buffer
121	trigb<20>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
122	nor32_charge	Digital (OC) output		Connect to DAQ
123	nor32_time	Digital (OC) output		
124	trigb<19>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
125	trigb<18>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
126	start_conv	Digital input		Connect to DAQ
127	trigb<17>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
128	gndd	Power	Ground	Connect to ground plane
129	trigb<16>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
130	vssd	Power	vss digital	
131	trigb<15>	Digital output		VH VL buffer
132	vddd	Power	3.3V	vddd
133	trigb<14>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
134	gndd2	Power	Ground	Connect to ground plane
135	vddd2	Power	3.3V	vddd
136	trigb<13>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
137	rstb	Digital input		Connect to DAQ
138	trigb<12>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
139	dout	Digital (OC) output		Connect to DAQ



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140	trigb<11>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
141	dout_n	Digital LVDS output		Connect to DAQ
142	trigb<10>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
143	dout_p	Digital LVDS output		Connect to DAQ
144	trigb<9>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
145	transmit_onb	Digital (OC) output		Connect to DAQ
146	select	Digital input		Connect to DAQ
147	trigb<8>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
148	sr_ck	Digital input		Connect to DAQ
149	trigb<7>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
150	sr_rstb	Digital input		Connect to DAQ
151	trigb<6>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
152	sr_out	Digital output		Connect to DAQ
153	trigb<5>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
154	sr_in	Digital input		Connect to DAQ
155	digital_probe	Digital output		Connect to DAQ
156	trigb<4>	Digital output	Trigger output (Hi state = VH)	Connect to DAQ
157	VL	Power	Low level of dig. Buffer -GND	Connect to ground
158	VH	Power	High level of dig. Buffer 1.5V (or 3.3V)	Connect to digital power supply
159	trigb<3>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
160	sr_load	Digital input		Connect to DAQ
161	trigb<2>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
162	trigb<1>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
163	trigb<0>	Digital output	Trigger output (Hi state = VH)	VH VL buffer
164	vssd	Power	Ground	Connect to ground plane
165	analog_probe	Analog output		
166	vref_charge	Analog Bias		Decoupling 100n or NC
167	gnd_otaq	Power		
168	out_charge_mux	Analog output		Connect to external ADC
169	vdd_otaq	Power	3.3V	vdd
170	ibo_discri_ADC	Analog Bias		Decoupling 100n or NC
171	srout_read	Digital output		Connect to DAQ
172	ck_read	Digital input		Connect to DAQ
173	srin_read	Digital input		Connect to DAQ
174	ibo_discri_charge	Analog Bias		Decoupling 100n or NC
175	ib_sca	Analog Bias		Decoupling 100n or NC
176	iref_inpDAC	Analog Bias		Decoupling 100n or NC
177	ibi_discri_charge	Analog Bias		Decoupling 100n or NC
178	vddd_discris	Power	3.3V	vddd
179	ibo_charge	Analog Bias		Decoupling 100n or NC
180	gndd_discris	Power	Ground	Connect to ground plane
181	ibi_charge	Analog Bias		Decoupling 100n or NC
182	ibo_inpDAC	Analog Bias		Decoupling 100n or NC
183	gnd_discri_ADC	Power	Ground	Connect to ground plane
184	ibm_inpDAC	Analog Bias		Decoupling 100n or NC
185	vdd_discri_ADC	Power	3.3V	vdd
186	ibi_inpDAC	Analog Bias		Decoupling 100n or NC



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187	gnd_discri_charge	Power	Ground	Connect to ground plane
188	vdd_discri_charge	Power	3.3V	vdd
189	ibi_tdc	Analog Bias		Decoupling 100n or NC
190	gnd_capa	Power	Ground	Connect to ground plane
191	ibo_tdc	Analog Bias		Decoupling 100n or NC
192	gnd_charge	Power	Ground	Connect to ground plane
193	ibo_cs_tdc	Analog Bias		Decoupling 100n or NC
194	vdd_charge	Power	3.3V	
195	ibm_cs_tdc	Analog Bias		Decoupling 100n or NC
196	gnd_inpDAC	Power		
197	ibi_cs_tdc	Analog Bias		Decoupling 100n or NC
198	vdd_inpDAC	Power	3.3V	vdd
199	gnd_tdc	Power	Ground	Connect to ground plane
200	ib_6bDAC	Analog Bias		Decoupling 100n or NC
201	vdd_tdc	Power	3.3V	vdd
202	gnd_discri	Power	Ground	Connect to ground plane
203	vdd_discri	Power	3.3V	vdd
204	ibo_discri	Analog Bias		Decoupling 100n or NC
205	vdd_time	Power	3.3V	vdd
206	ibi_discri	Analog Bias	785mV	Decoupling 100n or NC
207	ibo_time	Analog Bias	1.3V	Decoupling 100n or NC
208	ibi_time	Analog Bias		Decoupling 100n or NC

Table 8 – QFP 208 pin type description



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8.2 TFBGA 353 package

8.2.1 Package layout & mechanics

	1	2	3	4	5	6	7	8	9	10	11	12								
A	in4	in3	in2	in1	in0	ibo_time	ibo_discri	ibm_discri	ibi_cs_tdc	ibo_cs_tdc	ibo_tdc	ibi_inpDAC								
B	in5	NC	NC	NC	NC	ibi_time	ibi_discri	ib_fol_discri	ib_6bDAC	ibm_cs_tdc	ibi_tdc	ibm_inpDAC								
C	in6	NC																		
D	in7	NC																		
E	in8	NC											VDDI	VDDI	VDDI	VDDI	NC	NC	NC	NC
F	in9	NC											VDDI	VDDI	VDDI	VDDI	VDDA	VDDA	VDDA	VDDA
G	in10	NC																		
H	in11	NC											VDDI	VDDI	VSS	VSS	VSS	VSS	VSS	
J	in12	NC																		
K	in13	VDDI											VDDI	VDDI	VSS	VSS	VSS	VSS	VSS	
L	in14	VDDI																		
M	in16	in15											VDDI	NC	VSS	VSS	VSS	VSS	VSS	

Figure 47 – North-West Petiroc 2A ball-out



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N	in17	VDDI				VDDI	NC			VSS	VSS	VSS	VSS	VSS				
P	in18	VDDI				VDDI	VDDI			VSS	VSS	VSS	VSS	VSS	VSS			
R	in19	NC				VDDI	VDDI			VSS	VSS	VSS	VSS	VSS				
T	in20	NC				VDDI	VDDI			VSS	VSS	VSS	VSS	VSS				
U	in21	NC				VDDI	VDDI											
V	in22	NC				VDDI	VDDI											VDDA
W	in23	NC				VDDI	VDDI			VDDA	VDDA	vbg	vth_discr _charge	VDDA	ib_ADC			
Y	in24	NC																
AA	in25	NC																
AB	in26	NC															NC	NC
AC	in27	in28	in29	in30	in31	vref_time	vth_RF	vslope_td c	vref_inpD AC	vcasc1_td c	vcasc_tim e_pad	vcasc_dis cri_pad						
	1	2	3	4	5	6	7	8	9	10	11	12						

Figure 48 – South-West Petiroc 2A ball-out



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13	14	15	16	17	18	19	20	21	22	23	
ibo_inpDAC	ibo_charge	ibo_discr_charge	ibm_discr_charge	ck_read	out_charge_mux	analog_probe	trigb0	trigb1	trigb2	trigb3	A
ibi_charge	iref_inpDAC	ibi_discr_charge	ibi_discr_ADC	ibo_discr_ADC	ibm_discr_ADC	vref_charge	ib_otaq	sr_load	VH	trigb4	B
									VL	trigb5	C
									dig_probe	trigb6	D
NC	ib_sca	srin_read	srout_read	VDDD	VDDD	VDDD			sr_in	trigb7	E
VDDA	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD			sr_rstb	trigb8	F
						VDDD	sr_out		sr_ck	trigb9	G
VSS	VSS	VSS	VSS			VDDD	select		transmit_onb	trigb10	H
VSS	VSS	VSS	VSS			VDDD	dout		dout_p	trigb11	J
VSS	VSS	VSS	VSS			VDDD	rstb		dout_n	trigb12	K
VSS	VSS	VSS	VSS			NC	NC		trigb13	trigb14	L
VSS	VSS	VSS	VSS			VDDD	VDDD		trigb15	trigb16	M

Figure 49 – North-East Petiroc 2A ball-out



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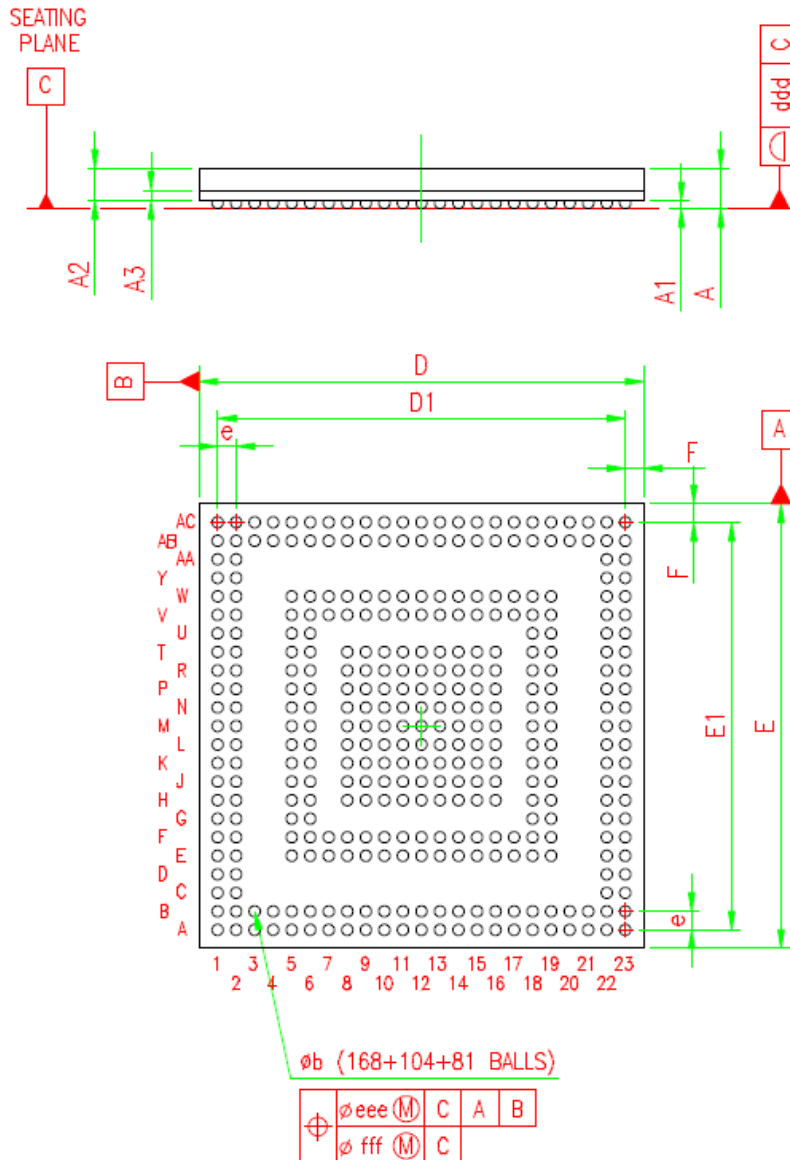


VSS	VSS	VSS	VSS		NC	NC			trigb17	trigb18	N
VSS	VSS	VSS	VSS		VDDD	nor32_time			start_conv	trigb19	P
VSS	VSS	VSS	VSS		VDDD	nor32_charge			trigb_mux	trigb20	R
VSS	VSS	VSS	VSS		VDDD	val_evtn			val_evtp	trigb21	T
					VDDD	raz_chnp			ck_40p	trigb22	U
VDDA	VDDA	VDDA	VDDD	VDDD	VDDD	VDDD			ck_40n	trigb23	V
startb_ADC_ext	hold_ext	pwr_on_DAC	pwr_on_a	pwr_on_d	VDDD	VDDD			raz_chnn	trigb24	W
									ck_160p	trigb25	Y
									ck_160n	trigb26	AA
vslope_delay	vcasc1_tdc_pad	vslope_ADC	out_DAC_delay	ibo_rx	ibi_rx	ibi_tx	vcm_tx	VH	VL	trigb27	AB
vref_time_pad	vref_tdc	vref_ADC	trig_ext	iref_DAC_delay	ibi_delay	pwr_on_ADC	trigb31	trigb30	trigb29	trigb28	AC
13	14	15	16	17	18	19	20	21	22	23	

Figure 50 – South-East Petiroc 2A ball-out



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DIMENSIONS

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A			1.20
A1	0.15		
A2		0.88	
A3		0.28	
b	0.25	0.30	0.35
D	11.85	12.00	12.15
D1		11.00	
e		0.50	
E	11.85	12.00	12.15
E1		11.00	
F		0.50	
ddd			0.08
eee			0.15
fff			0.05

Figure 51 - Petiroc 2A TFPGA package mechanics description

8.2.2 Pin type description

Please refer to section 8.2.2 of the present datasheet to get a pin description.



9 Petiroc 2A Q&A

Q : what is the utility of the input DAC ?

A :

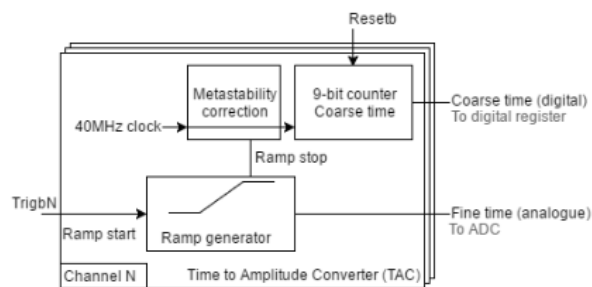
The input DAC allows to adjust SiPM High voltage channel by channel to correct breakdown voltage non-uniformities. It does not impact the fast signal behaviour

Q : how does the TDC works ? What is the TDC start? What is the TDC stop?

A :

A 9-bit coarse time counter is embedded in Petiroc 2A. The frequency clock is 40MHz.

The TDC interpolates the trigger timing in between two coarse time clock ticks. An analog ramp is started by the trigger and stopped by the next coarse time clock tick. There is a metastability remover system. The ramp is converted into digital data by the ADC.

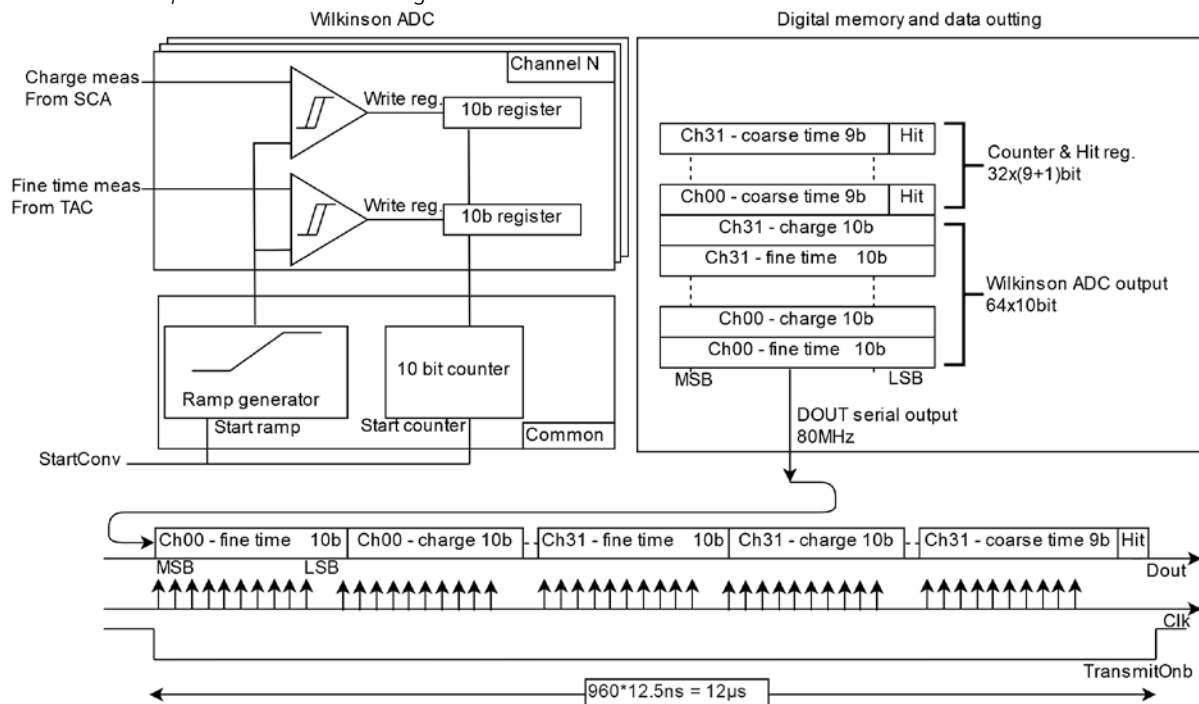


Q : how does the Data-out works ?

A :

The data-out is a serial digital read-out of all channels when using Petiroc 2A in full digital mode.

After conversion, the data are outed in digital with 80MHz data transmission.



Q : what is the utility of DAC_T and DAC_Q ?

A :

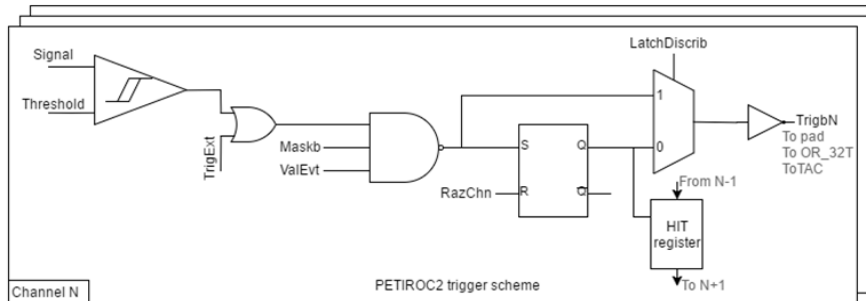
Petiroc 2A embeds 2 10-bit DAC to adjust the two trigger threshold.



Datasheet Petiroc 2A



DAC_T is the low level threshold that is used for time measurement. The trigger diagram block is shown below. Discriminator can be outed directly or can be latched when Petiroc 2A is used in full digital mode. When using analog serial read-out for faster event rate, a hit register allows to know which channel have passed the threshold.



DAC_Q set the value of a high level trigger that possibly allow discarding low energy events. The energy discriminator is connected on the energy measurement line, after the slow shaper.

Q : What is the event rate of Petiroc 2A

A :

In full-digital mode, rate per ASIC is 40Kevent/second

In analog mode (requires an external ADC) the rate can reach 500kcps

Q : What is the utility of OR32_T and OR32_Q ?

A :

OR32_T is the OR of all time trigger (threshold is set by DAC_T). It allows the user to know that at least one channel has passed the low level threshold

OR32_Q is the OR of all energy trigger (threshold is set by DAC_Q). It allows the user to know that at least one channel has passed the energy threshold.

In a more general manner, these two signals are used to trigger the DAQ system.

Q : Is there any company using Petiroc 2A in a system ?

A :

No commercial system is using Petiroc 2A, several HEP experiments and medical imaging companies are currently testing or prototyping Petiroc 2A.

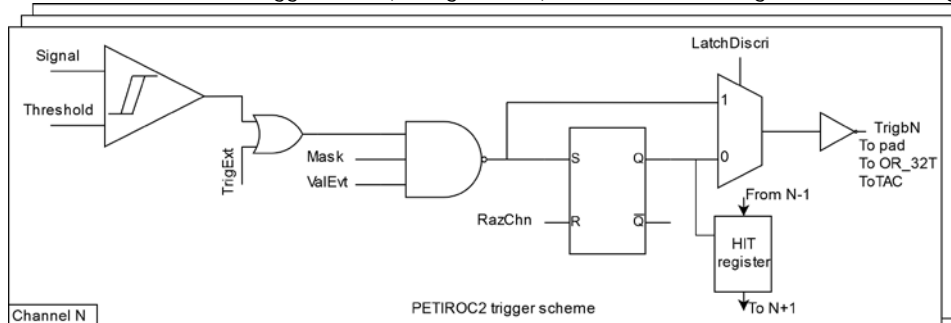
NDA signed with these companies does not allow Weeroc to provide their name.

Q : what is the utility of Razchnb and Valevt signal ?

A :

Razchnb is used to reset the fast trigger latches as shown in the diagram below.

ValEvt allow to blind the trigger chain (timing window) if needed. A Mask signal allows masking a channel if it is too noisy.





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10 Bug list & hotfix log

1. Gain reduction for pre-amplifier (20 gain instead of 40) : Place a 150 kOhm resistor between vref_time_pad (pin 71 or AC13) and ground. The pre-amplifier baseline will be shifted from ~1.15 V to ~1.75V. Time threshold (vth_time) will increase: DAC Code 0 ~1.473 V; DAC Code 1023 ~2.41 V

11 Document version

Version	Date	Pages	Changelog
2.3	29/05/2017	46	
2.4	11/08/2017	61	Updated info
2.5	15/11/2017	64	Updated info
2.5a	04/10/2018	64	Corrected an error about the pin number of vref_time_pad on Section 10. Bug list & hotfix log