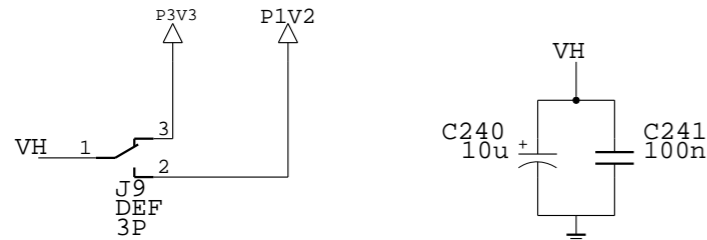
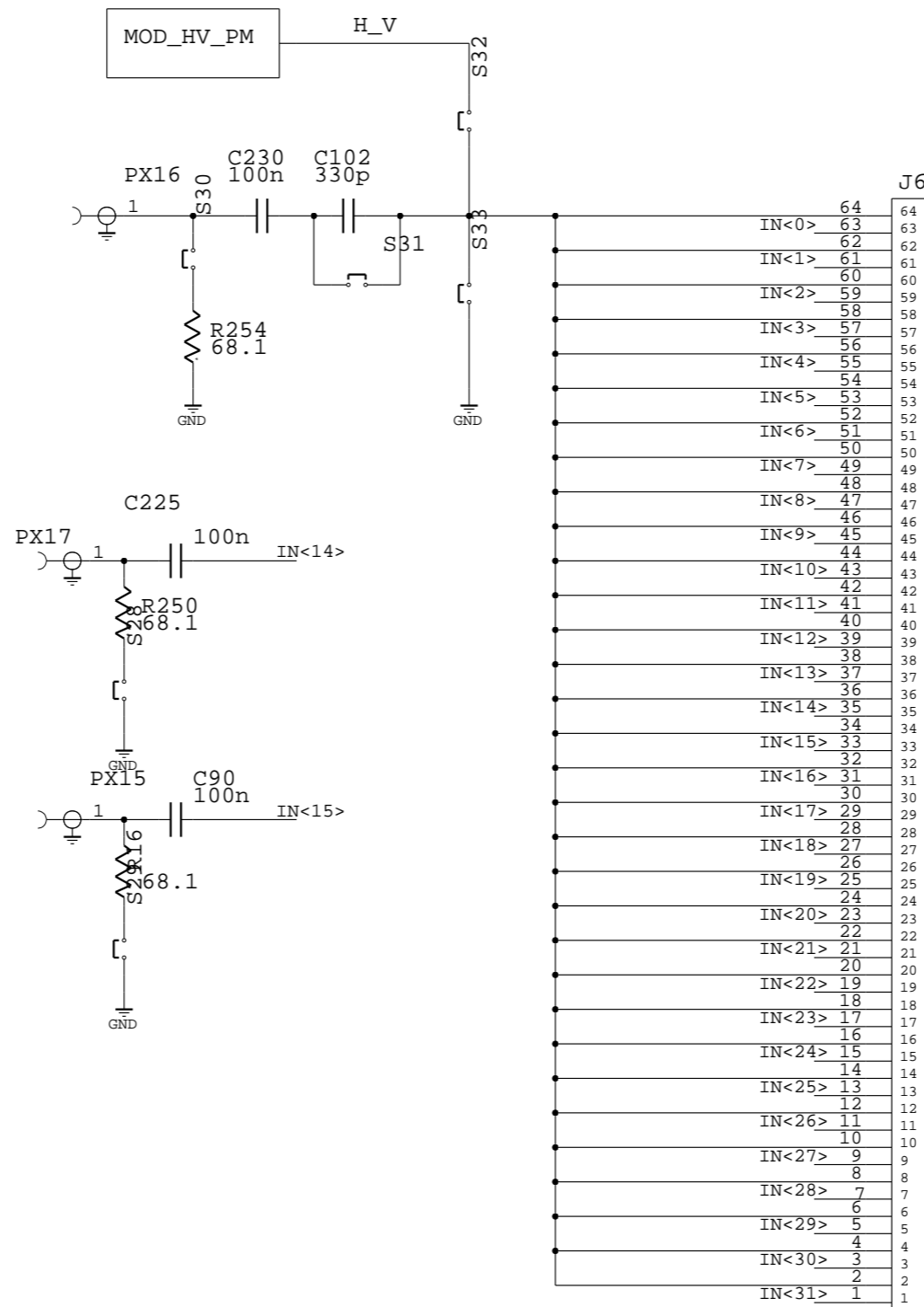


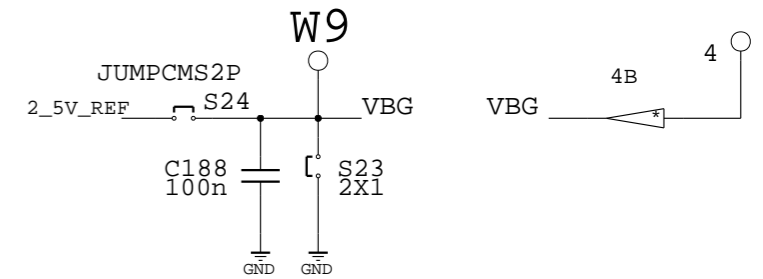
VH Selection with switch to select Voltage



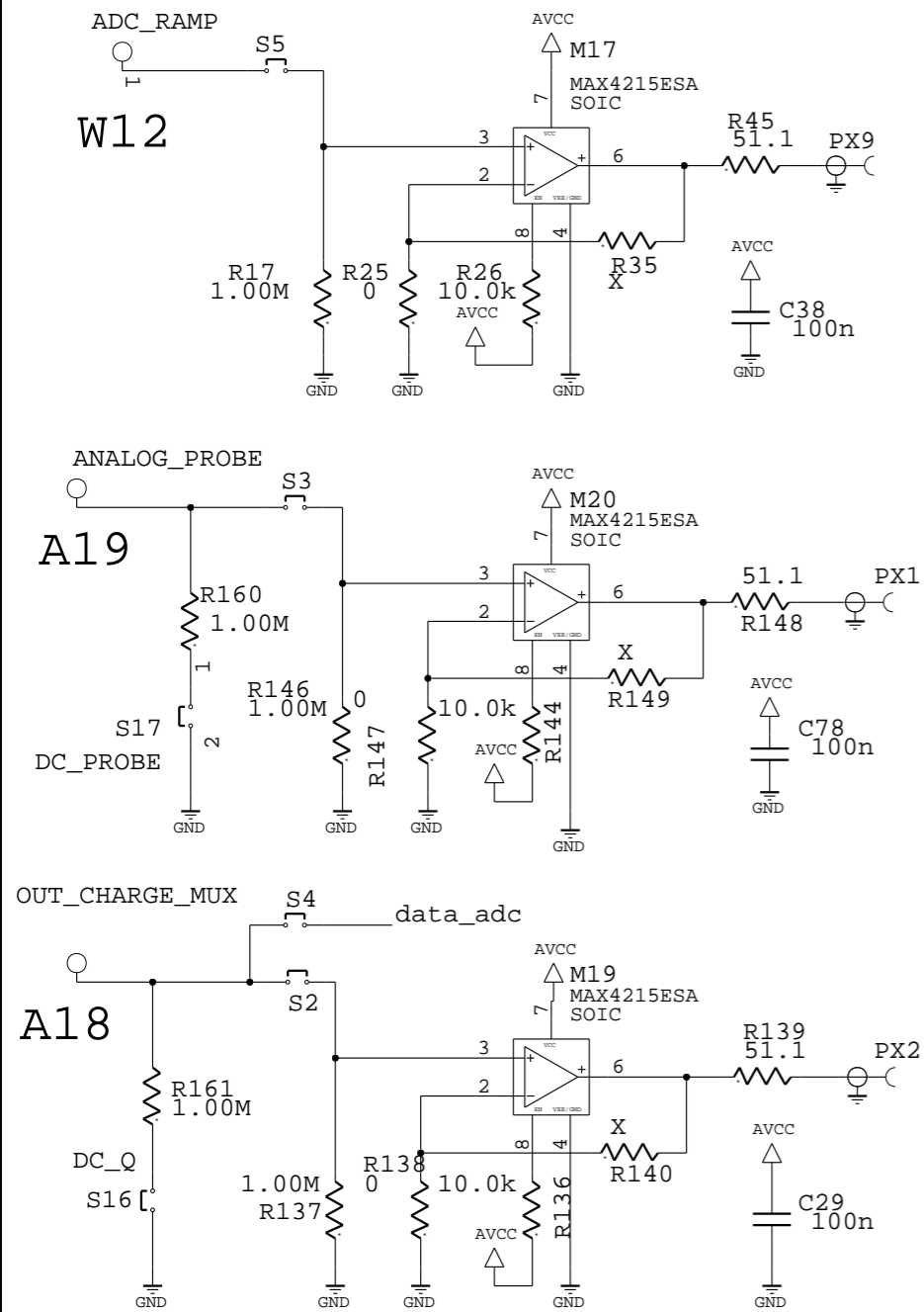
ANALOG INPUTS



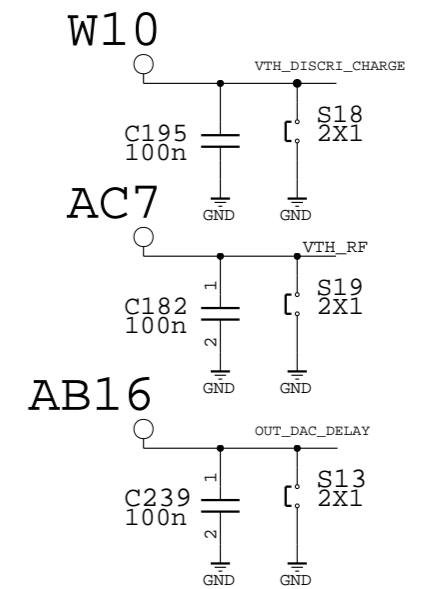
Bandgap



ANALOG OUTPUTS

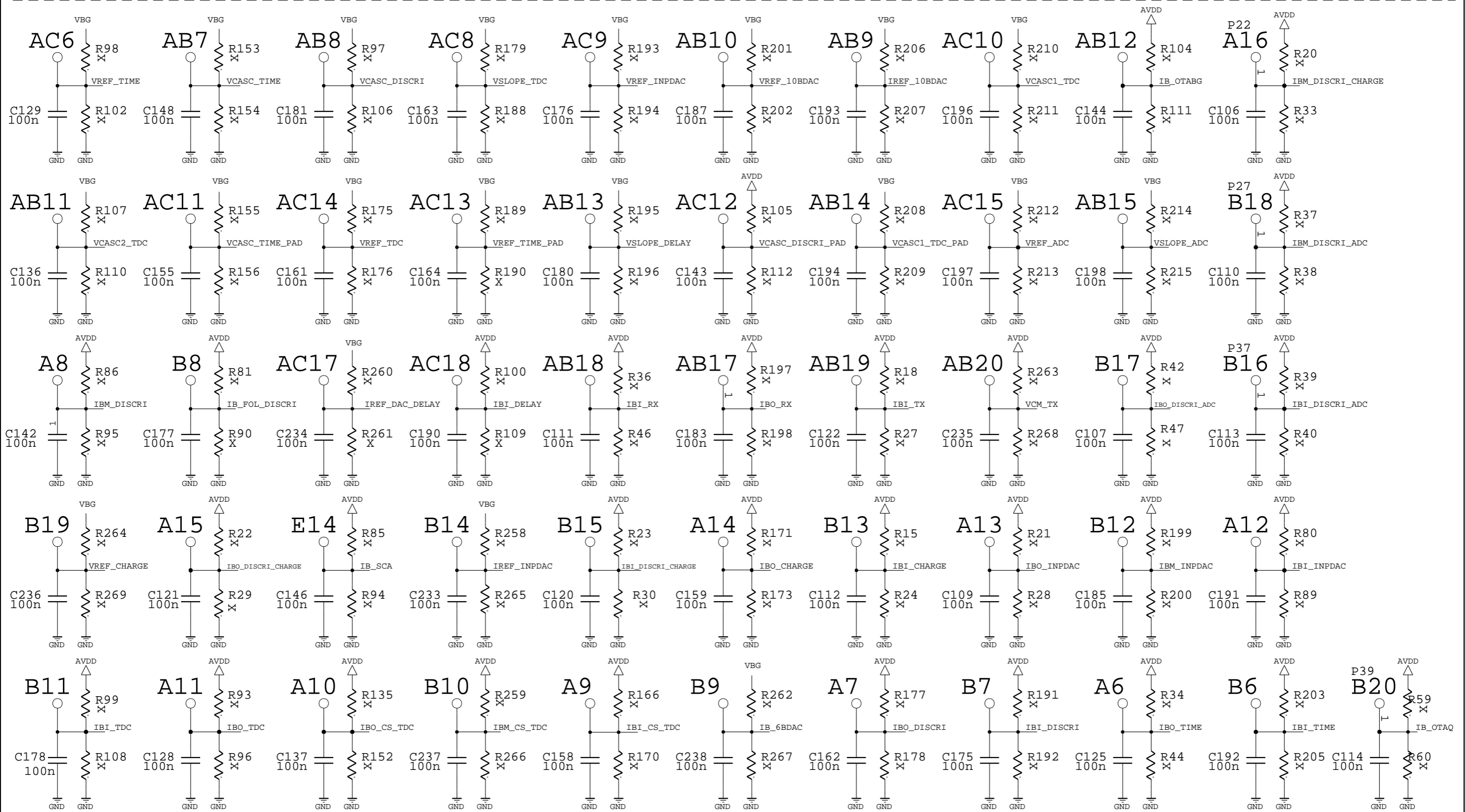


Threshold



test_petiroc_2_bga_v1

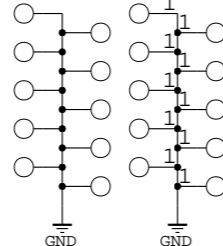
BIAS



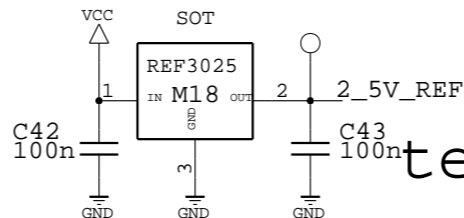
Valeurs Resistances

	Petiroc2	Petiroc2a
R188 =	150K	X
R215 =	150K	X
R262 =	300K	X

Thru holes ground



REF. VOLTAGE

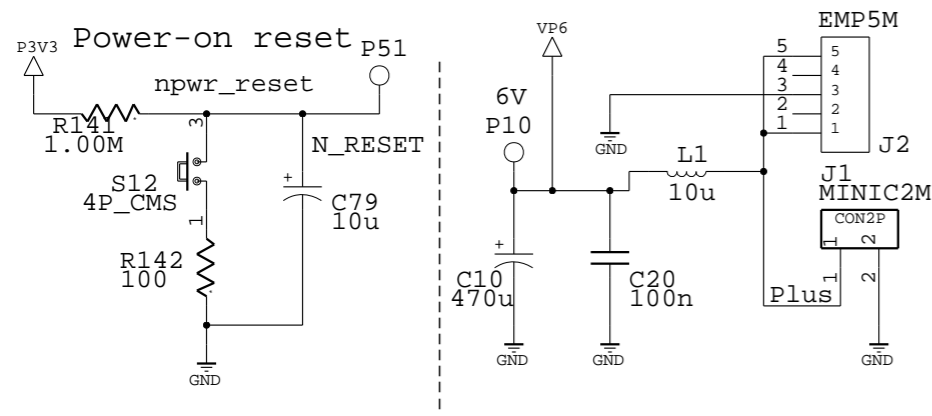


test_petiroc_2_bga_v1

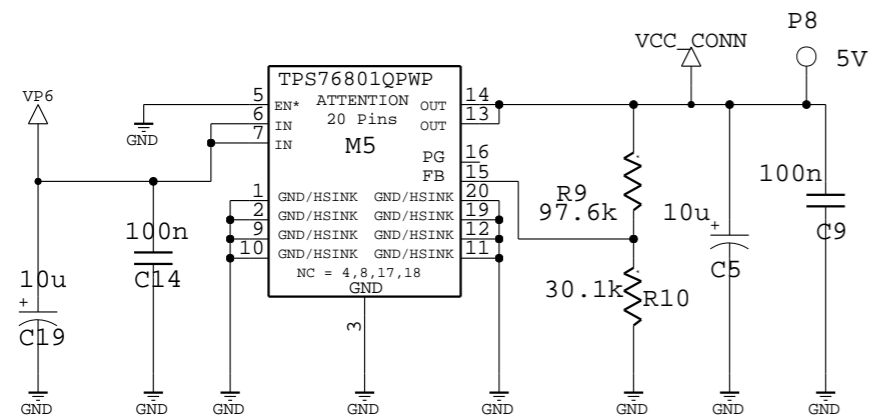
MODIFIE: Fri Mar 11 11:28:41 2016	
ETUDE: 1601	PAGE: 3 / 9
DESSIN: N.Seguin-Moreau S.Callier	SHEET: 3 / 10

---POWER SUPPLY---

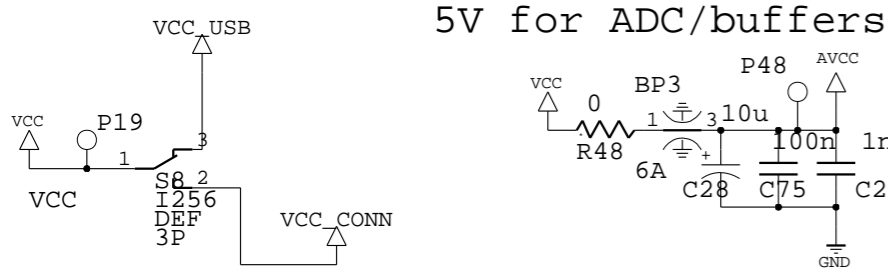
R 0805 (1%) for regulators
 $V_{reg} = 1.1834 * (1 + R1/R2)$ et $R2 = 30.1k$



Vcc from power conn.
for Buffers & external ADC

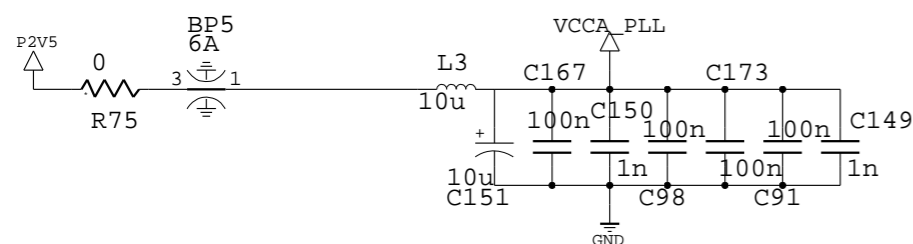


VCC selection

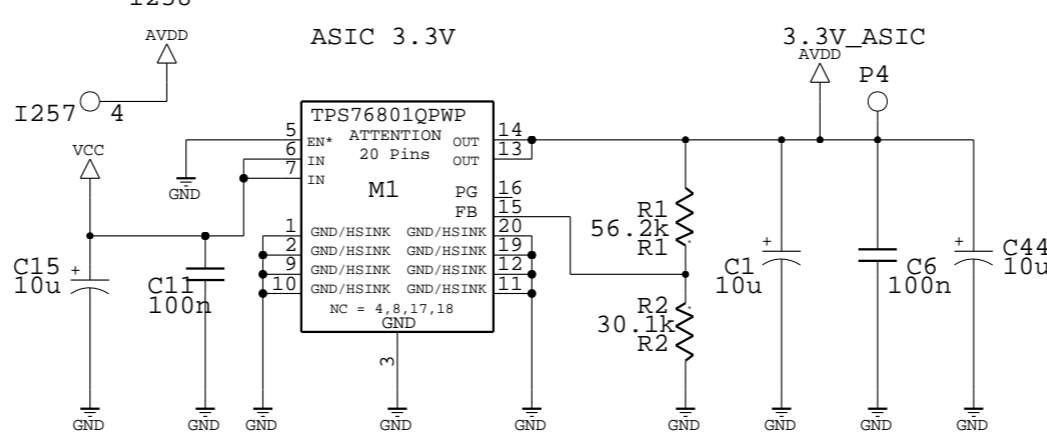


5V for ADC/buffers

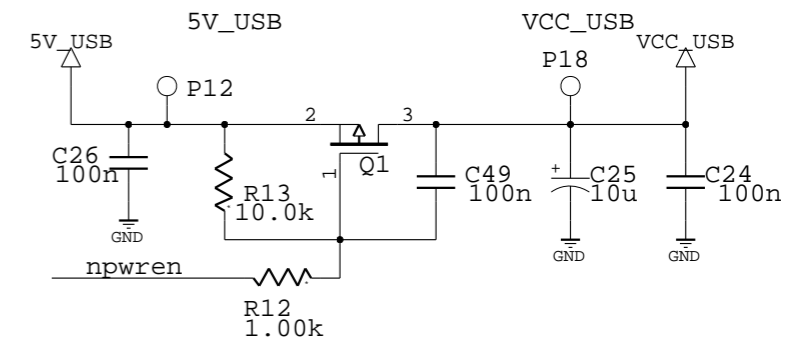
Analog 2V5



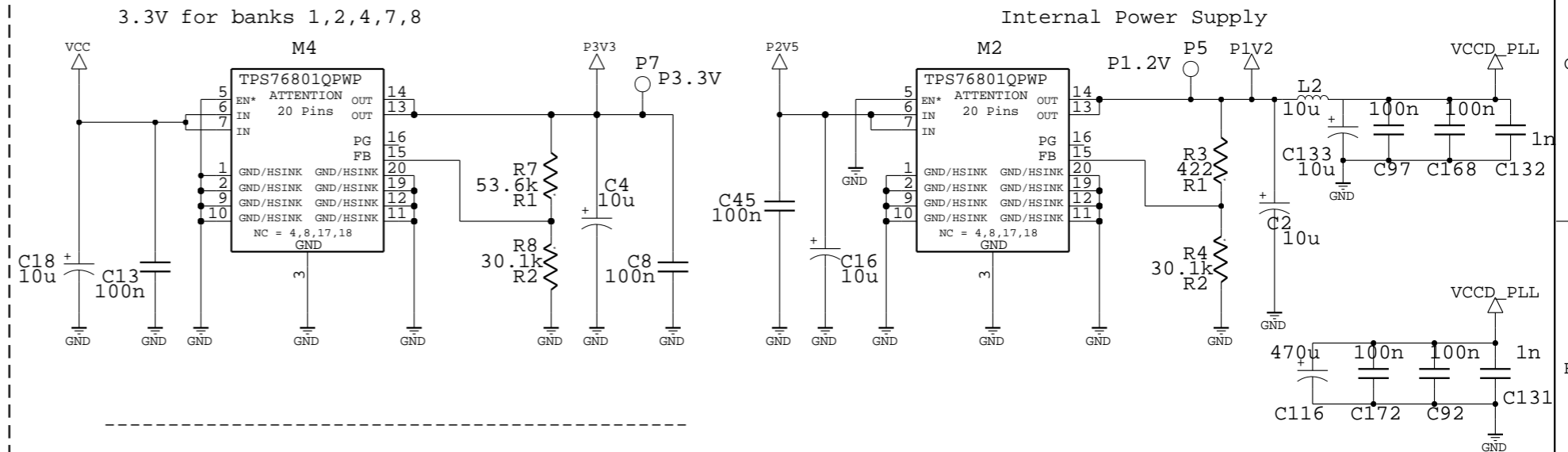
ASIC power supply



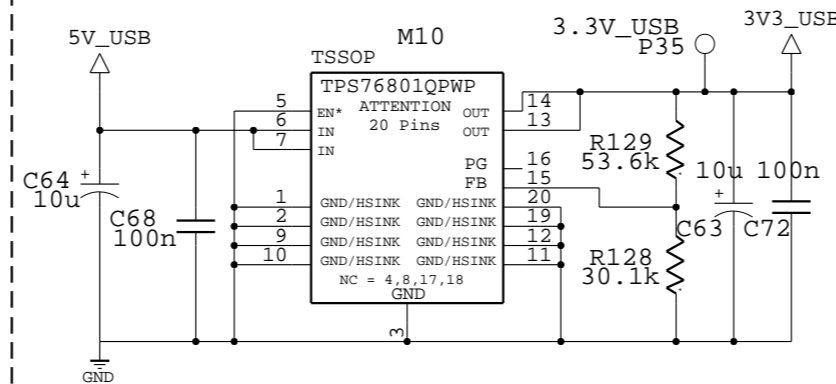
soft power start up
for USB enumeration



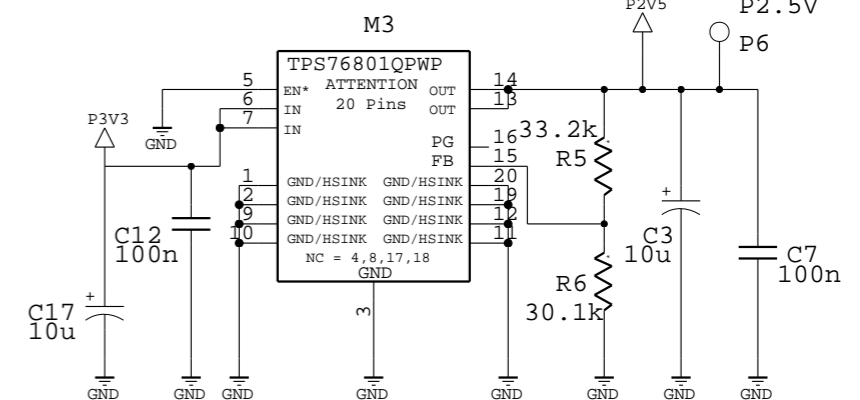
FPGA power supply



3V3 for USB



2.5V for bank 5 (LVDS)



test_petiroc_2_bga_v1

POWER

MODIFIE: Fri Mar 11 11:28:39 2016

ETUDE: 1601

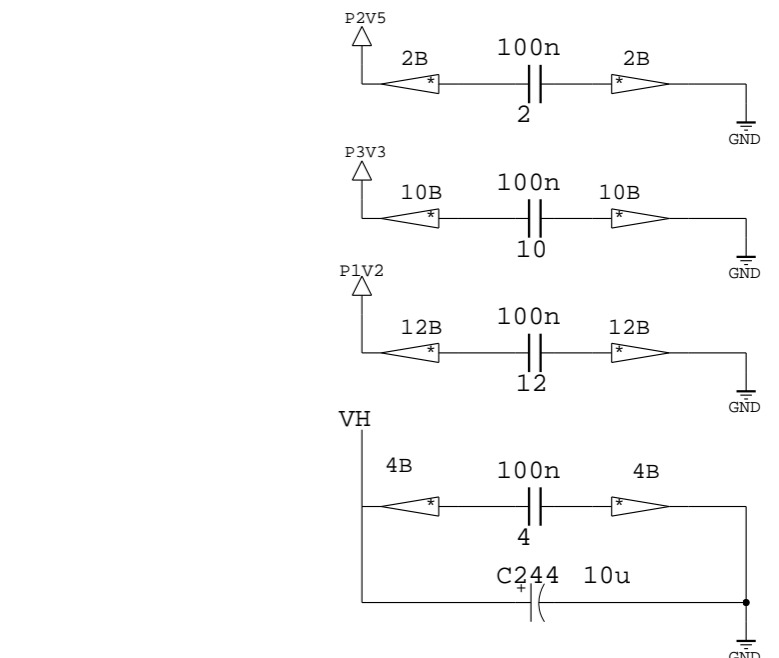
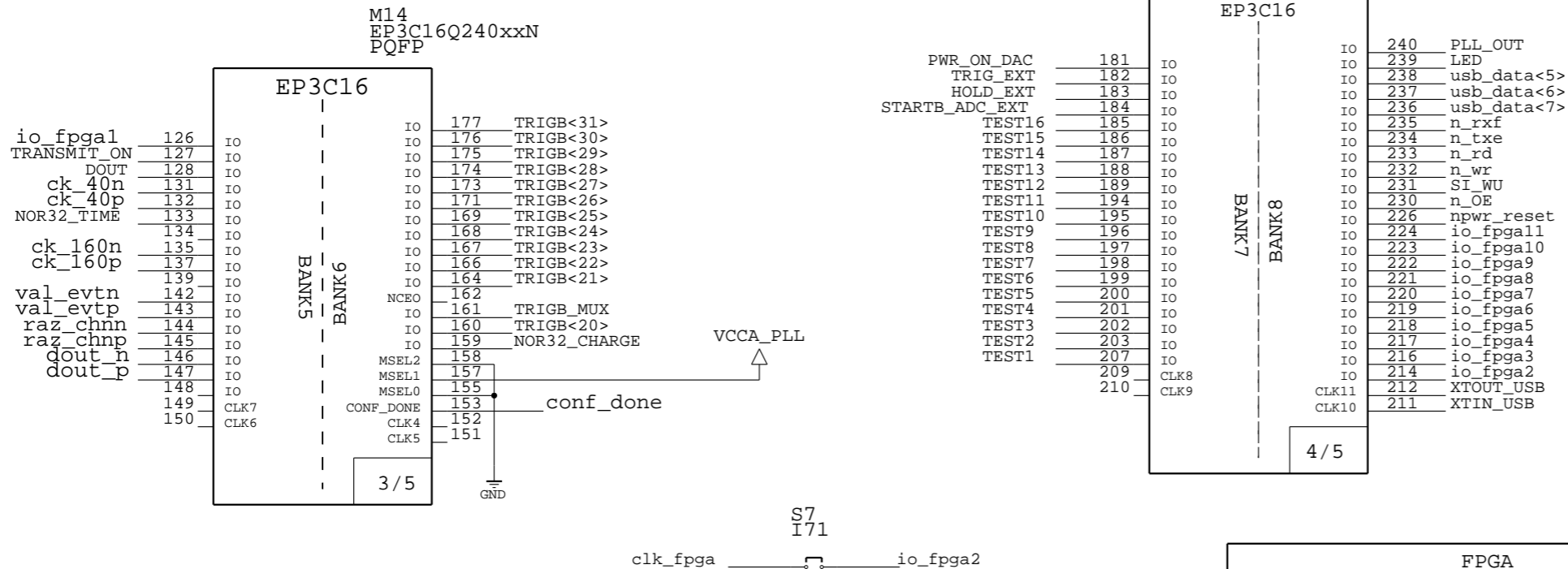
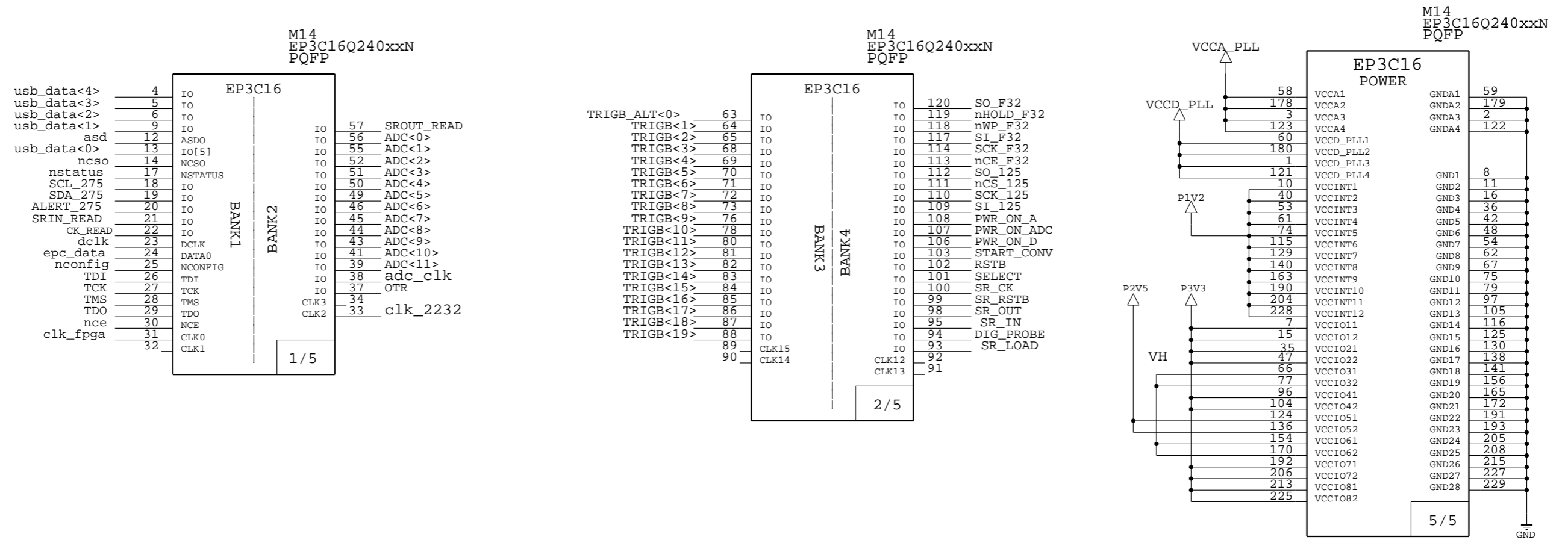
PAGE: 4 / 9

DESSIN: N.Seguin-Moreau
S.Callier


SHEET: 4 / 10





FPGA CYCLONE 3



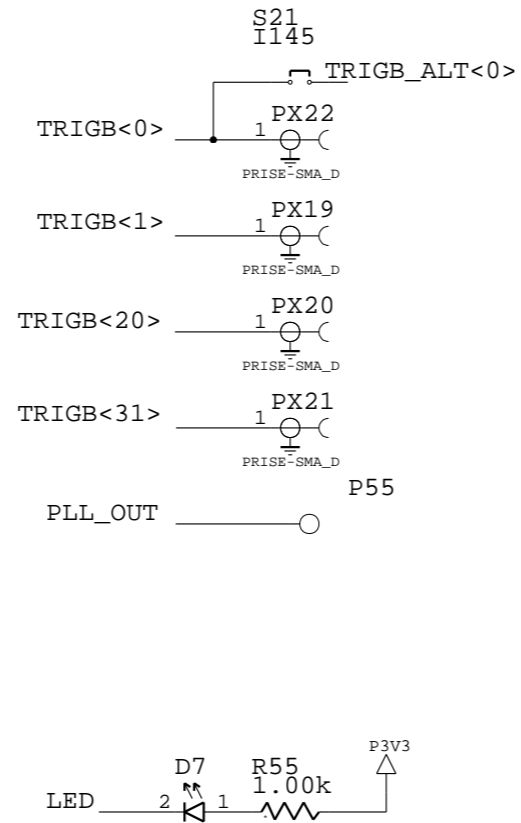
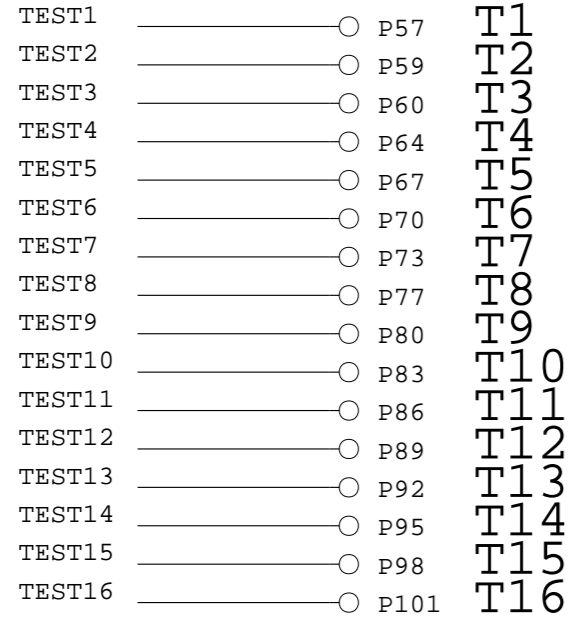
FPGA		MODIFIE: Fri Mar 11 11:28:41 2016	
test_petiroc_2_bga_v1		ETUDE: 1601	PAGE: 5 / 9
		DESSIN: N.Seguin-Moreau S.Callier	SHEET: 5 / 10



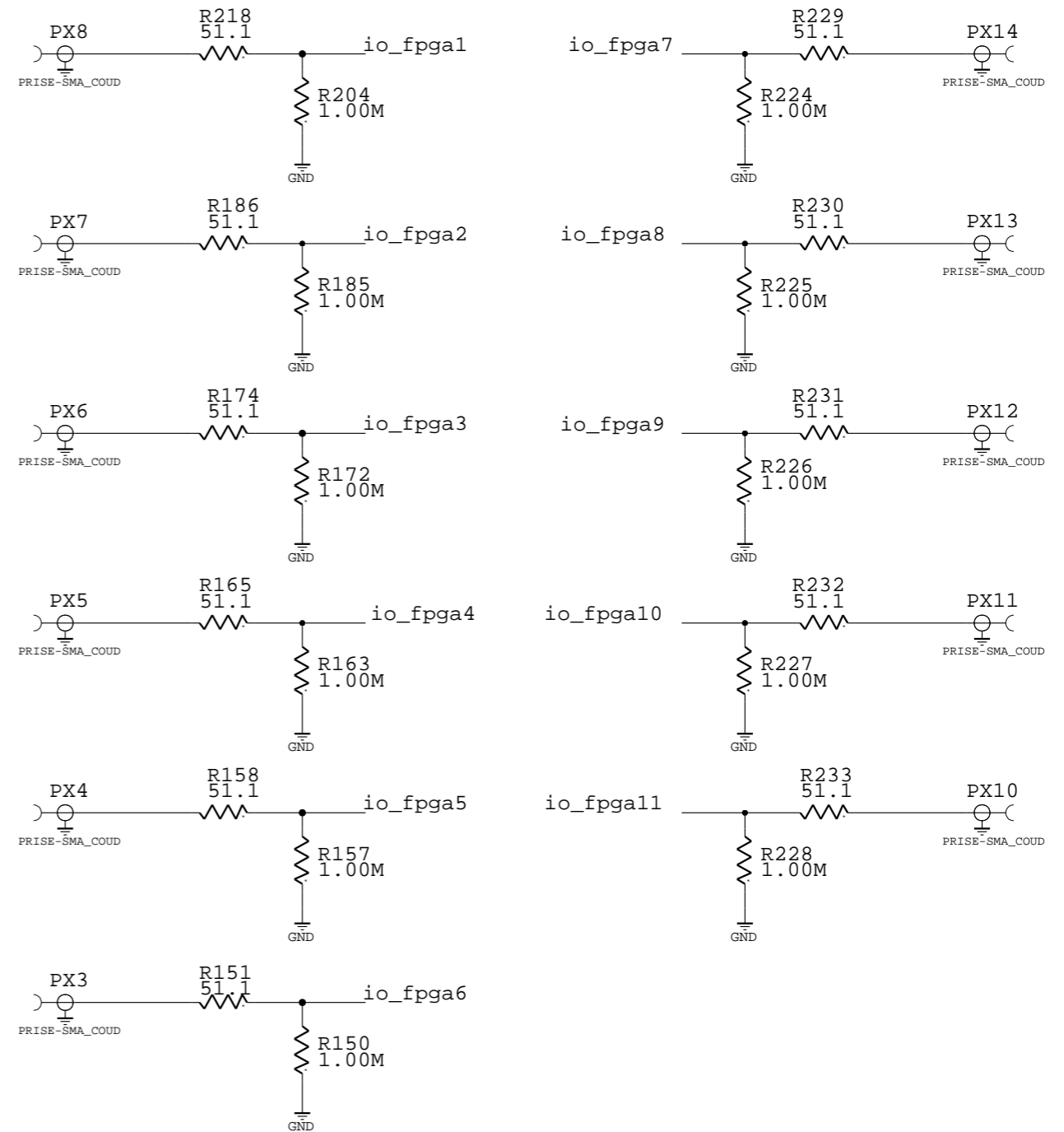
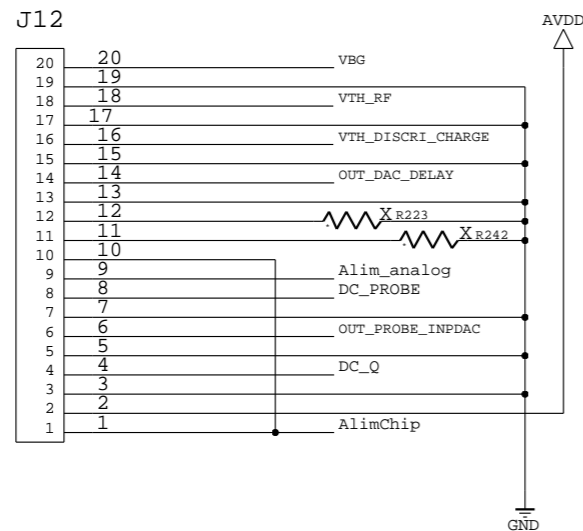



FPGA inputs/outputs

PINS TEST



DC measurement using Keithley

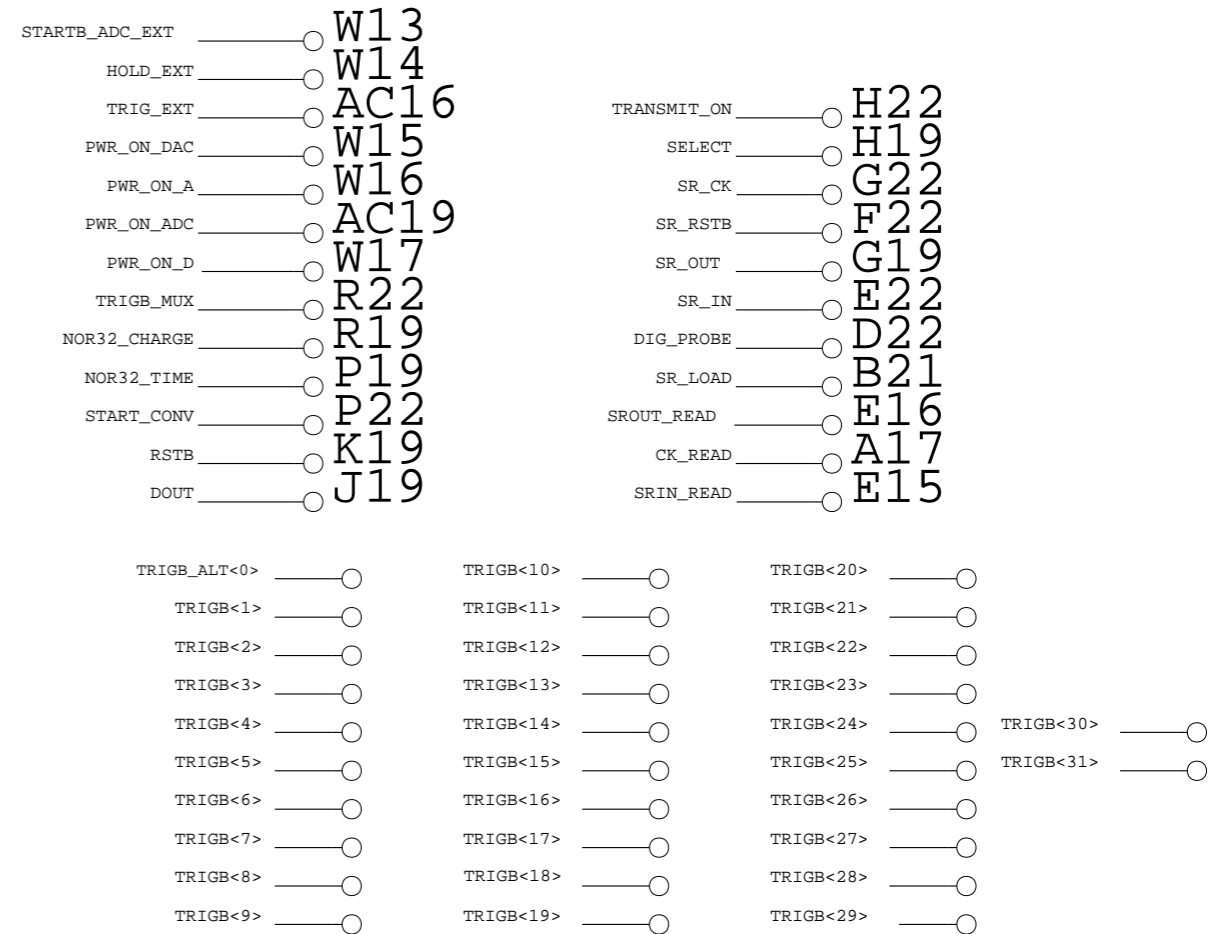
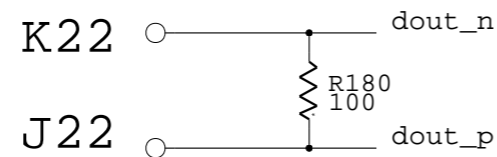
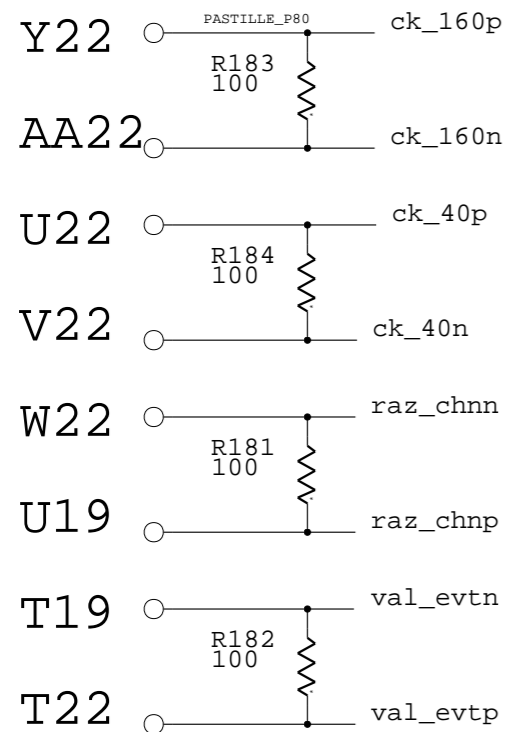


LVDS INPUTS

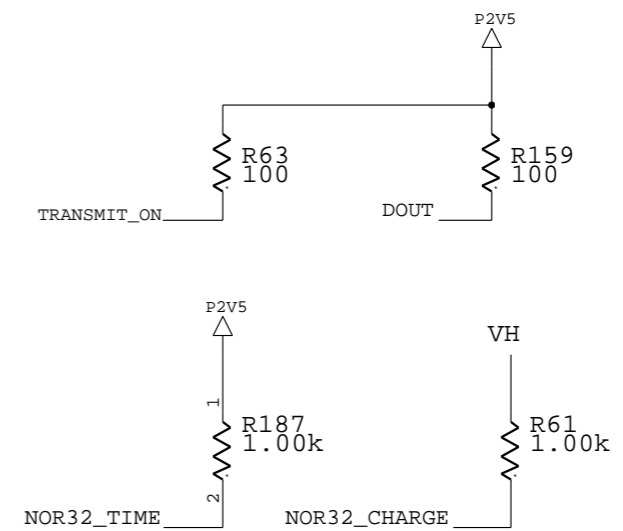
Digital ASIC

ASIC SIDE

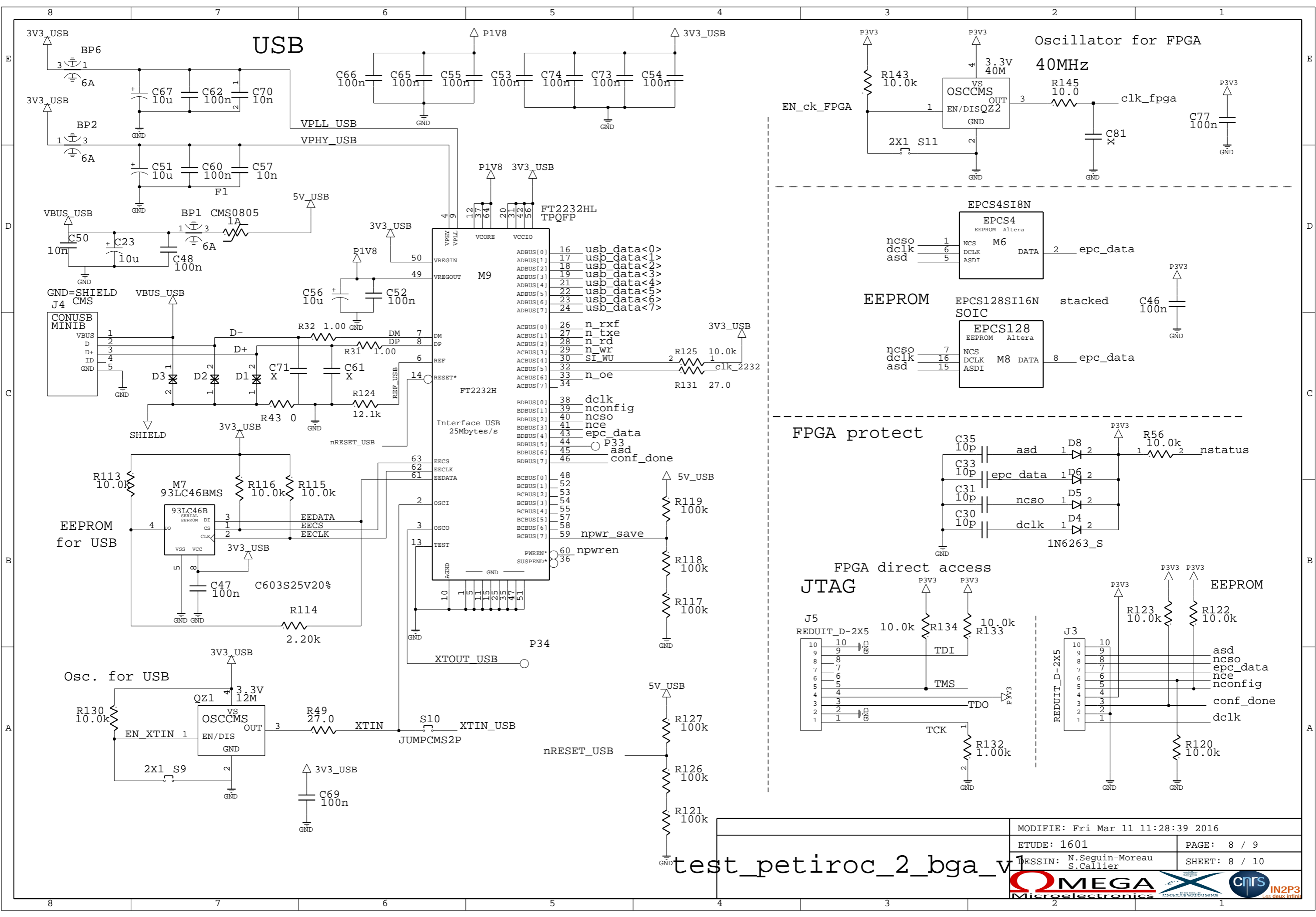
FPGA SIDE



OC OUTPUTS ASIC

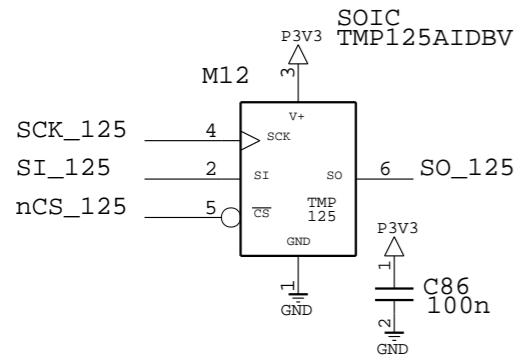


test_petiroc_2_bga_v1

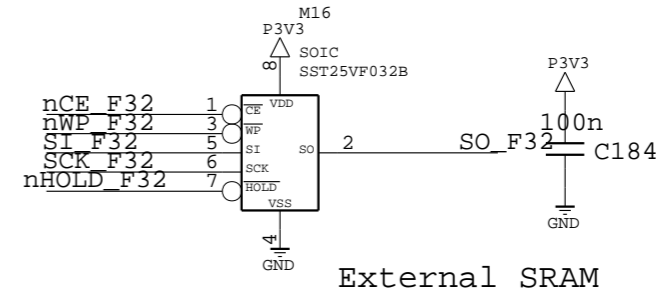
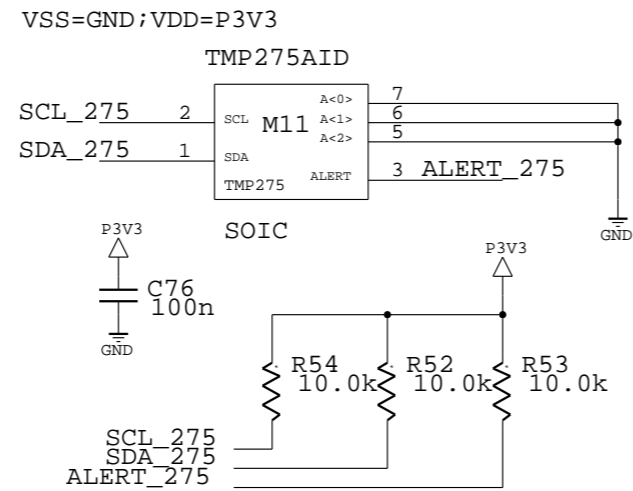


test_petiroc_2_bga_v1

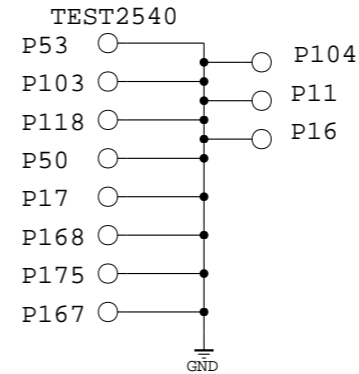
thermal probe



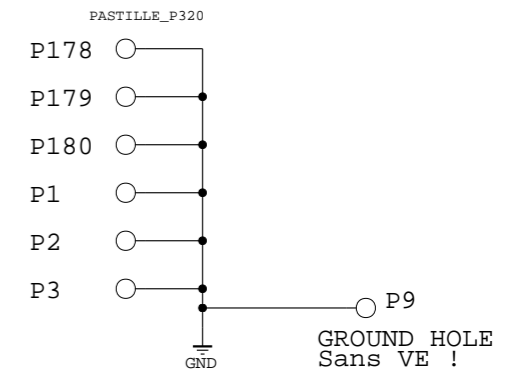
thermal probe



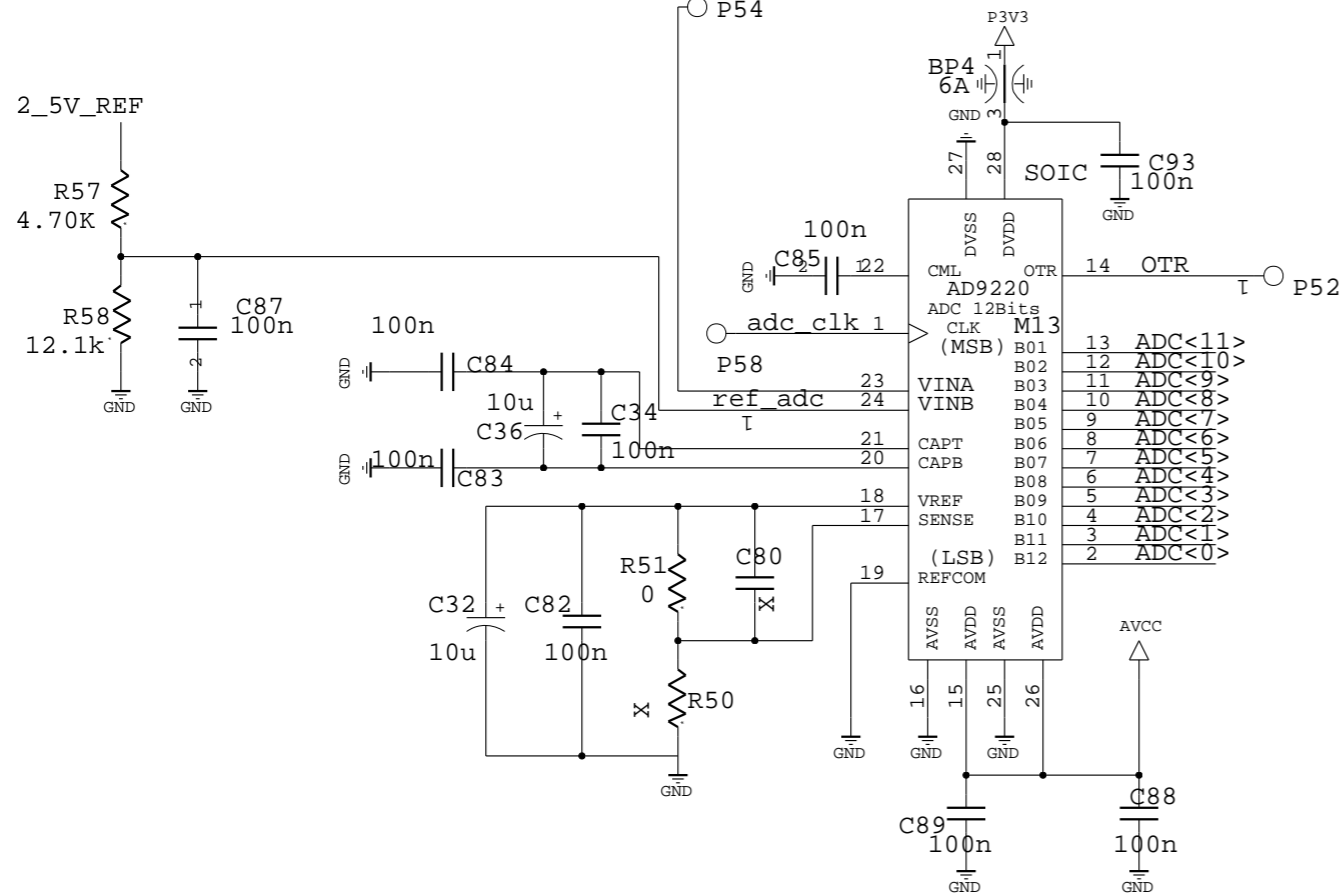
GROUND TEST POINTS



MECHANICAL FASTENING HOLES



data_adc



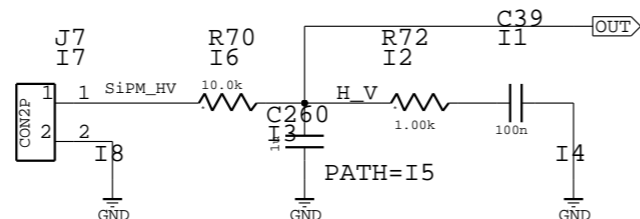
on board ADC

ALIGNMENT FOR CABLING

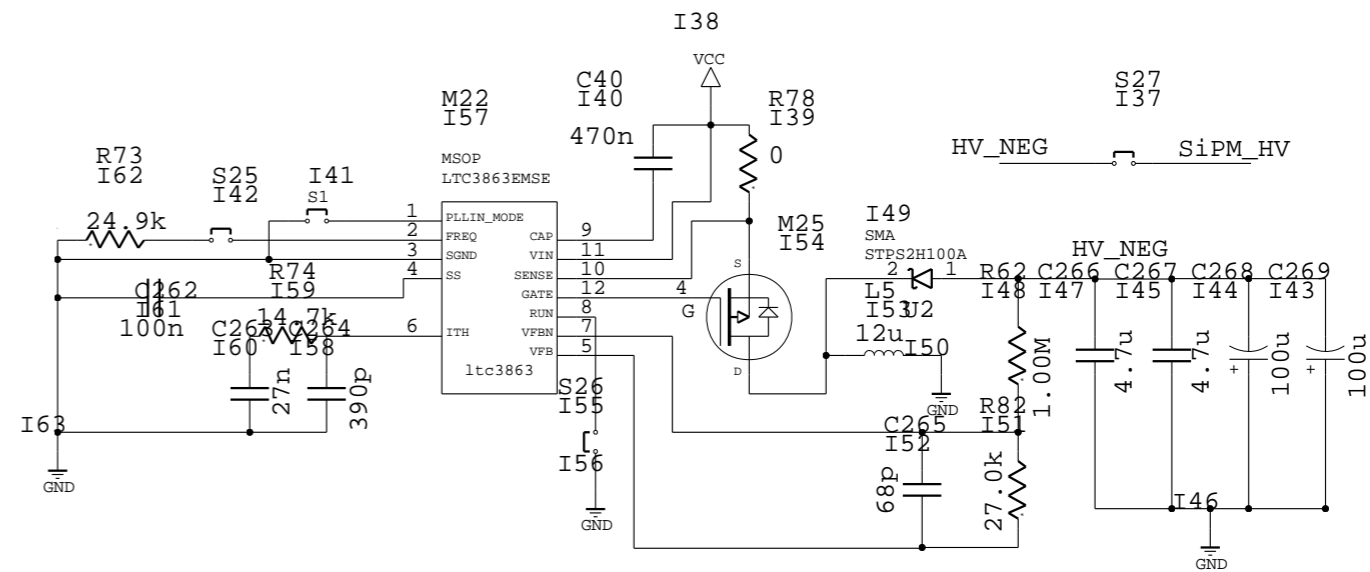
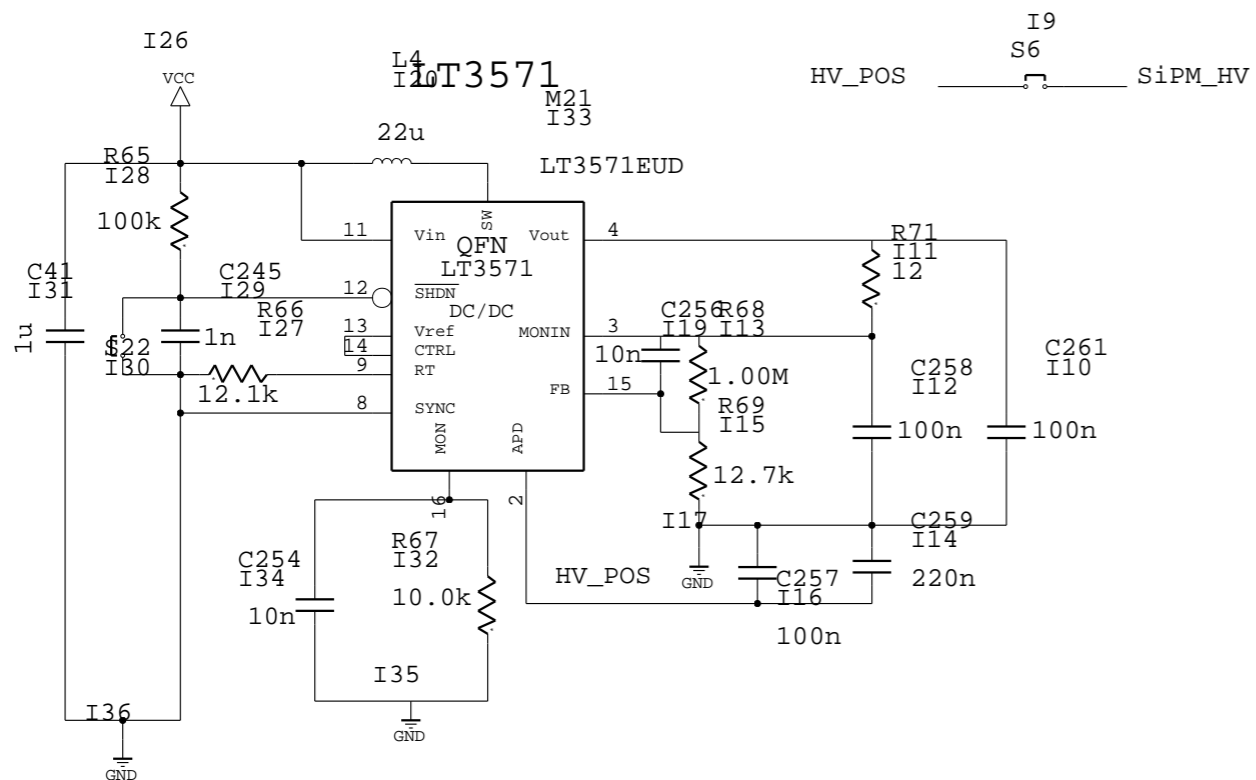
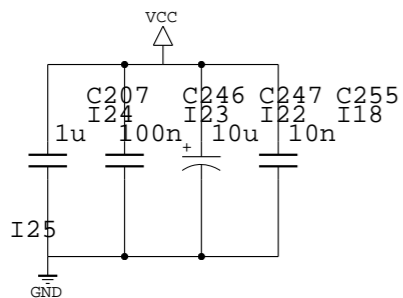


test_petiroc_2_bga_v1

HV_DECOUPLING



i21 High Voltage



mod_hv_pm

MODIFIE: Fri Mar 11 11:28:43 2016

ETUDE: PAGE: 1 / 1

DESSIN: SHEET: 10 / 10

