PSIROC ASIC Datasheet

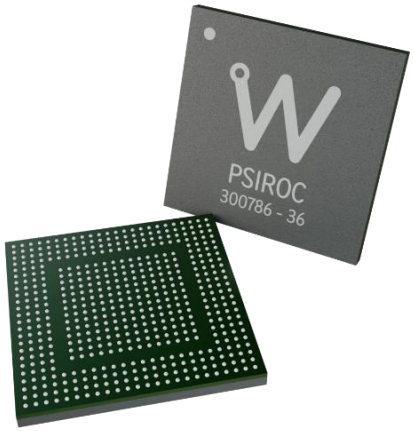
PSIROC
TSMC 013G
V 1.1

Psiroc is a 64-channel front-end ASIC designed to readout PIN diodes, silicon strips and GEMs, handling detector capacitances ranging from 0 up to few hundreds of pF.

Psiroc allows triggering down to 0.5 fC on sub-20pF detector capacitances and provides dual-gain energy measurement with excellent Signal-to-Noise Ratio on the high gain (SNR over 10 for 0.5 fC) and large dynamic range on the low gain. For input signals over few pC a channel-wise ToT output is also available. Psiroc can be programmed to output the shapers HG/LG, individual triggers or ToT signals (two output pins per channels). The preamplifier gain is adjustable from 125 mV/pC up to 4 V/pC.

Charge measurement is done with peak detectors but those can be used in a track & hold fashion thanks to an internal delay cell. Analog data are outputted on two multiplexed analog output and can be read-out with an external ADC. Shapers shaping time can be adjusted from 20 ns to 3 µs with a step of 20 ns up to 300 ns and a step of 200 ns up to 3 µs. Data acquisition can be done ASIC wide or channel-wise.

Channel-by-channel calibration on the trigger thresholds for time trigger and ToT can be done with individual 6-bit DACs.



Detector Read-Out	PIN Diodes, Silicon strips, GEMs
Number of Channels	64
Signal Polarity	Positive, negative
Sensitivity	Trigger on 0.5 fC on both polarity
Timing Resolution	< 150 ps RMS @ Q_{in} = 4 fC ; Cd/Cf = 20p/1p (pa gain = 1 V/pC)
Dynamic Range	Up to 5 pC with low gain charge measurement and up to 100 pC with ToT
Packaging & Dimension	BGA 20x20 mm^2
Power Consumption	350 mW – Supply voltage: 1.2 V
Inputs	64 analogue inputs
Outputs	2 outputs per channel, either: • 64 LVDS triggers • 2 x 64 TTL triggers • 64 TTL triggers and 64 analog outputs 2 multiplexed analogue outputs 3 NOR64 trigger outputs
Internal Programmable Features	3 trigger threshold tuning (10bits), channel-by-channel gain and shaping time adjustment (τ = 20 ns to 3 µs), individual trigger masking and cell powering.
Detector Read-Out	PIN Diodes, Silicon strips, GEMs

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Maximum ratings

001	Operating Temperature	ASIC operating temperature	-40	25	120	C
002	Power Supply	VDD_PA	1.08/2.25	1.2/2.5	1.32/2.75	V
003	Power Supply	VDD, DVDD	1.08	1.2	1.32	V
003	Ground	GND	0	0	0	V
004	Analog Inputs	in<0:63>	0	-	1.5	V
005	Digital Inputs (Single ended)	chip_id<0:3>, clk_sm_i2c, ck_read, rstn_read, rstn_probe, reset_n, resetn_i2c, rstn_sc, trig_ext, hold_ext	0	-	1.5	V
006	Digital Inputs (Differential -Common Mode)	valevent_n/p	520	580	640	mV
007	Digital Inputs (Differential - Swing)	valevent_n/p	300	410	410	mV
008	Digital Outputs (Single Ended)	errorn_sc, scl, sda, NOR_T1oc, NOR_T2oc, NOR_TQ, out_dprobe, out1<0:63>(Single ended mode), out2<0:63> >(Single ended mode)	1.08	1.2	1.32	V
009	Digital Outputs (Differential -Common Mode)	out1<0:63> (CLPS mode), out2<0:63> (CLPS mode)	520	580	640	mV
010	Digital Outputs (Differential - Swing)	out1<0:63> (CLPS mode), out2<0:63> (CLPS mode)	300	410	410	mV

Table 1 – Maximum ratings

ASIC Architecture

The block diagram of the ASIC is shown in Figure 1. The design is mostly an analog ASIC. In total there are 64 analog channels for signal triggering and pulse shaping.
The analog part consists of a charge pre-amplifier followed by a fast shaper and two slow shapers (Low gain & High Gain). Additionally, there is a charge trigger output taken directly from the Low Gain shaper output for charge veto. Each of the shapers has a dedicated peak detector cell.
On the backend there are two analog multiplexers which are used to output the peak detectors. For the three triggers (Times and Charge) there are NOR gate outputs. Lastly, there are 64 differential outputs which can be configured to output each channel trigger, single-ended or differential, or the slow shaper outputs.
The digital part is essentially an I^2C slave core IP used to handle the Slow Control[1] parameters to configure the ASIC.

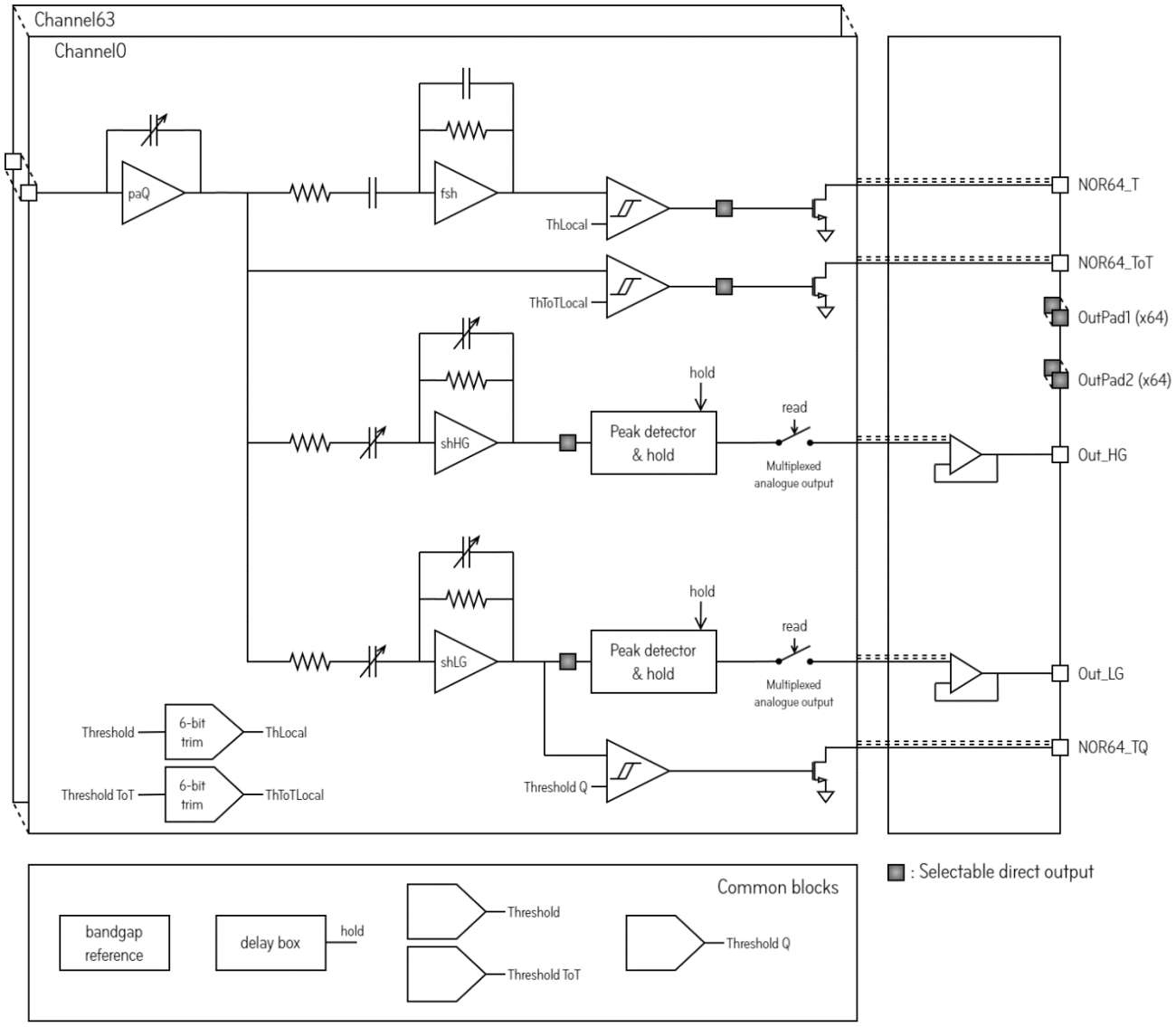


Figure 1 – ASIC block diagram

This ASIC design is optimized for PIN diodes, GEMs and silicon strips signals in both polarities, ranging from 0.5 fC up to 5 pC with low gain charge measurement and 100 pC with ToT. The design effort is mostly focused on the analog operation

[1] Slow Control stands for the register (TMR) storing the data for analogue block parameters.

of this ASIC. Most of the critical parts of the ASIC have been simulated at least in typical, best-case and worst-case corners. In typical, power supply is nominal at 1.2V, components are at nominal speed and temperature is equivalent to 27°C. In best-case, the components are set at fast speed, temperature is minimum at -40°C and power supply is boosted by 10% at 1.32 V. Lastly in worst-case, the components are set at slow speed, temperature is maximum at 125°C and power supply is reduced by 10% at 1.08 V.

Power consumption & DC levels

Following DC levels are observed at the references and biasing point of PSIROC with the default I²C configuration:

Signal name	*Description*	*Sim @ 27°C*
IB_PA	Bias current for charge preamplifier	1.728 V
THRESHOLD1	Threshold voltage for trigger T	380 mV
THRESHOLD2	Threshold voltage for trigger ToT	380 mV
THRESHOLDQ	Threshold voltage for trigger TQ	76 mV
VBG	Bandgap voltage	617 mV
VBIAS_1V	1V voltage regulator output	999 mV
VCASC_PA	Cascode voltage for charge preamplifier	849 mV
VCP_ABUFFER	Cascode voltage for analog mux & probe [PMOS]	800 mV
VCP_OUTING	Cascode voltage for channel shaper output [PMOS]	800 mV
VCP_PDETECTOR	Cascode voltage for channel peak detector [PMOS]	800 mV
VCN_ABUFFER	Cascode voltage for analog mux & probe [NMOS]	400 mV
VCN_OUTING	Cascode voltage for channel shaper output [NMOS]	400 mV
VCN_PDETECTOR	Cascode voltage for channel peak detector [NMOS]	400 mV
VREF_PA	Voltage reference for charge preamplifier (positive input only)	2.2 V
VREF_INV	Voltage reference for preamplifier inverting stage (negative input only)	1.25 V
VREF_DELAY	Voltage reference for delay box (ramp starting point)	100 mV
VREF_FSH	Voltage reference for fast shaper	400 mV
VREF_SH	Voltage reference for slow shapers	100 mV
VREF_THDAC	Voltage reference for dual-threshold DAC	380 mV
VREF_THDACQ	Voltage reference for energy veto threshold DAC	75 mV
VTH_DELAY	Threshold voltage for delay box	756 mV

Table 2 – DC points

Results are given for VDD_PA = 2.5 V. With VDD_PA = 1.2 V results for IB_PA, VREF_INV and VREF_PA will be modified accordingly. Power consumption of static power (amplifier biasing) has been simulated at 290 mA over 1.2V thus giving 350 mW for the full chip at room temperature and less than 5.5 mW per channel (x64). Around 40 % of the power consumption is sunk by the VDD_PA and 40 % is sunk by the VDD_PDETECTOR.

The power consumption is obtained without taking into account the probes and channel-by-channel analog buffers consumption. When the output pads are configured to output analog signals, the consumption is increased by 1.5 mA per active analog buffer (depending on the SC parameters controlling the buffer biasing at address 66).

I²C configuration

This ASIC can be configured using the I²C interface. The I²C slave core has been designed with SEU mitigations in place. Block diagrams, list of registers and registers writing sequences are depicted in Figure 2, Table 3 and Figure 3 respectively. Features of this IP are the following:

- Triplicated Design
- 256 addresses for the channel numbers
- 256 addresses for the register numbers
- 15 Chip ID numbers

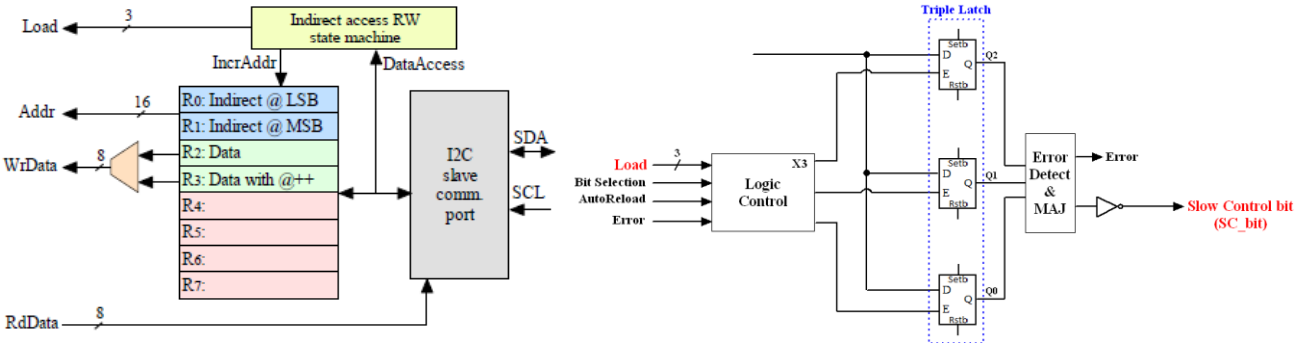


Figure 2 – Left: I2C slave core registers. Right: Slow Control bit cell design.

I2C Address	Register
0	ASIC parameter address (LSB): Channel
1	ASIC parameter address (MSB): Register
2	Data Read/to Write
3	Data with auto-incremental Address
4-5-6	TBD
7	Status register (error, parity)

Table 3 – I2C slave core register descriptions.

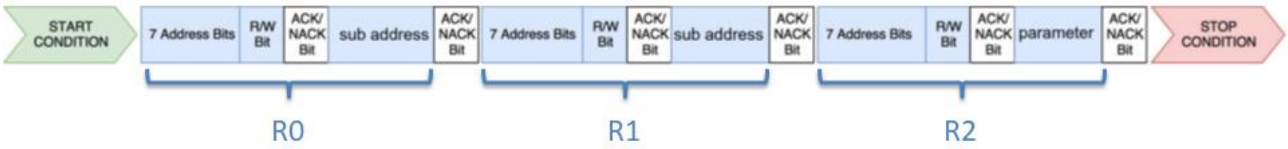


Figure 3 – I2C registers writing sequences.

There are two ways of addressing the Slow Control parameter sub-address. The first one is to read or write each sub-address directly as depicted in Figure 4. The second one adds the possibility of auto incrementing the sub-address based on the previous sub-address. This procedure is shown in Figure 5.

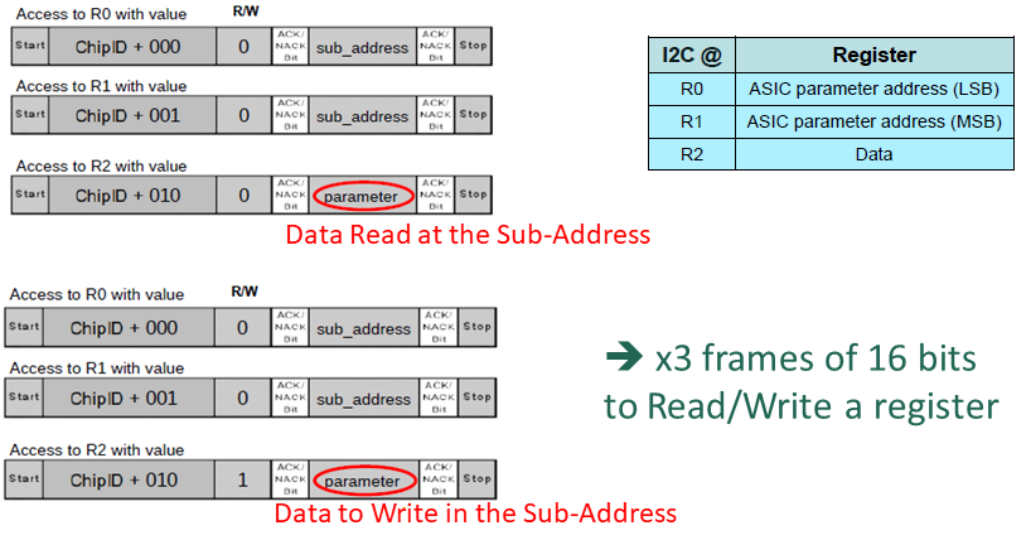


Figure 4 – Slow Control simple or direct parameter sub-addressing procedure.

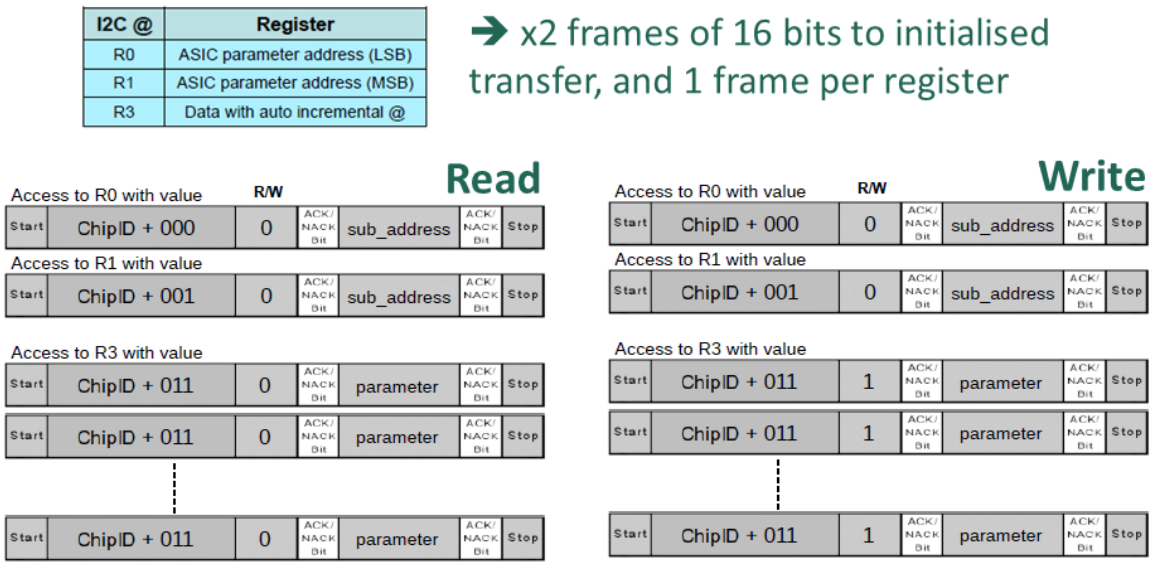


Figure 5 – Slow Control auto-increment parameter sub-addressing procedure.

Slow Control parameters available for this ASIC are listed in Table 4. "NC" term denotes non used Slow Control bits. Data in "Address" and "Subadd" columns denote the sub-addresses R0 & R1 in the writing sequences respectively (Figure 3). Data payload in R2 (direct parameter addressing – Figure 4) or R3 (auto-increment addressing – Figure 5) will be based on data in "Parameters or Default Value" column. The address configuration has been arranged in the following way:

- 0-63: channel wise configuration (with the address corresponding to the channel number);
- 64: ASIC biasing;
- 65: common blocks;
- 66: outing;
- 67: event validation gating.

Address	Subadd	Bit#	Default value	Name	Description
0-63	0	7	0	NC	Not Connected
		6	0	polarity	Polarity 0 – negative input (default) 1 – positive input
		[5-0]	001000	paGain[5:0]	Preamplifier gain Cf = 125 fF – 8 pF
	1	[7-6]	00	NC	Not Connected
		[5-0]	001000	paComp[5:0]	Preamplifier compensation Ccomp = 0 – 7,875 pF
	2	7	0	slowShapingHG,	Toggle bit for the high gain shaping time LSB 0 – 20 ns (default) 1 – 200 ns
		6	0	slowShapingLG	Toggle bit for the low gain shaping time LSB 0 – 20 ns (default) 1 – 200 ns
		[5-3]	000	Ileak[2:0]	Adjust DC feedback to account for leakage current from detector
		[2-0]	000	Ccomp_fsh[2:0]	Fast shaper compensation
	3	[7-4]	0001	tauLG[3:0]	Shaping time of low gain shaper 20 ns – 300 ns with 20 ns LSB or 200 ns – 3 µs with 200 ns LSB.
		[3-0]	0001	tauHG[3:0]	Shaping time of high gain shaper 20 ns – 300 ns with 20 ns LSB or 200 ns – 3 µs with 200 ns LSB.
	4	[7-6]	00	NC	Not Connected
		[5-0]	000000	calibDacT[5:0]	Threshold calibration DAC for trigger T ($V_{thresholdT}$ - 15 mV – 0 mV)
	5	[7-6]	00	NC	Not Connected
		[5-0]	000000	calibDacToT[5:0]	Threshold calibration DAC for ToT ($V_{thresholdToT}$ - 15 mV – 0 mV)
	6	[7-5]	011	NC	Not Connected
		4	1	EN_fsh	Enable bit for fast shaper 0 – disable fast shaper 1 – enable fast shaper (default)
		3	1	EN_pa	Enable bit for preamplifier 0 – disable preamplifier 1 – enable preamplifier (default)
		2	1	EN_discriT	Enable bit for trigger discriminator 0 – disable trigger discriminator 1 – enable trigger discriminator (default)
		1	1	EN_discriToT	Enable bit for ToT discriminator

					0 – disable ToT discriminator 1 – enable ToT discriminator (default)
		0	1	EN_discriCharge	Enable bit for charge discriminator 0 – disable charge discriminator 1 – enable charge discriminator (default)
	7	[7-5]	000	NC	Not Connected
		4	0	EN_Ctest	Enable bit for Ctest 0 – disable Ctest (default) 1 – enable Ctest
		3	1	EN_shLG	Enable bit for low gain shaper 0 – disable shaper low gain 1 – enable shaper low gain (default)
		2	1	EN_shHG	Enable bit for high gain shaper 0 – disable shaper high gain 1 – enable shaper high gain (default)
		1	1	EN_pdetLG	Enable bit for low gain peak detector 0 – disable peak detector low gain 1 – enable peak detector low gain (default)
		0	1	EN_pdetHG	Enable bit for high gain peak detector 0 – disable peak detector high gain 1 – enable peak detector high gain (default)
	66	[7-5]	000	NC	Not Connected
		4	0	cmd_TQ	Probe switch command for the charge trigger 0 – disabled (default) 1 – enabled
		3	0	cmd_shhg	Probe switch command for the shaper high gain 0 – disabled (default) 1 – enabled
		2	0	cmd_shlg	Probe switch command for the shaper low gain 0 – disabled (default) 1 – enabled
		1	0	cmd_fsh	Probe switch command for the fast shaper 0 – disabled (default) 1 – enabled
		0	0	cmd_pa	Probe switch command for the preamplifier 0 – disabled (default) 1 – enabled

64	0	[7-4]	0100	ibi_pa[3:0]	Preamplifier first stage bias current
		[3-0]	0100	ibo_pa[3:0]	Preamplifier output stage bias current
	1	[7-4]	0100	ibshift_ota[3:0]	Preamplifier feedback OTA bias current
		[3-0]	0100	ib_ota[3:0]	
	2	[7-4]	0100	ibi_inv[3:0]	Preamplifier inverter first stage bias current

		[3-0]	0100	ibo_inv[3:0]	Preamplifier inverter output stage bias current
	3	[7-4]	0100	ibi_fsh[3:0]	Fast shaper input stage bias current
		[3-0]	0100	ibo_fsh[3:0]	Fast shaper output stage bias current
	4	[7-4]	0100	ibi_shHg[3:0]	Slow shaper high gain first stage bias current
		[3-0]	0100	ibo_shHg[3:0]	Slow shaper high gain output stage bias current
	5	[7-4]	0100	ibi_shLg[3:0]	Slow shaper low gain first stage bias current
		[3-0]	0100	ibo_shLg[3:0]	Slow shaper low gain output stage bias current
	6	[7-4]	0100	ibi_pdetector[3:0]	Peak detector amplifier first stage bias current
		[3-0]	0100	ibi_pdBuffer[3:0]	Peak detector buffer first stage bias current
	7	[7-4]	0100	ibFCP_pdetector[3:0]	Peak detector amplifier second stage bias current
		[3-0]	0100	ibFCN_pdetector[3:0]	Peak detector amplifier second stage bias current
	8	[7-4]	0100	ibFCP_pdBuffer[3:0]	Peak detector buffer second stage bias current
		[3-0]	0100	ibFCN_pdBuffer[3:0]	Peak detector buffer second stage bias current
	9	[7-4]	0100	ibi_discri1[3:0]	Discriminator T first stage bias current
		[3-0]	0100	ibm1_discri1[3:0]	Discriminator T second stage bias current
	10	[7-4]	0100	ibm2_discri1[3:0]	Discriminator T third stage bias current
		[3-0]	0100	ibi_discri2[3:0]	Discriminator ToT first stage bias current
	11	[7-4]	0100	ibm1_discri2[3:0]	Discriminator ToT second stage bias current
		[3-0]	0100	ibm2_discri2[3:0]	Discriminator ToT third stage bias current
	12	[7-4]	0100	ibi_discriCharge[3:0]	Discriminator Q first stage bias current
		[3-0]	0100	ibo_discriCharge[3:0]	Discriminator Q second stage bias current
	13	[7-4]	0100	ib_calibDac[3:0]	threshold calibration DAC bias current
		[3-2]	11	NC	Not Connected
		1	1	ON_pa	Power ON bit for preamplifier 0 – OFF 1 – ON (default)
		0	1	ON_fsh	Power ON bit fast shaper 0 – OFF 1 – ON (default)
	14	7	1	ON_shHG	Power ON bit for high gain slow shaper 0 – OFF 1 – ON (default)
		6	1	ON_shLG	Power ON bit for low gain slow shaper 0 – OFF 1 – ON (default)
		5	1	ON_pdetector	Power ON bit for peak detectors 0 – OFF

					1 – ON (default)
		4	1	ON_calibDac	Power ON bit for calibration DACs 0 – OFF 1 – ON (default)
		3	1	ON_discriCharge	Power ON bit for charge discriminator 0 – OFF 1 – ON (default)
		2	1	ON_pdBuffer	Power ON bit for peak detector buffers 0 – OFF 1 – ON (default)
		1	1	ON_discriT	Power ON bit for trigger discriminator 0 – OFF 1 – ON (default)
		0	1	ON_discriToT	Power ON bit for ToT discriminator 0 – OFF 1 – ON (default)

65	0	[7-6]	00	NC	Not Connected
		[5-0]	100000	bg[5:0]	bandgap temperature deviation trimming
	1	[7-0]	00000000	DacT[7-0]	Set Trigger threshold (Low): Bits [7-0]
	2	[7-2]	000000	DacToT[5-0]	Set ToT Trigger threshold (High): Bits [5-0]
		[1-0]	00	DacT[9-8]	Set Time Trigger threshold (Low): Bits [9-8]
	3	[7-4]	0000	DacQ[3-0]	Set Charge Trigger threshold: Bits [3-0]
		[3-0]	0000	DacToT[9-6]	Set ToT Trigger threshold (High): Bits [9-6]
	4	[7-6]	00	NC	Not Connected
		[5-0]	000000	DacQ[9-4]	Set Charge Trigger threshold: Bits [9-4]
	5	[7-4]	0100	Ibi_thresholdDac[3:0]	Set Time threshold DAC input stage bias
		[3-0]	0100	Ibo_thresholdDac[3:0]	Set Time threshold DAC output stage bias
	6	[7-4]	0100	Ibi_thresholdDacQ[3:0]	Set Charge threshold DAC input stage bias
		[3-0]	0100	Ibo_thresholdDacQ[3:0]	Set Charge threshold DAC output stage bias
	7	[7-4]	0000	vbias[3:0]	vbias_1v DC value trimming
		3	1	EN_thT	Enable bit for thresholdT 0 – disabled 1 – enabled (default)
		2	1	EN_thToT	Enable bit for thresholdToT 0 – disabled 1 – enabled (default)
		1	1	EN_thQ	Enable bit for thresholdQ 0 – disabled 1 – enabled (default)
		0	1	EN_bg	Enable bit for bandgap 0 – disabled 1 – enabled (default)
	8		11111111	delay[7:0]	Delay box trimming value. Total delay is delay × 0.85ns × slopeTrim.

	9	[7-4]	0100	slopeTrim[3:0]	Set delay slope value to adjust the delay dynamic range. Total delay is delay × 0.85ns × slopeTrim.
		[3-0]	0100	ibi_discri_delay[3:0]	Delay discriminator first stage bias current
	10	[7-4]	0100	ibm_discri_delay[3:0]	Delay discriminator second stage bias current
		[3-0]	0100	ibo_discri_delay[3:0]	Delay discriminator third stage bias current
	11	[7-4]	0100	ibi_delayDac[3:0]	Delay threshold DAC first stage bias current
		[3-0]	0100	ibo_delayDac[3:0]	Delay threshold DAC output stage bias current
	12		1	hysteresisT	Enable hysteresis for trigger T 0 – disable 1 – enable (default)
			1	hysteresisToT	Enable hysteresis for trigger ToT 0 – disable 1 – enable (default)
			1	EN_delay	Enable bit for the delay box 0 – disable 1 – enable (default)
			0	selHoldExt	External hold selection bit 0 – internal (default) 1 – external
			0100	selTrig[3:0]	Trigger selection for peak detector and delay box. See section Peak detectors
	66	[7-2]	000000	NC	Not Connected
		1	0	cmd_globalTrigger	Probe switch command for the global trigger 0 – disabled (default) 1 – enabled
		0	0	cmd_hold	Probe switch command for hold signal 0 – disabled (default) 1 – enabled

66	0	[7-6]	00	cm[1:0],	outing selection for channel 0
		[5-4]	11	lvdsOut[1:0]	
		[3-2]	00	outPad2[1:0]	
		[1-0]	00	outPad[1:0]	
	1	[7-6]	00	cm[1:0],	outing selection for channel 1
		[5-4]	11	lvdsOut[1:0]	
		[3-2]	00	outPad2[1:0]	
		[1-0]	00	outPad[1:0]	
	...	...	...	...	...
	63	[7-6]	00	cm[1:0],	outing selection for channel 63
		[5-4]	11	lvdsOut[1:0]	
		[3-2]	00	outPad2[1:0]	
		[1-0]	00	outPad[1:0]	

	64	7	0	extendedOutput	Toggle to extended output mode: 0 – disabled (default) 1 – enabled
		[6-5]	01	delayPE[1:0]	Setting for CLPS driver pre-emphasis delay
		[4-0]	00000	bufSize[4:0]	Set buffer size for single ended trigger output
	65	[7-4]	1111	bufSizeClps[3:0]	Setting for CLPS driver strength
		[3-0]	1111	bufSizePE[3:0]	Setting for CLPS driver pre-emphasis
	66	[7-6]	11	NC	Not Connected
		[5-4]	11	cmProbe[1:0]	Set compensation capacitor value for probe buffer
		[3-2]	11	cmLG[1:0]	Set compensation capacitor value for low gain buffer
		[1-0]	11	cmHG[1:0]	Set compensation capacitor value for high gain buffer
	67	[7-4]	0100	ibi_aBuffer[3:0]	Set analog buffers first stage bias current (probe and OUT_AMUXLG/HG)
		[3-0]	0100	ibFCP_aBuffer[3:0]	Set analog buffers second stage bias current (probe and OUT_AMUXLG /HG)
	68	[7-4]	0100	ibFCN_aBuffer[3:0]	Set analog buffers second stage bias current (probe and OUT_AMUXLG /HG)
		[3-0]	0100	ibi_outing[3:0]	Set analog buffers first stage bias current (OUT1 and OUT2)
	69	[7-4]	0100	ibFCP_outing[3:0]	Set analog buffers second stage current (OUT1 and OUT2)
		[3-0]	0100	ibFCN_outing[3:0]	Set analog buffers second stage current (OUT1 and OUT2)
	70	[7-5]	000	NC	Not Connected
		4	0	ON_outing	Power on bit for analogue buffers driving OUT1 and OUT2
		3	1	ON_aBuffer	Power on bit for probe and analog multiplexer's buffers
		2	0	EN_probe	Enable bit for analogue probe
		1	1	EN_aMuxHG	Enable bit for multiplexer buffer for high gain measurement
		0	1	EN_aMuxLG	Enable bit for analogue probe, multiplexer buffer for low gain measurement

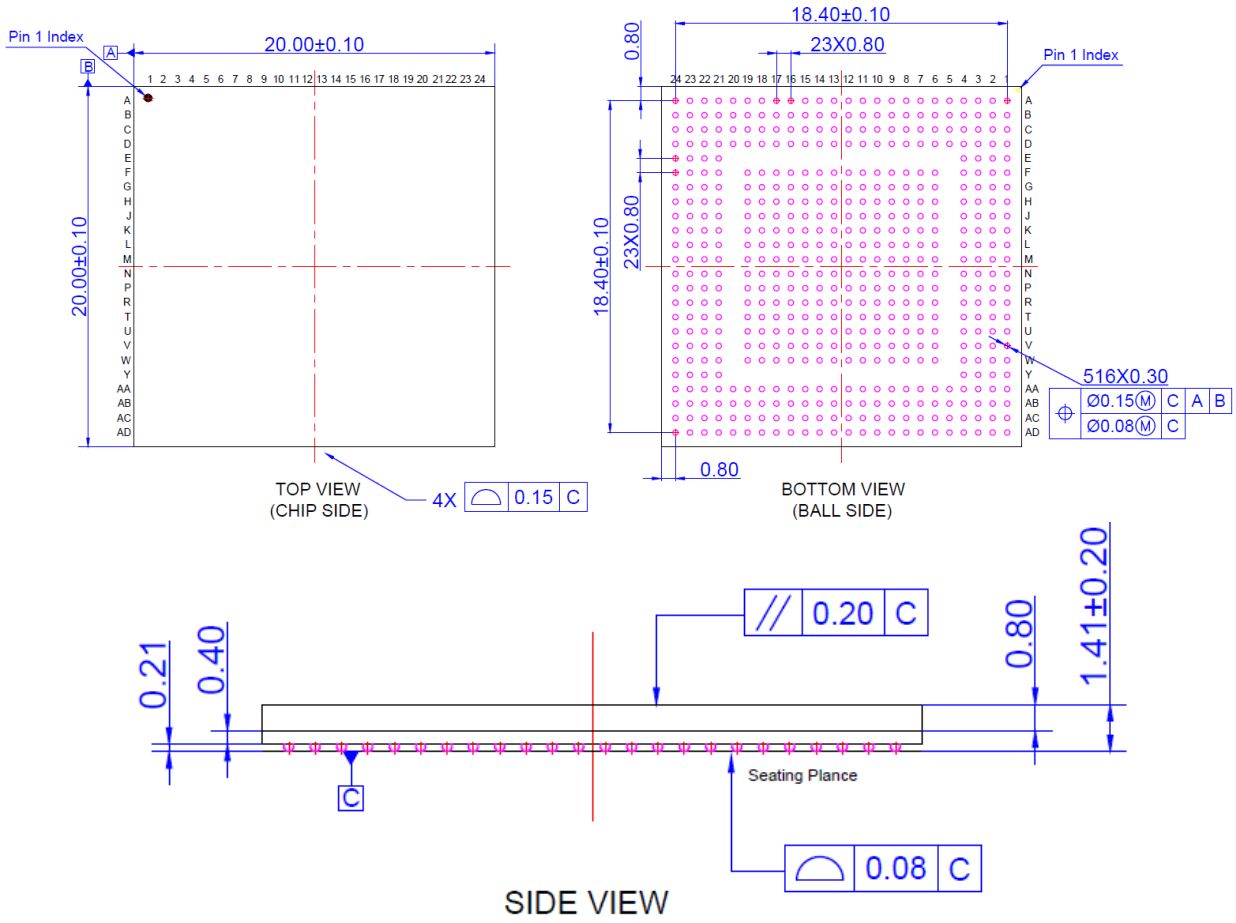
67	0	[7-2]	000000	NC	Not Connected
		1	1	EN_Rx	Enable bit for the differential receiver (valid event signal) 0 – Disable 1 – Enable (default)
		0	0	Forced_ValEvt	Enable bit for forced valid event bit 0 – External (default) 1 – Internal

Table 4 – PSIROC Slow Control list

Specifically, for Address 0-63, each subadd in this section will correspond only to the selected channel. This means that in order to have channel wide operation each Address will have to be selected when writing the Slow Control operation. All the other Addresses (64-67) operations will be effective for the whole ASIC.

Pinout, Power supplies & mechanics

Mechanics



Ball-out

	1	2	3	4	5	6	7	8	9	10	11	12
A	in<53>	in<55>	in<57>	in<59>	in<61>	in<63>	in<62>	reset_n	sda	clk_sm_i2c	valevent_n	valevent_p
B	in<51>	in<52>	in<54>	in<56>	in<58>	in<60>	in_ctest	rstn_probe	rstn_i2c	scl	rstn_sc	GND
C	in<49>	in<50>	vcp_outing	NC	NC	NC	NC	NC	NC	NC	NC	GND
D	in<47>	in<48>	vcn_outing	NC	NC	NC	NC	NC	NC	NC	NC	GND
E	in<45>	in<46>	vcp_aBuffer	NC								
F	in<43>	in<44>	vcn_aBuffer	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
G	in<41>	in<42>	vref_thDacQ	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
H	in<39>	in<40>	vref_thDac	NC		VDD	VDD	NC	GND	GND	GND	GND
J	in<37>	in<38>	thresholdQ	NC		VDD	VDD	NC	GND	GND	GND	GND
K	in<35>	in<36>	thresholdToT	NC		VDD	VDD	NC	GND	GND	GND	GND
L	in<33>	in<34>	threshold	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
M	out_aMuxLG	in<32>	out_aprobe	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
N	out_aMuxHG	in<30>	vref_inv	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
P	in<31>	in<28>	vbg	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
R	in<29>	in<26>	vbias_1v	NC		VDD	VDD	NC	GND	GND	GND	GND
T	in<27>	in<24>	vcasc_pa	NC		VDD	VDD	NC	GND	GND	GND	GND
U	in<25>	in<22>	vref_pa	NC		VDD	VDD	NC	GND	GND	GND	GND
V	in<23>	in<20>	vref_fsh	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
W	in<21>	in<18>	vref_sh	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
Y	in<19>	in<16>	vcp_pdetect	NC								
Z	in<17>	in<14>	vcn_pdetect	NC	NC	NC	NC	NC	NC	NC	NC	GND
AA	in<15>	in<12>	vref_delay	NC	NC	NC	NC	NC	NC	NC	NC	GND
AB	in<13>	in<10>	in<8>	in<6>	in<4>	in<2>	Vth_delay	ib_pa	NC	NC	NC	GND
AC	in<11>	in<9>	in<7>	in<5>	in<3>	in<1>	in<0>	reserved	holdExt	out_dprobe	trigExt	NOR_T1oc
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 6 – PSIROC Ball-out East part

13	14	15	16	17	18	19	20	21	22	23	24	
ck_read	rstn_read	out1<62>	out2<62>	out1<63>	out2<63>	out1<61>	out2<61>	out1<52>	out2<52>	out1<53>	out2<53>	A
NC	NC	out1<60>	out2<60>	out1<56>	out2<56>	out1<59>	out2<59>	out1<50>	out2<50>	out1<51>	out2<51>	B
NC	NC	out1<58>	out2<58>	out1<54>	out2<54>	out1<57>	out2<57>	out1<48>	out2<48>	out1<49>	out2<49>	C
NC	NC	NC	NC	NC	NC	out1<55>	out2<55>	out1<46>	out2<46>	out1<47>	out2<47>	D
								out1<44>	out2<44>	out1<45>	out2<45>	E
DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		out1<42>	out2<42>	out1<43>	out2<43>	F
DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		out1<40>	out2<40>	out1<41>	out2<41>	G
GND	GND	GND	GND	GND	DVDD	DVDD		out1<38>	out2<38>	out1<39>	out2<39>	H
GND	GND	GND	GND	GND	DVDD	DVDD		out1<36>	out2<36>	out1<37>	out2<37>	J
GND	GND	GND	GND	GND	DVDD	DVDD		out1<34>	out2<34>	out1<35>	out2<35>	K
GND	GND	GND	GND	GND	DVDD	DVDD		out1<32>	out2<32>	out1<33>	out2<33>	L
GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	chip_id<0>	errorn_sc	M
GND	GND	GND	GND	GND	DVDD	DVDD		NC	chip_id<3>	chip_id<2>	chip_id<1>	N
GND	GND	GND	GND	GND	DVDD	DVDD		out1<30>	out2<30>	out1<31>	out2<31>	P
GND	GND	GND	GND	GND	DVDD	DVDD		out1<28>	out2<28>	out1<29>	out2<29>	R
GND	GND	GND	GND	GND	DVDD	DVDD		out1<26>	out2<26>	out1<27>	out2<27>	T
GND	GND	GND	GND	GND	DVDD	DVDD		out1<24>	out2<24>	out1<25>	out2<25>	U
DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		out1<22>	out2<22>	out1<23>	out2<23>	V
DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		out1<20>	out2<20>	out1<21>	out2<21>	W
								out1<18>	out2<18>	out1<19>	out2<19>	Y
NC	NC	NC	NC	NC	NC	out1<9>	out2<9>	out1<16>	out2<16>	out1<17>	out2<17>	Z
NC	NC	out1<4>	out2<4>	out1<8>	out2<8>	out1<7>	out2<7>	out1<14>	out2<14>	out1<15>	out2<15>	AA
NC	NC	out1<2>	out2<2>	out1<6>	out2<6>	out1<5>	out2<5>	out1<12>	out2<12>	out1<13>	out2<13>	AB
NOR_T2oc	NOR_TQoc	out1<0>	out2<0>	out1<1>	out2<1>	out1<3>	out2<3>	out1<10>	out2<10>	out1<11>	out2<11>	AC
13	14	15	16	17	18	19	20	21	22	23	24	

Figure 7 – PSIROC ball-out West part

PSIROC pinout

Net Name	BGA Ball	Type
OUT_AMUXLG	N1	Multiplexed Analog Output
OUT_AMUXHG	M1	
OUT_APROBE	M3	
IB_PA	AB8	Voltage Reference
RESERVED	AC8	
THRESHOLD	L3	
THRESHOLDTOT	K3	
THRESHOLDQ	J3	
VBG	P3	
VBIAS_1V	R3	
VREF_FSH	V3	
VREF_PA	U3	
VCN_ABUFFER	F3	
VCN_OUTING	D3	
VCN_PDETECTOR	Z3	
VCP_ABUFFER	E3	
VCP_OUTING	C3	
VCP_PDETECTOR	Y3	
VREF_INV	N3	
VREF_DELAY	AA3	
VCASC_PA	T3	
VREF_SH	W3	
VREF_THDAC	H3	
VREF_THDACQ	G3	
VTH_DELAY	AB7	
IN_CTEST	B7	Analog Input
CHIP_ID<0>	M23	I/O Digital Single Ended
CHIP_ID<1>	N24	
CHIP_ID<2>	N23	
CHIP_ID<3>	N22	
CK_READ	A13	
CLK_SM_I2C	A10	
ERRORN_OC	M24	
HOLDEXT	AC9	
NOR_T1OC	AC12	
NOR_T2OC	AC13	
NOR_TQOC	AC14	
OUT_DPROBE	AC10	
RESET_N	A8	
RSTN_I2C	B9	
RSTN_PROBE	B8	
RSTN_READ	A14	
RSTN_SC	B11	
SCL	B10	
SDA	A9	
TRIGEXT	AC11	
DVDD	F13	Power Supply - DVDD
DVDD	F14	
DVDD	F15	
DVDD	F16	
DVDD	F17	
DVDD	F18	
DVDD	F19	
DVDD	G13	
DVDD	G14	
DVDD	G15	
DVDD	G16	
DVDD	G17	
DVDD	G18	
DVDD	G19	
DVDD	H18	
DVDD	H19	
DVDD	J18	
DVDD	J19	
DVDD	K18	
DVDD	K19	
DVDD	L18	
DVDD	L19	
DVDD	M18	
DVDD	M19	
DVDD	N18	
DVDD	N19	
DVDD	P18	
DVDD	P19	
DVDD	R18	
DVDD	R19	
DVDD	T18	
DVDD	T19	

DVDD	U18	
DVDD	U19	
DVDD	V13	
DVDD	V14	
DVDD	V15	
DVDD	V16	
DVDD	V17	
DVDD	V18	
DVDD	V19	
DVDD	W13	
DVDD	W14	
DVDD	W15	
DVDD	W16	
DVDD	W17	
DVDD	W18	
DVDD	W19	
GND	AA12	Ground
GND	AB12	
GND	B12	
GND	C12	
GND	D12	
GND	F12	
GND	G12	
GND	H9	
GND	H10	
GND	H11	
GND	H12	
GND	H13	
GND	H14	
GND	H15	
GND	H16	
GND	H17	
GND	J9	
GND	J10	
GND	J11	
GND	J12	
GND	J13	
GND	J14	
GND	J15	
GND	J16	
GND	J17	
GND	K9	
GND	K10	
GND	K11	
GND	K12	
GND	K13	
GND	K14	
GND	K15	
GND	K16	
GND	K17	
GND	L9	
GND	L10	
GND	L11	
GND	L12	
GND	L13	
GND	L14	
GND	L15	
GND	L16	
GND	L17	
GND	M9	
GND	M10	
GND	M11	
GND	M12	
GND	M13	
GND	M14	
GND	M15	
GND	M16	
GND	M17	
GND	N9	
GND	N10	
GND	N11	
GND	N12	
GND	N13	
GND	N14	
GND	N15	
GND	N16	
GND	N17	
GND	P9	
GND	P10	
GND	P11	
GND	P12	
GND	P13	
GND	P14	
GND	P15	

GND	P16	
GND	P17	
GND	R9	
GND	R10	
GND	R11	
GND	R12	
GND	R13	
GND	R14	
GND	R15	
GND	R16	
GND	R17	
GND	T9	
GND	T10	
GND	T11	
GND	T12	
GND	T13	
GND	T14	
GND	T15	
GND	T16	
GND	T17	
GND	U9	
GND	U10	
GND	U11	
GND	U12	
GND	U13	
GND	U14	
GND	U15	
GND	U16	
GND	U17	
GND	V12	
GND	W12	
GND	Z12	
IN<0>	AC7	Analog Input
IN<1>	AC6	
IN<2>	AB6	
IN<3>	AC5	
IN<4>	AB5	
IN<5>	AC4	
IN<6>	AB4	
IN<7>	AC3	
IN<8>	AB3	
IN<9>	AC2	
IN<10>	AB2	
IN<11>	AC1	
IN<12>	AA2	
IN<13>	AB1	
IN<14>	Z2	
IN<15>	AA1	
IN<16>	Y2	
IN<17>	Z1	
IN<18>	W2	
IN<19>	Y1	
IN<20>	V2	
IN<21>	W1	
IN<22>	U2	
IN<23>	V1	
IN<24>	T2	
IN<25>	U1	
IN<26>	R2	
IN<27>	T1	
IN<28>	P2	
IN<29>	R1	
IN<30>	N2	
IN<31>	P1	
IN<32>	M2	
IN<33>	L1	
IN<34>	L2	
IN<35>	K1	
IN<36>	K2	
IN<37>	J1	
IN<38>	J2	
IN<39>	H1	
IN<40>	H2	
IN<41>	G1	
IN<42>	G2	
IN<43>	F1	
IN<44>	F2	
IN<45>	E1	
IN<46>	E2	
IN<47>	D1	
IN<48>	D2	
IN<49>	C1	
IN<50>	C2	
IN<51>	B1	

IN<52>	B2	
IN<53>	A1	
IN<54>	B3	
IN<55>	A2	
IN<56>	B4	
IN<57>	A3	
IN<58>	B5	
IN<59>	A4	
IN<60>	B6	
IN<61>	A5	
IN<62>	A7	
IN<63>	A6	
VDD_PA	F6	Power Supply - VDD_PA
VDD_PA	F7	
VDD_PA	F8	
VDD_PA	G6	
VDD_PA	G7	
VDD_PA	G8	
VDD_PA	L6	
VDD_PA	L7	
VDD_PA	M6	
VDD_PA	M7	
VDD_PA	N6	
VDD_PA	N7	
VDD_PA	P6	
VDD_PA	P7	
VDD_PA	V6	
VDD_PA	V7	
VDD_PA	V8	
VDD_PA	W6	
VDD_PA	W7	
VDD_PA	W8	
OUT2<0>	AC16	I/O Digital Differential (1GHz)
OUT2<1>	AC18	
OUT2<2>	AB16	
OUT2<3>	AC20	
OUT2<4>	AA16	
OUT2<5>	AB20	
OUT2<6>	AB18	
OUT2<7>	AA20	
OUT2<8>	AA18	
OUT2<9>	Z20	
OUT2<10>	AC22	
OUT2<11>	AC24	
OUT2<12>	AB22	
OUT2<13>	AB24	
OUT2<14>	AA22	
OUT2<15>	AA24	
OUT2<16>	Z22	
OUT2<17>	Z24	
OUT2<18>	Y22	
OUT2<19>	Y24	
OUT2<20>	W22	
OUT2<21>	W24	
OUT2<22>	V22	
OUT2<23>	V24	
OUT2<24>	U22	
OUT2<25>	U24	
OUT2<26>	T22	
OUT2<27>	T24	
OUT2<28>	R22	
OUT2<29>	R24	
OUT2<30>	P22	
OUT2<31>	P24	
OUT2<32>	L22	
OUT2<33>	L24	
OUT2<34>	K22	
OUT2<35>	K24	
OUT2<36>	J22	
OUT2<37>	J24	
OUT2<38>	H22	
OUT2<39>	H24	
OUT2<40>	G22	
OUT2<41>	G24	
OUT2<42>	F22	
OUT2<43>	F24	
OUT2<44>	E22	
OUT2<45>	E24	
OUT2<46>	D22	
OUT2<47>	D24	
OUT2<48>	C22	
OUT2<49>	C24	
OUT2<50>	B22	
OUT2<51>	B24	

OUT2<52>	A22	
OUT2<53>	A24	
OUT2<54>	C18	
OUT2<55>	D20	
OUT2<56>	B18	
OUT2<57>	C20	
OUT2<58>	C16	
OUT2<59>	B20	
OUT2<60>	B16	
OUT2<61>	A20	
OUT2<62>	A16	
OUT2<63>	A18	
OUT1<0>	AC15	
OUT1<1>	AC17	
OUT1<2>	AB15	
OUT1<3>	AC19	
OUT1<4>	AA15	
OUT1<5>	AB19	
OUT1<6>	AB17	
OUT1<7>	AA19	
OUT1<8>	AA17	
OUT1<9>	Z19	
OUT1<10>	AC21	
OUT1<11>	AC23	
OUT1<12>	AB21	
OUT1<13>	AB23	
OUT1<14>	AA21	
OUT1<15>	AA23	
OUT1<16>	Z21	
OUT1<17>	Z23	
OUT1<18>	Y21	
OUT1<19>	Y23	
OUT1<20>	W21	
OUT1<21>	W23	
OUT1<22>	V21	
OUT1<23>	V23	
OUT1<24>	U21	
OUT1<25>	U23	
OUT1<26>	T21	
OUT1<27>	T23	
OUT1<28>	R21	
OUT1<29>	R23	
OUT1<30>	P21	
OUT1<31>	P23	
OUT1<32>	L21	
OUT1<33>	L23	
OUT1<34>	K21	
OUT1<35>	K23	
OUT1<36>	J21	
OUT1<37>	J23	
OUT1<38>	H21	
OUT1<39>	H23	
OUT1<40>	G21	
OUT1<41>	G23	
OUT1<42>	F21	
OUT1<43>	F23	
OUT1<44>	E21	
OUT1<45>	E23	
OUT1<46>	D21	
OUT1<47>	D23	
OUT1<48>	C21	
OUT1<49>	C23	
OUT1<50>	B21	
OUT1<51>	B23	
OUT1<52>	A21	
OUT1<53>	A23	
OUT1<54>	C17	
OUT1<55>	D19	
OUT1<56>	B17	
OUT1<57>	C19	
OUT1<58>	C15	
OUT1<59>	B19	
OUT1<60>	B15	
OUT1<61>	A19	
OUT1<62>	A15	
OUT1<63>	A17	
VALEVENT_N	A11	I/O Digital Differential (50MHz)
VALEVENT_P	A12	
VDD	F9	Power Supply - VDD
VDD	F10	
VDD	F11	
VDD	G9	
VDD	G10	
VDD	G11	

VDD	H6		VDD	T7	
VDD	H7		VDD	U6	
VDD	J6		VDD	U7	
VDD	J7		VDD	V9	
VDD	K6		VDD	V10	
VDD	K7		VDD	V11	
VDD	R6		VDD	W9	
VDD	R7		VDD	W10	
VDD	T6		VDD	W11	

Table 5 – PSIROC ASIC pin list

PSIROC ASIC floorplan & packaging

Naked die size is 4.72 mm x 11.12 mm including scribe line giving a die area of 52.5 mm^2. The ASIC has 515 bump pads which bonded to BGA substrate.

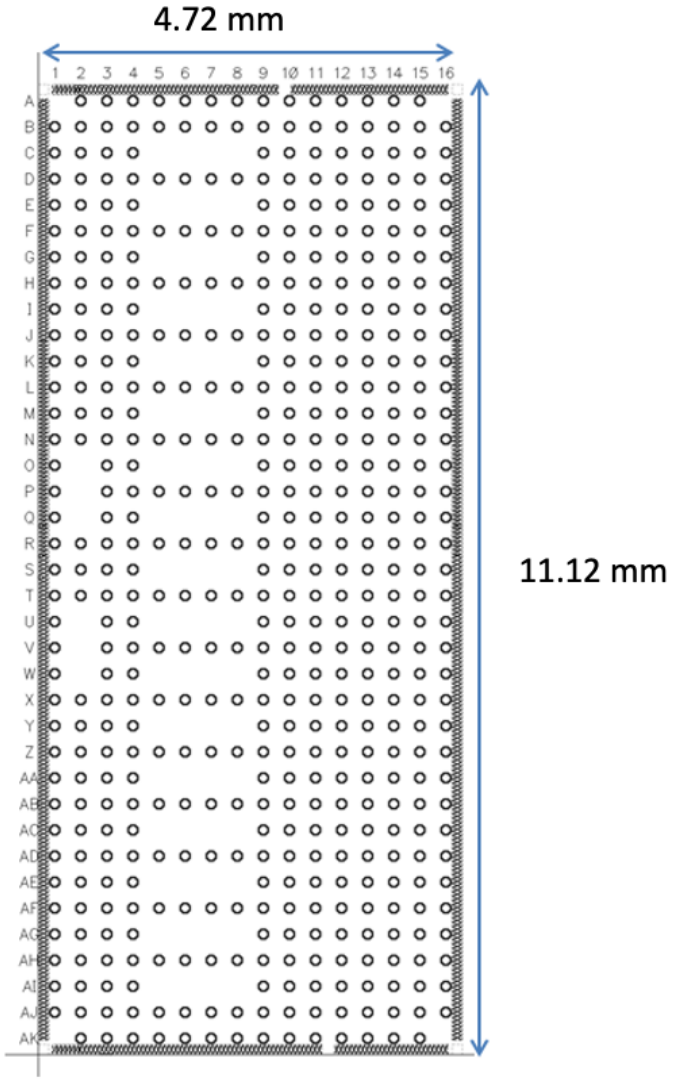


Figure 8 – Padring and form factor

Power supply

The core of the ASIC is powered by 1.2 V and power supplies are separated in several zone to reduce EMC influence from various sections of the ASIC. It is recommended to at least separate the digital power supply from the analog power supply and to use decoupling capacitors for stabilizing & filtering of the power supply.

Pin Name	Pin Type	Description	Connected to
VDD_PA	Power Supply	Input stage power supply	2.5V or 1.2V
VDD	Power Supply	Analog power supply	1.2V
DVDD	Power Supply	Digital power supply	1.2V
GND	Ground	Ground	0

Input connection

The input pins are solely reserved for the detector inputs. Short distance of traces for routing the input signal is highly recommended.

Pin Name	Ball Map	Description	Connected to
in<0:63>	Various location (refer to Table 5)	Connection to detector	

Biasing & debugging connections

Biasing pins are mostly optional I/Os which are available for debugging and modifying analog section biasing if required. It could be left open or connected to decoupling capacitors in most cases. However, if a biasing modification is required, it is also possible to connect the pin to resistor-based voltage divider (refer Figure 9). The expected DC value of each pin can be found in Table 2. Additionally, the proposed connection for debugging and analog readout pins (OUT_AMUXLG, OUT_AMUXLG, OUT_APROBE & IN_CTEST) is shown in Figure 10 and Figure 11.

Pin Name	Ball Map	Description	Connected to
OUT_AMUXLG	N1	Multiplexed Low Gain Shaper output	ADC/ Analog buffer /Oscilloscope
OUT_AMUXHG	M1	Multiplexed High Gain Shaper output	ADC/ Analog buffer /Oscilloscope
OUT_APROBE	M3	Analog Probe monitoring output	Analog buffer & oscilloscope
IB_PA	AB8	Input stage pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
OUT1<0:63>	Various location	High Gain/Low Gain output	ADC/ Analog buffer /Oscilloscope
OUT2<0:63>	Various location	High Gain/Low Gain output	ADC/ Analog buffer /Oscilloscope
THRESHOLD	L3	Trigger threshold	Decoupling capacitor
THRESHOLDTOT	K3	ToT Trigger threshold	Decoupling capacitor
THRESHOLDQ	J3	Charge Trigger threshold	Decoupling capacitor

VBG	P3	Bandgap output	Decoupling capacitor
VBIAS_1V	R3	1V low impedance bias output	Decoupling capacitor
VREF_FSH	V3	Fast shaper reference voltage	Decoupling capacitor and/or voltage divider
VREF_PA	U3	Pre-amp reference voltage	Decoupling capacitor and/or voltage divider
VCN_ABUFFER	F3	Analog buffer amp cascode N voltage	Decoupling capacitor and/or voltage divider
VCN_OUTING	D3	Output buffer amp cascode N voltage	Decoupling capacitor and/or voltage divider
VCN_PDETECTOR	Z3	Peak detector cascode N voltage	Decoupling capacitor and/or voltage divider
VCP_ABUFFER	E3	Analog buffer amp cascode P voltage	Decoupling capacitor and/or voltage divider
VCP_OUTING	C3	Output buffer amp cascode P voltage	Decoupling capacitor and/or voltage divider
VCP_PDETECTOR	Y3	Peak detector cascode P voltage	Decoupling capacitor and/or voltage divider
VREF_INV	N3	Voltage reference for the preamplifier inverter, only used for positive input signal polarities	Decoupling capacitor
VREF_DELAY	AA3	Delay cell reference voltage	Decoupling capacitor and/or voltage divider
VCASC_PA	T3	Preamplifier cascode reference	Decoupling capacitor and/or voltage divider
VREF_SH	W3	Shaper reference voltage	Decoupling capacitor and/or voltage divider
VREF_THDAC	H3	Time Trigger threshold DAC reference voltage	Decoupling capacitor and/or voltage divider
VREF_THDACQ	G3	Charge Trigger threshold DAC reference voltage	Decoupling capacitor and/or voltage divider
VTH_DELAY	AB7	Delay cell threshold output	Decoupling capacitor
IN_CTEST	B7	Charge injection input	Waveform generator or pulser

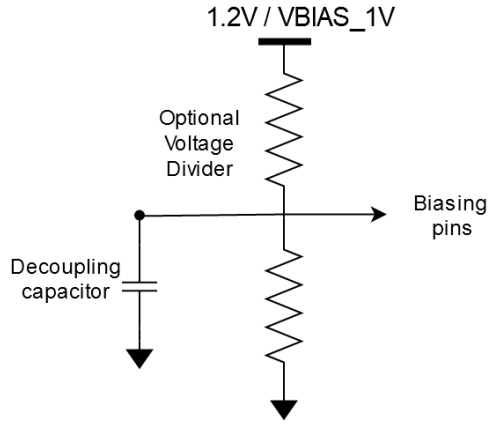


Figure 9 – Proposed connection for biasing points.

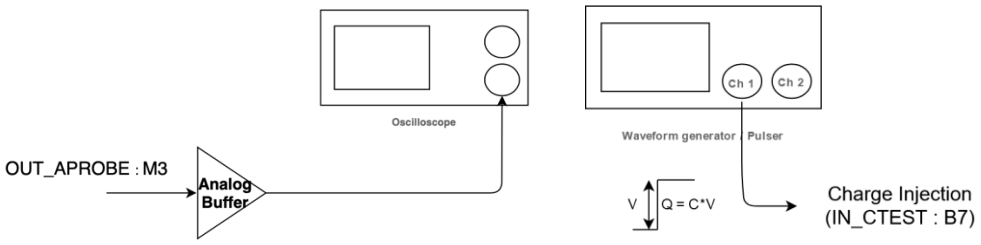


Figure 10 – Proposed connection for OUT_APROBE (Left figure) and IN_CTEST (Right figure)

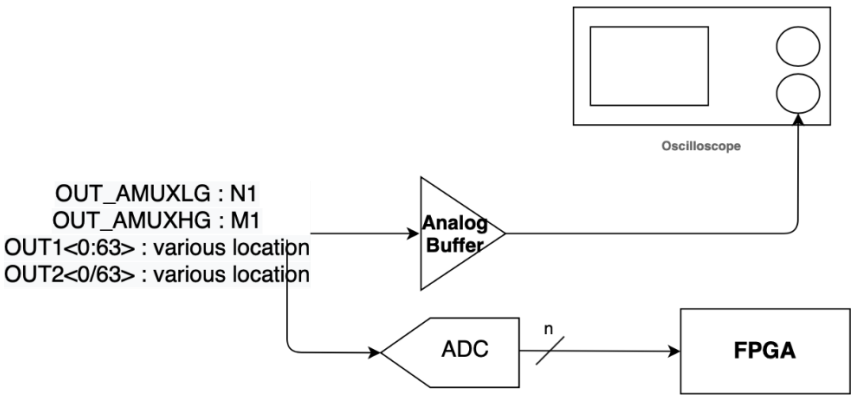


Figure 11 – Proposed connection for OUT_AMUXLG, OUT_AMUXHG, OU1<0:63> and OUT2<0:63>

Digital connections

The digital I/Os are divided into 3 types: single-ended, bidirectional and differential (CLPS[2]). The proposed connection for bidirectional and differential pins are shown in Figure 12. The pins are active high unless it is stated to be active low. Additionally, suggestions of connecting various digital I/Os are also shown in Figure 13 and Figure 14.

Pin Name	Ball Map	Description	Connected to
CHIP_ID<0:3>	M23, N24, N23, N22	Chip ID for I2C (PSIROC CHIP_ID<0:3> = "0001"): Single Ended	FPGA
CLK_SM_I2C	A10	Clock for I2C slave core: Single Ended	FPGA
ERRORN_SC	M24	Slow Control reset error: Single Ended, active low	FPGA
CK_READ	A13	Clock for read register: Single Ended	FPGA
RSTN_READ	A14	Low level reset for read register: Single Ended, active low	FPGA
RESET_N	A8	Low level reset for digital part (delay box + peak detector): Single Ended, active low	FPGA
RSTN_PROBE	B8	Low level reset for probe registers (analog debugging & signal monitoring): Single Ended, active low.	FPGA
RSTN_I2C	B9	Low level reset for I2C slave core: Single Ended, active low.	FPGA
SCL	B10	SCL line for I2C: Bidir	FGPA with 47k Ohm pull up resistor to 1.2V
SCA	A9	SDA line for I2C: Bidir	FGPA with 47k Ohm pull up resistor to 1.2V
NOR_T1OC	AC12	NOR gate Time trigger output (Low threshold): Single Ended, open collector	FPGA/Oscilloscope with pull-up resistor
NOR_T2OC	AC13	NOR gate Time trigger output (High threshold): Single Ended, open collector	FPGA/Oscilloscope with pull-up resistor
NOR_TQOC	AC14	NOR gate Charge trigger output: Single Ended, open collector	FPGA/Oscilloscope with pull-up resistor
OUT_DPROBE	AC10	Multiplexed digital probe(monitoring) output: Single Ended	FPGA/Oscilloscope
HOLDEXT	AC9	External hold signal for peak detector: Single Ended	FPGA/Waveform generator
TRIGEXT	AC11	External trigger: Single Ended	FPGA/Waveform generator
RSTN_SC	B11	Low level reset for Slow Control registers: Single Ended, active low	FPGA
VALEVENT_N/P	A11/12	Differential fast discriminator masking inputs: CLPS	FPGA

[2] CLPS stands for CERN Low Power Signaling. It is not a fairly common digital I/Os standard. The common voltage is set at 0.6V with signal swing of 300mV.

OUT1<0:63>	Various location	Single ended/Differential (refer to readout setting)	FPGA
OUT2<0:63>	Various location	Single ended/Differential (refer to readout setting)	FPGA

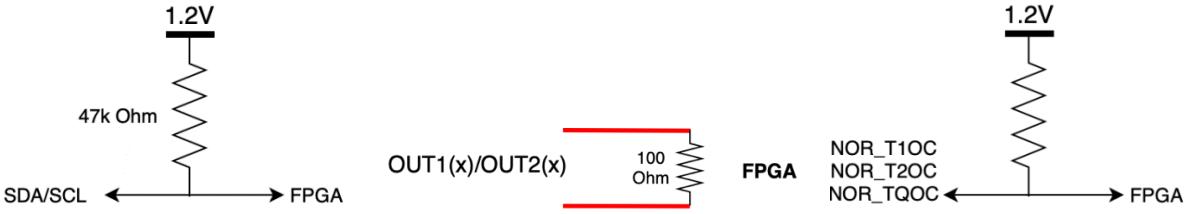


Figure 12 – Left: Proposed connection for SDA/SCL. Middle: Differential outputs connection. Right: Open Collector output

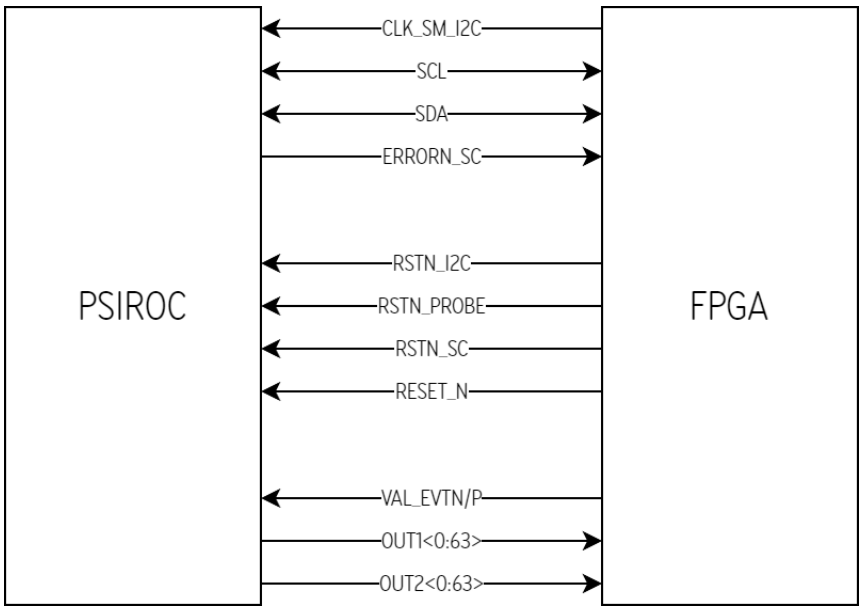


Figure 13 – Trigger outputs, Resets and I2C for Slow Control connections suggestion

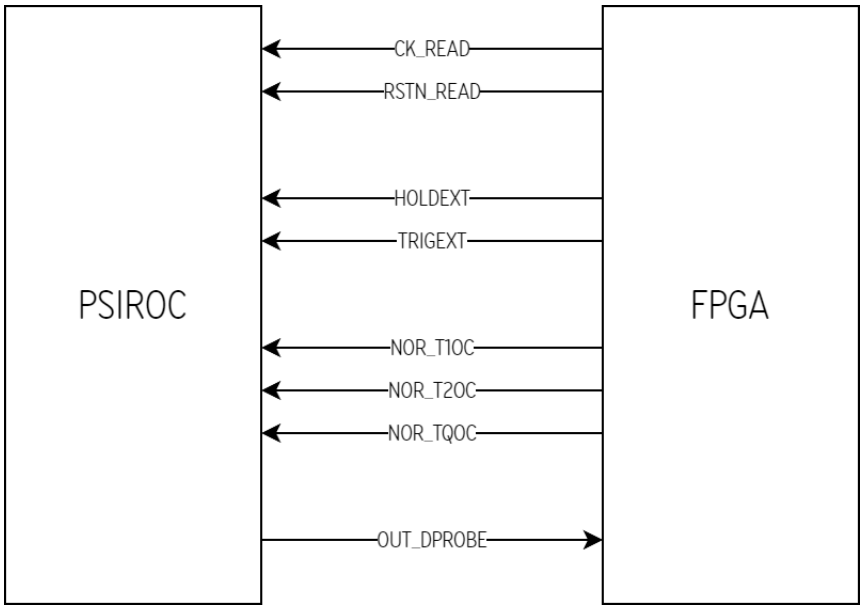


Figure 14 – Read Register, external control inputs, NOR trigger outputs and Digital monitor connections suggestion

PSIROC analog operation

The analog part of PSIROC is composed of a charge pre-amplifier followed by a fast shaper for input signal discrimination & triggering and two slow shapers (High Gain and Low Gain) for energy measurement. Schematic diagram of the analog section is shown in Figure 15.

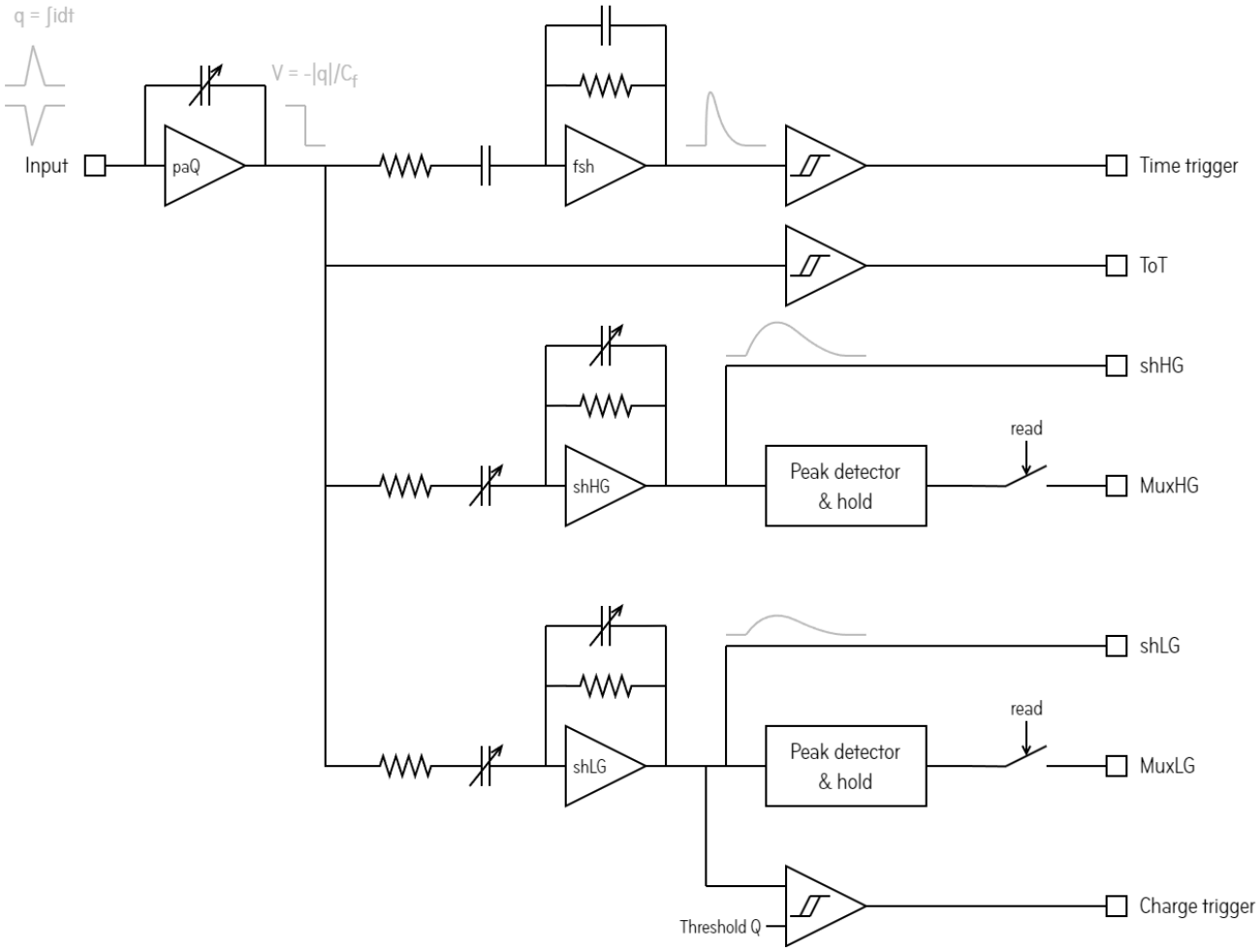


Figure 15 – PSIROC Analog Section

Charge pre-amplifier

This ASIC accepts both input polarities. The output of the pre-amplifier is a voltage step with a slow return to baseline. The pre-amplifier has a variable gain adjustment accessible through Slow Control bits:

- *paGain* (Address: 0-63; Subadd: 0; Bits: 5-0). Cf: 125 fF – 8 pF.

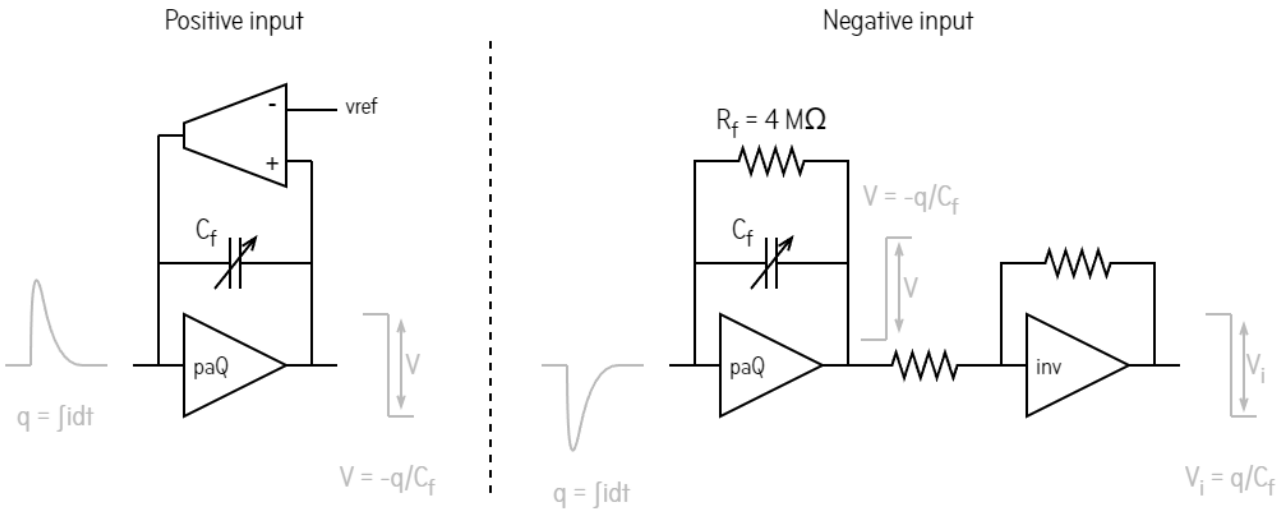


Figure 16 – Pre-amplifier block diagram for positive (left) and negative (right) input signals.

The Slow Control bits will change the value of feedback capacitor Cf of the pre-amplifier. Depending on the polarity of the input signal the corresponding slow control bit must be set:

- *polarity* (Address: 0-63; Subadd: 0; Bits: 6). 0: negative input – 1: positive input.

The feedback is done either with a feedback OTA or a 4 MOhm resistor. The OTA is mainly used to bias the output higher than the input. The input is biased at V_{th} of the input Nmos (~500 mV) and in the case of positive input signal, the output is negative hence having a higher output DC biasing (> 2 V if VDD_PA = 2.5 V) gives more dynamic range. When used for negative input signal the pre-amplifier output is inverted and series noise is added to the signal because of the inverter resistors. This is more noticeable for larger C_f values (lower gains) because for large gains the input Nmos thermal noise is the major noise contributor (see Figure 17).

Compensation must also be set for pre-amplifier stability. The *paComp* value can be kept the same as the *paGain*:

- *paComp* (Address: 0-63; Subadd: 1; Bits: 5-0). Ccomp: 0 F – 7.875 pF.

Discriminators

The first discriminator is preceded by a fast shaper to significantly increase Signal to Noise Ratio. Its threshold can be adjusted by the *DACT* slow control bits.

- (*DACT*, Address: 65; Subadd: 2; Bits: 1-0 & Subadd: 1; Bits: 7-0).

The second discriminator is plugged directly at paQ output and can be used for ToT measurements. Because the paQ discharge is very slow the ToT can be as large as few hundreds of microseconds for signal charges of a few tens of pico-coulombs. Its threshold is adjusted via *DACTOT*:

- (*DACTOT*, Address: 65; Subadd: 3; Bits: 3-0 & Subadd: 2; Bits: 7-2).

Energy measurement

This ASIC also embeds two shapers (High Gain & Low Gain). Both of the shapers have a variable shaping time. The shaping time for both shapers can be adjusted using the Slow Control bits *tauHG* (Address: 0-63; Subadd: 3; Bits: 7-4) for the High Gain shaper and *tauLG* (Address: 0-63; Subadd: 3; Bits: 3-0) for the Low Gain shaper. The Slow Control bits adjusting the shaping time are:

- *tauHG* (Address: 0-63; Subadd: 3; Bits: 7-4). Shaping time span: 20 ns ~300 ns. Step = 20 ns
- *tauLG* (Address: 0-63; Subadd: 3; Bits: 3-0). Shaping time span: 20 ns ~300 ns. Step = 20 ns

If the slow control bits *slowShapingLG* (Address: 0-63; subadd: 7; bit: 7) or *slowShapingHG* (Address: 0-63; subadd: 7; bit: 6) are set to '1', the adjustment becomes 200 ns ~ 3 µs with a step of 200 ns.

Switching this bit actually multiplies the shaper resistors by 10 so it will add a copious amount of series noise (from 14.7 kΩ → 15.6 nV/√Hz to 147 kΩ → 49.3 nV/√Hz). Albeit it is second stage noise it has a very noticeable effect as shown on Figure 17. Thus, unless long integration time are needed and ENC is acceptable it is better to stick with LSB = 20 ns.

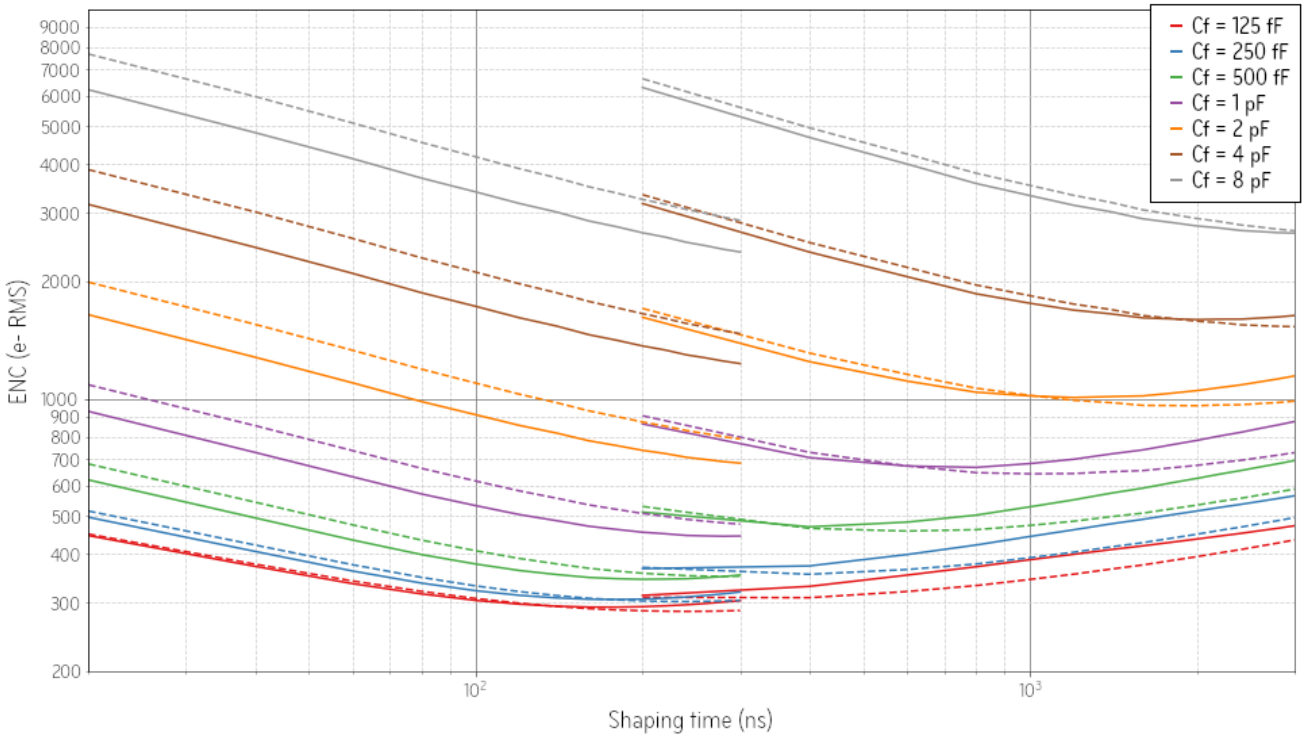


Figure 17 – ENC as a function of shaping time with Cd = 20 pF (simulation results). Solid line: positive input; dotted line: negative input. The discontinuity is due to the shaping time LSB toggling from 20 ns to 200 ns.

Each of the shaper output will be sent to a peak detector cell which will be connected to an analog multiplexer for external amplitude (charge) measurements. Additionally, the Low Gain shaper signal can be used to generate a "charge" Trigger (TQ). The threshold can be set through the following Slow Control bits:

- *DACQ* (Address: 65; Subadd: 4; Bits: 5-0 & Subadd: 3; Bits: 7-4). Voltage span: 75 mV ~ 1,2 V. Step = 1 mV

Peak detectors

Peak detectors are used to sample the amplitude of the shaper signal by conserving the peak analog value of this signal. The operation of the peak detector is illustrated in the Figure 19. Shaper output will be fed into the peak detector cell and Time or Charge trigger (localized or global) will be used as an acquisition trigger to start peak detection. Refer to Figure 18 for acquisition trigger logic. Local trigger denotes the trigger generated within the hit channel and global ASIC trigger denotes the OR output of any trigger in the ASIC. This selection can be done with the following Slow Control bits:

- *selTrig<1:0>* (Address: 65; Subadd: 12; Bits: 1-0). The following triggers can be selected:
  - "00" Global ASIC trigger (Refer to *selTrig<3:2>* Slow Control bit) (default);
  - "01" Local Trigger T;
  - "10" Local Trigger ToT;
  - "11" Local Charge Trigger.

When the "*selTrig<1:0>*" is set to "00", the acquisition trigger enabling the peak detectors is ASIC wide. Therefore, there are several signals which can be used for this purpose and can be set through the following Slow Control bits:

- *selTrig<3:2>* (Address: 65; Subadd: 12; Bits: 3-2). The following triggers can be selected:
  - "00" Ground (meant to be used with TRIGEXT (AC11));
  - "01" Global Trigger T (default);
  - "10" Global Trigger ToT;
  - "11" Global Charge Trigger.

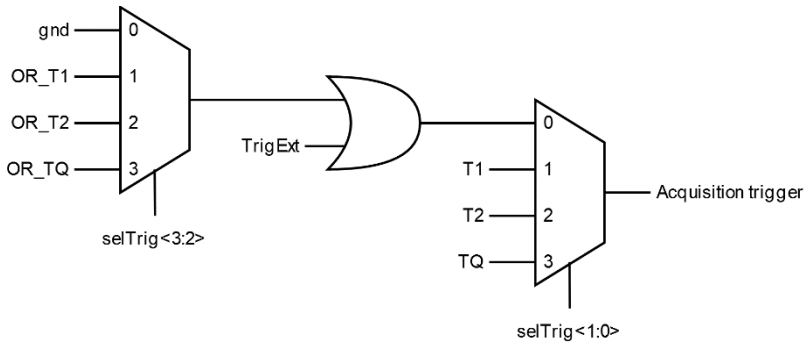


Figure 18 – Acquisition trigger logic per channel.

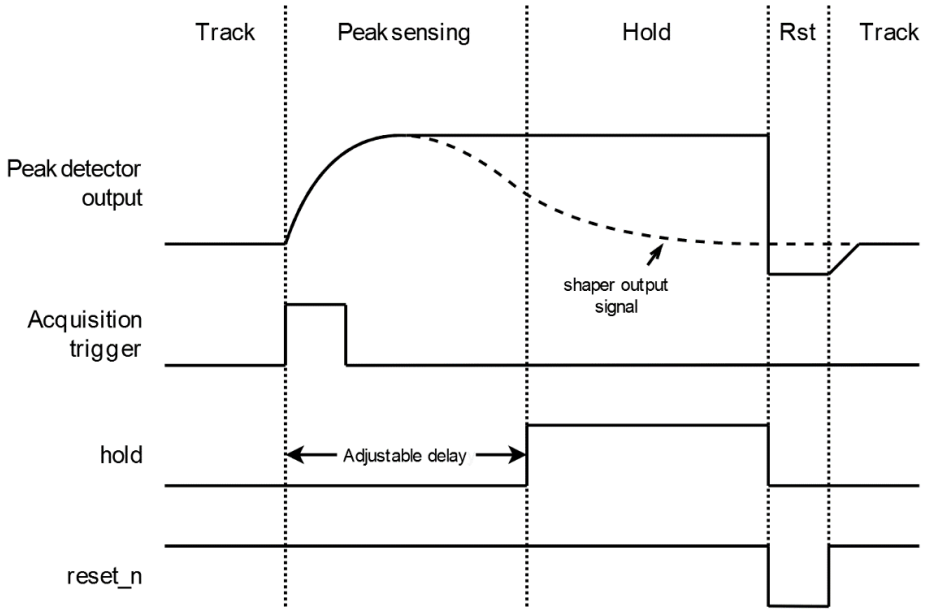


Figure 19 – Illustration of peak detection in PSIROC.

Additionally, a delay cell (at ASIC level) is used to generate a "hold" signal that opens the input of the peak detector, making it bling to any subsequent event, before sending it to the analog multiplexer output. This delay cell will take as input the acquisition trigger chosen by user (Slow Control bits: *selTrig* (Address: 65; Subadd: 12; Bits: 3-0)). Then a delay can be applied to this trigger using the following Slow Control bits:

- *Delay* (Address: 65; Subadd: 8; Bits: 7-0). Delay span: 2 ns~2.6 µs. Step size depends on *slopeTrim*;
- *SlopeTrim* (Address: 65; Subadd: 9; bits: 7-4). @0x0 max delay = 60 ns; @0xF max delay = 2.6 µs.

The hold signal can be fed externally by setting the SC bit *selHoldExt* to '1' (address: 65; subadd: 12; Bit: 4) and using the pin HOLDEXT (AC9, active high).

PSIROC trigger and backend operation

Outing selection

There are 128 programmable output pins on PSIROC (2 per channel) and 5 hard-wired. The 5 hard-wired outputs are the 3 logic NOR of the triggers (open collector output), NOR_TOC (AC12, for T1), NOR_TOTOC (AC13, for T2) and NOR_TQOC (AC14, for TQ) and two multiplexed analog outputs OUT_AMUXHG (M1, for High Gain charge measurement), and OUT_AMUXLG (N1, for Low Gain charge measurement). Those two analog outputs are used to read out the analog values stored in the "peak detector and hold" cells.

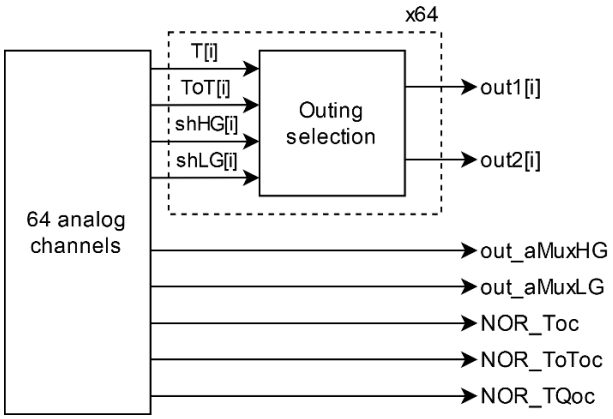


Figure 20 – PSIROC output schematic.

The following Slow Control bits are used to select the per channel output to be sent to OUT1<0:63> and OUT2<0:63> ballout:

- *lvdsOut[1:0]* (Address: 66; Subadd: 0; Bits: 5-4)
- *outPad1[1:0]* (Address: 66; Subadd: 0; Bits: 1-0)
- *outPad2[1:0]* (Address: 66; Subadd: 0; Bits: 3-2)

lvdsOut has the priority over the *outPad1* and *outPad2* meaning it must be set to "00" to output non-differential signals. It should be noted that the differential outputs are only available for Time Trigger outputs (T1 & T2).
The following values are available for *lvdsOut* Slow Control bits:

- 00 = Differential output disabled, refer to *outPad1* and *outPad2* Slow Control settings;
- 01 = Differential output for Trigger T;
- 10 = Differential output for Trigger ToT;
- 11 = disable all outputs.

The following settings are available for *outPad1* and *outPad2* Slow Control bits:

- 00 = single-ended output for Trigger T;
- 01 = single-ended output for Trigger ToT;
- 10 = High gain slow shaper output;
- 11 = Low gain slow shaper output.

Some examples:

lvdsOut[1:0]	*outPad1[1:0]*	*outPad2[1:0]*	OUT1[i]	OUT2[i]
00	00	01	T	ToT
01	xx	xx	CLPS T_p	CLPS T_n
00	00	10	T1	HG slow shaper

Outputs are programmable channel per channel. For instance, users could choose to output the triggers T1/T2 on OUT1[m]/OUT2[m] and the slow shaper high gain/low gain outputs on OUT1[n]/OUT2[n], etc.

Extended output

PSIROC can be toggled to use only 32 channels but with 4 direct outputs per channel. When the *extendedOutput* bit is set to '1' (Address: 66; Subadd: 64; bit: 7), trigger signals of even channels will be sent to the following odd channel. This means that odd channels become unable to output anything and can be completely powered off. This operation allows to either output both single ended triggers T and ToT along both shaper outputs HG and LG or have both T1 and T2 CLPS trigger outputs per channel.
To have e.g., both T1 and T2 CLPS trigger outputs one would need to set *extendedOutput* to '1', *lvdsOut* to '01' on even channels and *lvdsOut* to '10' on odd channels. Hence on out1/2[0] would be the CLPS T of channel 0 and on out1/2[1] the CLPS ToT of channel 0. Channel 1 would be unable to output anything. Channel 2 trigger T would be on out1/2[2] and ToT on out1/2[3] etc.
Note that if not powered off, the discriminators of odd channels can still participate to NOR triggers. This would most likely be unwanted behavior so setting off the analogue blocks of those unused channels would be needed.

Read register

Operating the analog multiplexers (OUT_AMUXLG and OUT_AMUXHG) for the shapers can be done by accessing the read registers through CK_READ (A13) and RSTN_READ (A14) pins. Operating these registers requires only a low-level reset (RSTN_READ) and a certain number of clock cycles (CK_READ) to be sent to the ASIC. The timing diagram and the expected outputs on OUT_AMUXLG and OUT_AMUXHG pads are shown in Figure 21. This operation should be performed when the peak detector is in hold mode. At the end of the reading procedure the RESET_N pin (A8) should be asserted during 20 ns to reset the peak detectors and delay cell.

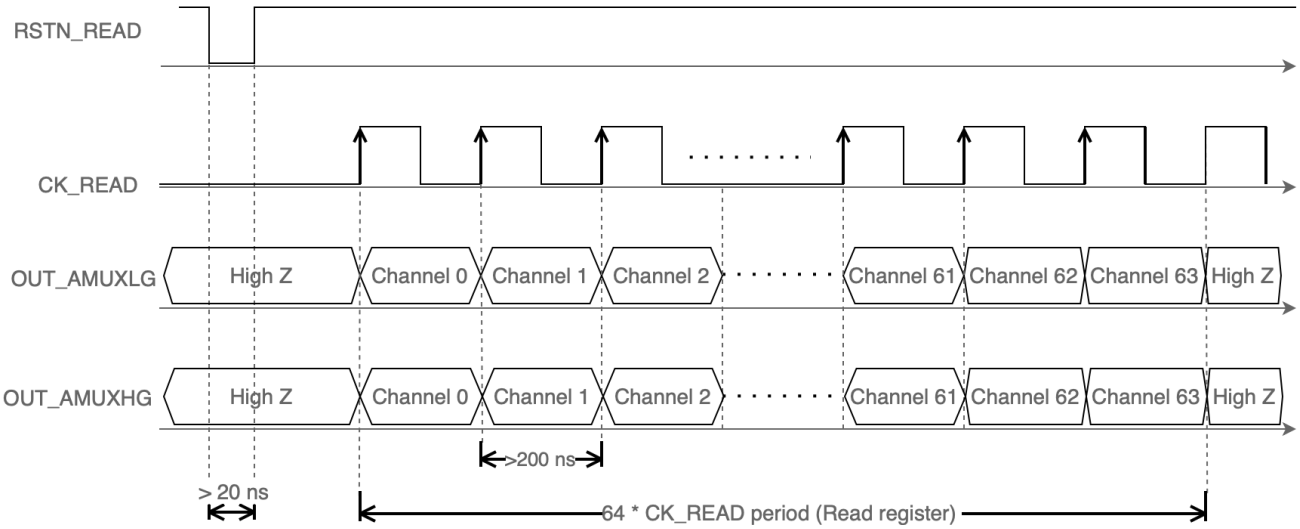


Figure 21 – Analog multiplexer for High Gain and Low Gain shapers readout timing diagram

The RSTN_READ pin can be asserted at the beginning or the end of the data acquisition. The read register just has to be reset between two acquisitions to ensure its correct positioning (see Figure 22).

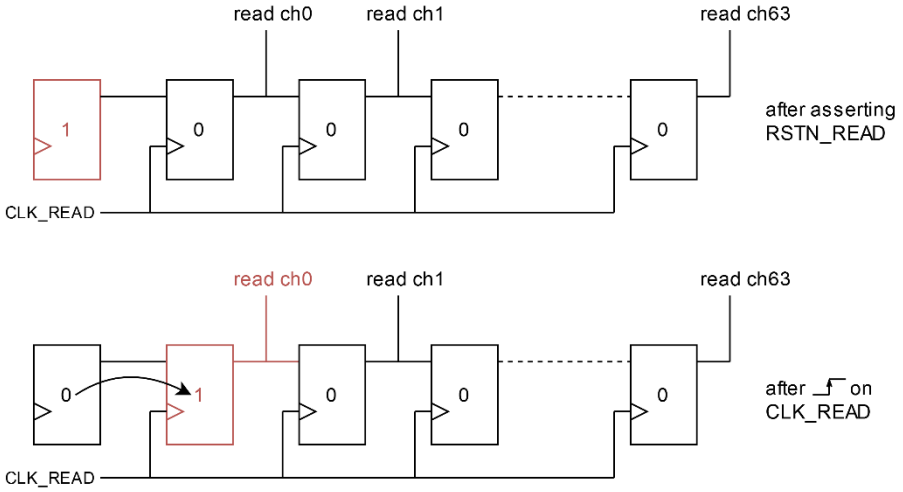


Figure 22 – read register operation.

Data acquisition examples

Example 1: default configuration

On example 1 is considered that the default SC settings are kept for acquisition. The acquisition trigger is the logic OR of trigger T with *selTrig* = "0100". The "hold" signal is generated internally by the delay box and after its assertion the DAQ can be started by the user. Please note that the hold signal can't be monitored. The output NOR_TOC has to be monitored to know when an acquisition is started by the ASIC. The user must wait for a selected time depending on the chosen delay before starting to assert the CLK_READ pin. Figure 23 shows an example with an input signal on IN<2>. An external ADC must be used to digitize the analog data on OUT_AMUXHG and OUT_AMUXLG. If the user wants to speed up the DAQ process the CLK_READ can be used to fast forward the read register up to the desired channel (without the need to wait 200 ns per channel) and the ADC will be used to digitize only the channel hit.

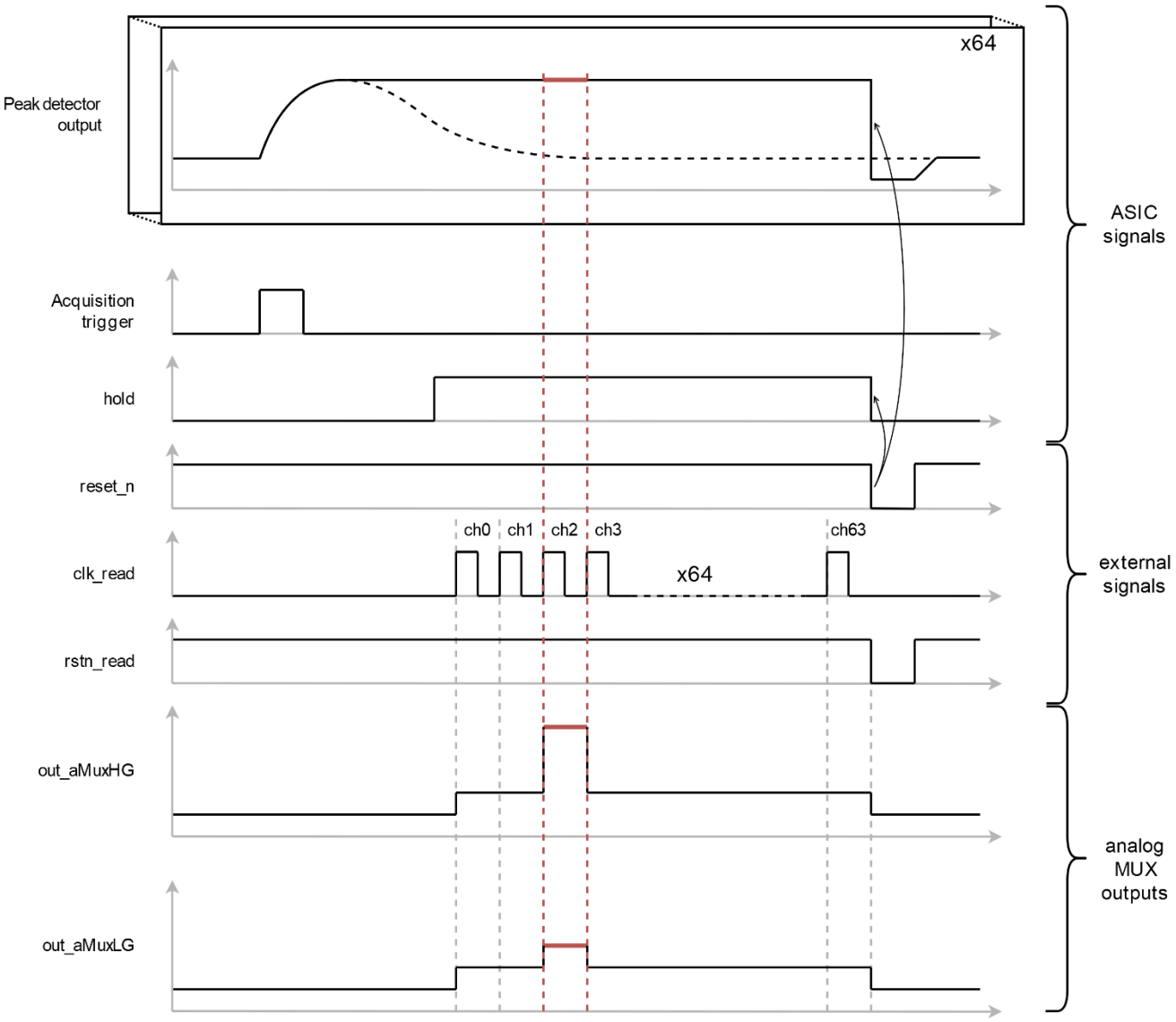


Figure 23 – Example 1 DAQ timing diagram.

Example 2: Charge measurement with custom topological trigger

On example 2 it is assumed that the user wants to trigger an acquisition when 2 or more channels are hit under a 1 ns period. An FPGA is used to implement the trigger logic so when the channels 1 and 2 are hit the pin TRIGEXT (AC11) is asserted by the FPGA. The slow control parameter *selTrig* is set to "0000" to use the TRIGEXT pin as the acquisition trigger. The outing can be set to either output LVDS trigger T (*lvdsOut* = "01") or a single ended trigger T (lvdsOut = "00" and *outPad1* or *outPad2* = "00"). The external trigger starts the delay box and after a given time the user can start the read-out procedure similarly to example 1.

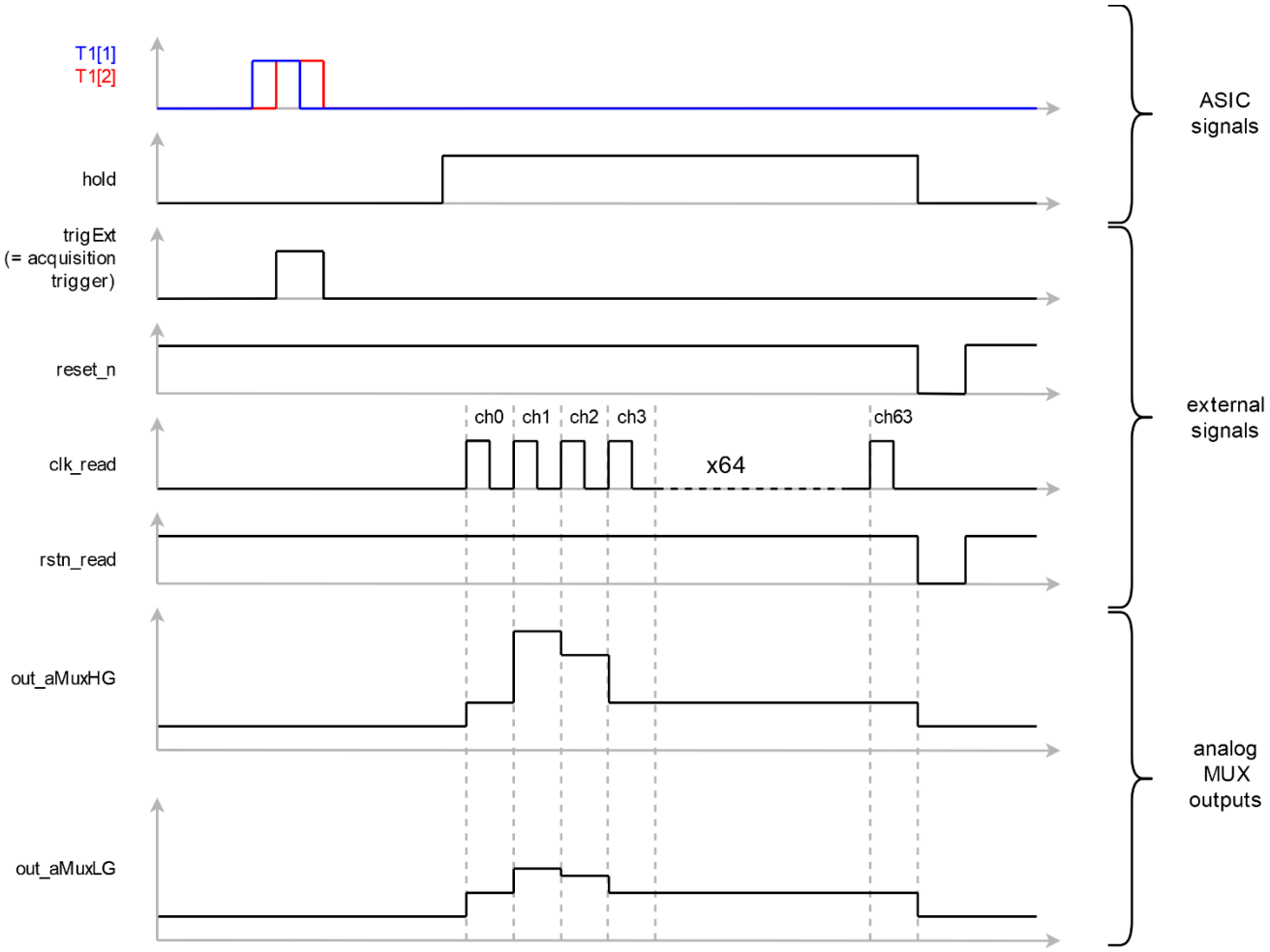


Figure 24 – Example 2 DAQ timing diagram.

Datasheet version history

Version	Date	Information
1.0	21/12/2023	Initial release
1.1	07/05/2024	I^2C parameters corrections