



Radiatoroc is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM). Radiatoroc allows triggering down to 1/3 p.e. and provides dual-gain energy measurement with excellent Signal-to-noise ratio on the high gain (SNR over 10 for single p.e.) and large dynamic range on the low gain.

Moreover, Radiatoroc can output the 64-channel triggers with jitter as low as 55 ps FWHM on a single p.e. (160 fC, $C_{inj} = 100\text{pF}$). Photo-counting has been measured to be over 200 MHz. Time Over Threshold (TOT) can be used and has been measured to be able to handle the full input swing.

An adjustment of the SiPM high-voltage is possible using a channel-by-channel 8-bit DAC connected to the ASIC inputs to homogenize SiPM gains.

Timing resolution better than 55 ps FWHM is possible along with 1% linearity energy measurement up to 2000 p.e. Outputs can be selected via I2C channel wise with 2 direct outputs per channel and the possibility to output single-ended/differential triggers or analog signals.



| | |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Detector Read-Out | SiPM, SiPM array |
| Number of Channels | 64 |
| Signal Polarity | Positive |
| Sensitivity | Trigger on 1/3 of photo-electron |
| Timing Resolution | 55 ps FWHM on single photo-electron @ 10^6 SiPM gain |
| Photocounting | 200 Mhz |
| Dynamic Range | Up to 2000 photo-electrons @ 10^6 SiPM gain |
| Packaging & Dimension | BGA 20x20 mm ² |
| Power Consumption | 310 mW – Supply voltage: 1.2 V |
| Inputs | 64 analogue inputs with independent SiPM HV adjustments |
| Outputs | 2 direct outputs per channel, selectable channel-per-channel, either : <ul style="list-style-type: none"> • 1 LVDS triggers • 2 TTL triggers • 1 TTL triggers and 1 analog outputs • 2 analog outputs 2 multiplexed analogue outputs 3 NOR64 trigger outputs |
| Internal Programmable Features (I2C) | 64 HV adjustment for SiPM (64 x 8 bits), 3 trigger threshold tuning (10bits), channel-by-channel gain and shaping time adjustment ($\tau = 20\text{ ns to } 300\text{ ns}$), individual trigger masking and cell powering. |



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Maximum ratings

| | | | | | | |
|-----|----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------|-----|------|----|
| 001 | Operating Temperature | ASIC operating temperature | -40 | 25 | 120 | C |
| 002 | Power Supply | VDD_PA, VDD, DVDD | 1.08 | 1.2 | 1.32 | V |
| 003 | Ground | GND | 0 | 0 | 0 | V |
| 004 | Analog Inputs | in<0:63> | 0 | - | 1.5 | V |
| 005 | Digital Inputs (Single ended) | chip_id<0:3>, clk_sm_i2c, ck_read, rstn_read, rstn_probe, reset_n, resetn_i2c, rstn_sc, trig_ext, hold_ext | 0 | - | 1.5 | V |
| 006 | Digital Inputs (Differential -Common Model) | valevent_n/p | 520 | 580 | 640 | mV |
| 007 | Digital Inputs (Differential - Swing) | valevent_n/p | 300 | 410 | 410 | mV |
| 008 | Digital Outputs (Single Ended) | errorn_sc, scl, sda, NOR_T1oc, NOR_T2oc, NOR_TQ, out_dprobe, out1<0:63>(Single ended mode), out2<0:63> >(Single ended mode) | 1.08 | 1.2 | 1.32 | V |
| 009 | Digital Outputs (Differential -Common Model) | out1<0:63> (CLPS mode), out2<0:63> (CLPS mode) | 520 | 580 | 640 | mV |
| 010 | Digital Outputs (Differential - Swing) | out1<0:63> (CLPS mode), out2<0:63> (CLPS mode) | 300 | 410 | 410 | mV |

Table 1 - Maximum ratings



ASIC Architecture

The block diagram of the ASIC is shown in Figure 1. The design is mostly an analog ASIC. In total there are 64 analog channels for signal triggering and pulse shaping.

The analog part consists of an input DAC, a time trigger pre-amplifier with dual threshold trigger outputs and two shapers (Low gain & High Gain). Additionally, there is a charge trigger output taken directly from the Low Gain shaper output. Each of the shapers has a dedicated peak detector cell.

On the backend there are two analog multiplexers which are used to output the peak detectors. For the three triggers (Times and Charge) there are NOR gate outputs. Lastly, there are 64 differential outputs which can be configured to output each channel trigger, single-ended or differential, or the slow shaper outputs.

The digital part is essentially an I2C slave core IP used to handle the Slow Control¹ parameters to configure the ASIC.

¹ Slow Control stands for the register (TMR) storing the data for analog block parameters.

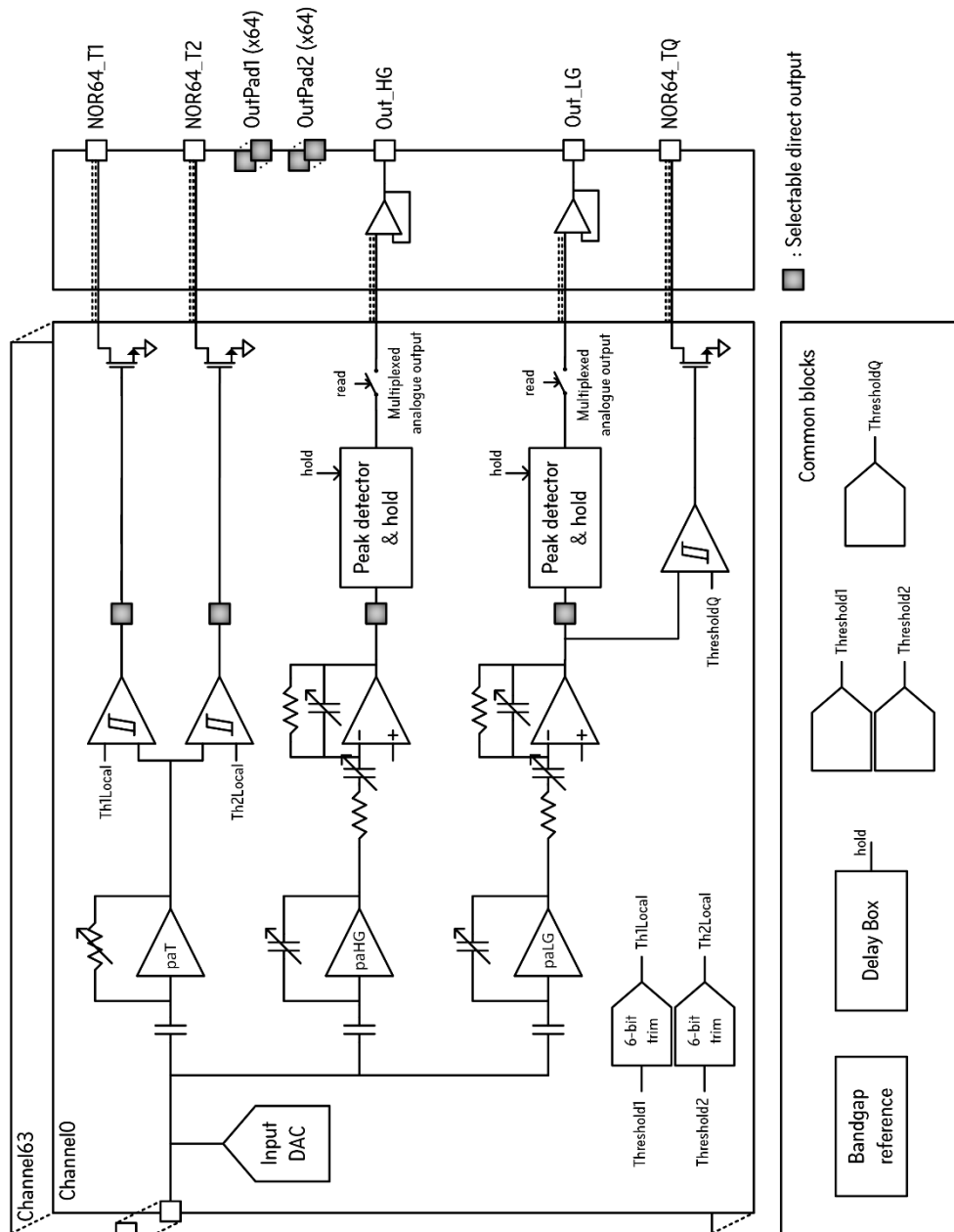


Figure 1 - ASiC block diagram

This ASiC design is optimized for SiPM signal with positive polarity, ranging from 1 photoelectrons (p.e) up to 2000 p.e. The design effort is mostly focused on the analog operation of this ASiC. Most of the critical parts of the ASiC have been simulated at least in typical, best-case and worst-case corners. In typical, power supply is nominal at 1.2V, components are at nominal speed and temperature is equivalent to 27°C. In best-case, the components are set at fast speed, temperature is minimum at -40°C and power supply is boosted by 10% at 1.32 V. Lastly in worst-case, the components are set at slow speed, temperature is maximum at 125°C and power supply is reduced by 10% at 1.08 V.

Power consumption & DC levels

Following DC levels are observed at the references and biasing point of RADIOROC with the default I²C configuration:



| <i>Signal name</i> | <i>Description</i> | <i>Sim @ 27°C</i> |
|----------------------|-----------------------------------------------------|-------------------|
| <i>IB_PAT</i> | Bias current for preamplifier trigger | 495 m |
| <i>THRESHOLD1</i> | Threshold voltage for trigger 1 | 536m |
| <i>THRESHOLD2</i> | Threshold voltage for trigger 2 | 536m |
| <i>THRESHOLD0</i> | Threshold voltage for charge trigger | 75m |
| <i>VBG</i> | Bandgap voltage | 621m |
| <i>VBIAS_1V</i> | 1V voltage regulator output | 995m |
| <i>VCASC_PAO</i> | Cascode voltage for charge measurement preamplifier | 279m |
| <i>VCASC_PAT</i> | Cascode voltage for trigger preamplifier | 846m |
| <i>VCP_ABUFFER</i> | Cascode voltage for analog mux & probe [PMOS] | 796m |
| <i>VCP_OUTING</i> | Cascode voltage for channel shaper output [PMOS] | 796m |
| <i>VCP_PDETECTOR</i> | Cascode voltage for channel peak detector [PMOS] | 796m |
| <i>VCN_ABUFFER</i> | Cascode voltage for analog mux & probe [NMOS] | 398m |
| <i>VCN_OUTING</i> | Cascode voltage for channel shaper output [NMOS] | 398m |
| <i>VCN_PDETECTOR</i> | Cascode voltage for channel peak detector [NMOS] | 398m |
| <i>VREF_1V</i> | 1V voltage reference from BG for regulator input | 1.0 |
| <i>VREF_DELAY</i> | Voltage reference for delay box (starting point) | 100m |
| <i>VREF_INDAC</i> | Voltage reference for input DAC | 597m |
| <i>VREF_SH</i> | Voltage reference for shaper | 100m |
| <i>VREF_THDAC</i> | Voltage reference for dual-threshold DAC | 536m |
| <i>VREF_THDAC0</i> | Voltage reference for charge threshold DAC | 75m |
| <i>VTH_DELAY</i> | Threshold voltage for delay box | 748m |

Table 2 - DC points

Power consumption of static power (amplifier biasing) has been simulated at 258 mA over 1.2V thus giving 310 mW for the full chip at room temperature and less than 5 mW per channel (x64). Around 40 % of the power consumption is sunk by the VDD_PA and 40 % is sunk by the VDD_PDETECTOR.

The power consumption is obtained without taking into account the probes and channel-by-channel analog buffers consumption. When the output pads are configured to output analog signals the consumption is increased by 1.5 mA per active analog buffer (depending on the SC parameters controlling the buffer biasing at address 66).

I²C configuration

This ASIC can be configured using I²C interface. The I²C slave core can be programmed using a custom I²C protocol that does not follow the IEEE standard. The I²C slave core has been designed with SEU mitigations in place.

Features of this IP are the following:

- Triplicated Design
- 2048 addresses for the channel numbers
- 32 addresses for the register numbers
- 15 Chip ID numbers

The I²C slave core must receive a clock through the clk_sm_i2c port. This clock must have a frequency exactly 20 times higher than the clock sent by the I²C master on the SCL line. These clocks must be synchronous. Figure 2 and Table 3 describe the I²C slave core structure in the ASIC and the registers content.

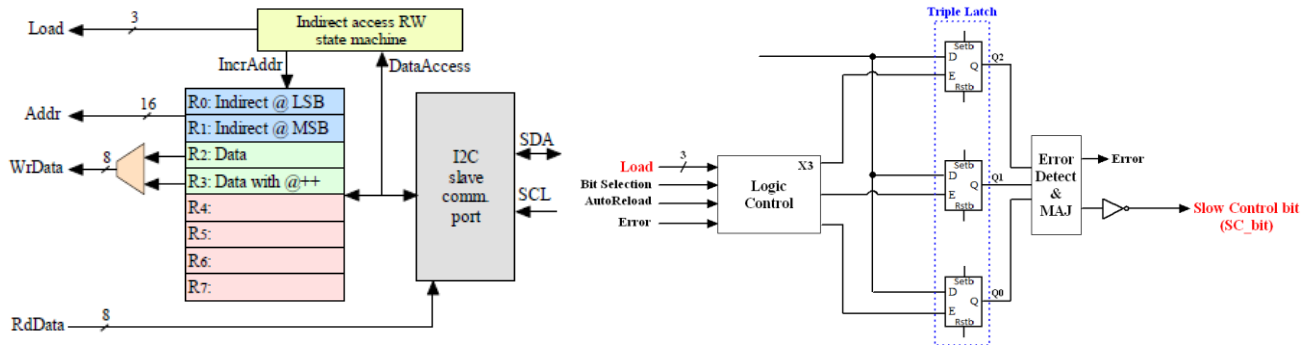


Figure 2 - Left: I2C slave core registers. Right: Slow Control bit cell design.

| I2C Address | Register |
|-------------|----------------------------------------|
| 0 | ASIC parameter address (LSB): Channel |
| 1 | ASIC parameter address (MSB): Register |
| 2 | Data Read/to Write |
| 3 | Data with auto-incremental Address |
| 4-5-6 | TBD |
| 7 | Status register (error, parity) |

Table 3 - I2C slave core register descriptions.

To address the Slow control parameters, the user can read or write each sub-address directly or it can use the auto increment feature that increments the sub-address based on the previous sub-address.

Figure 3 describes simple read and write I2C procedures. The full address to be sent is composed of the address and the sub-address of the slow control register, as described in Figure 4. The slow control registers associated addresses and sub-addresses can be found in Table 4.

Figure 5 shows a screenshot of an I²C write procedure to the slow control register with address 52 and sub-address 7.

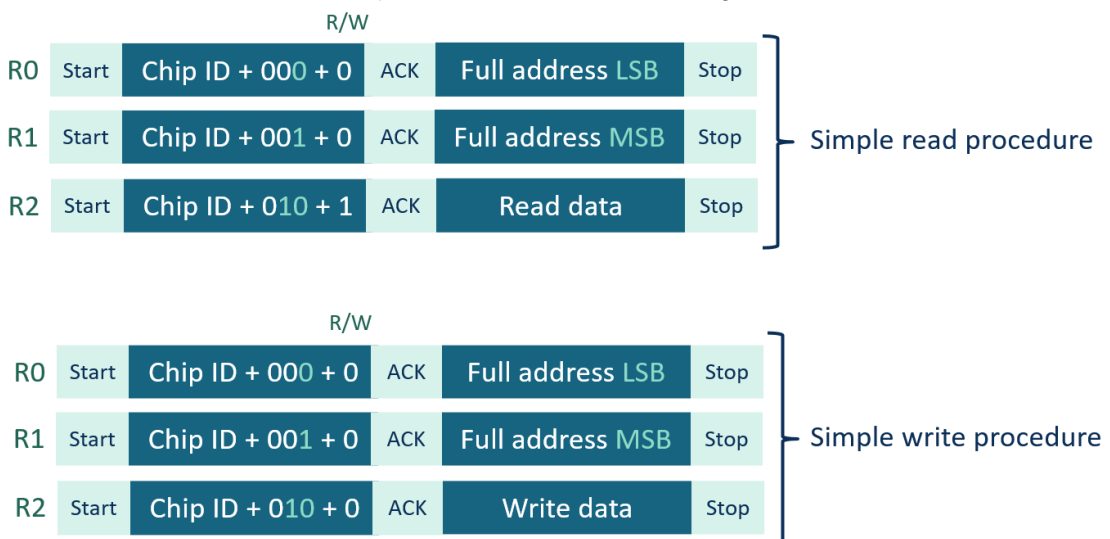


Figure 3 - Slow Control simple or direct parameter sub-addressing procedure.

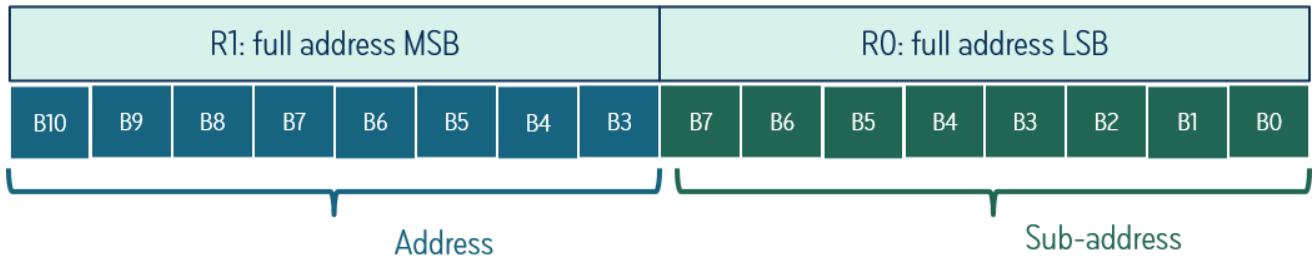


Figure 4 – Address and Sub-Address of the I²C register for setting the Slow Control of Radioroc

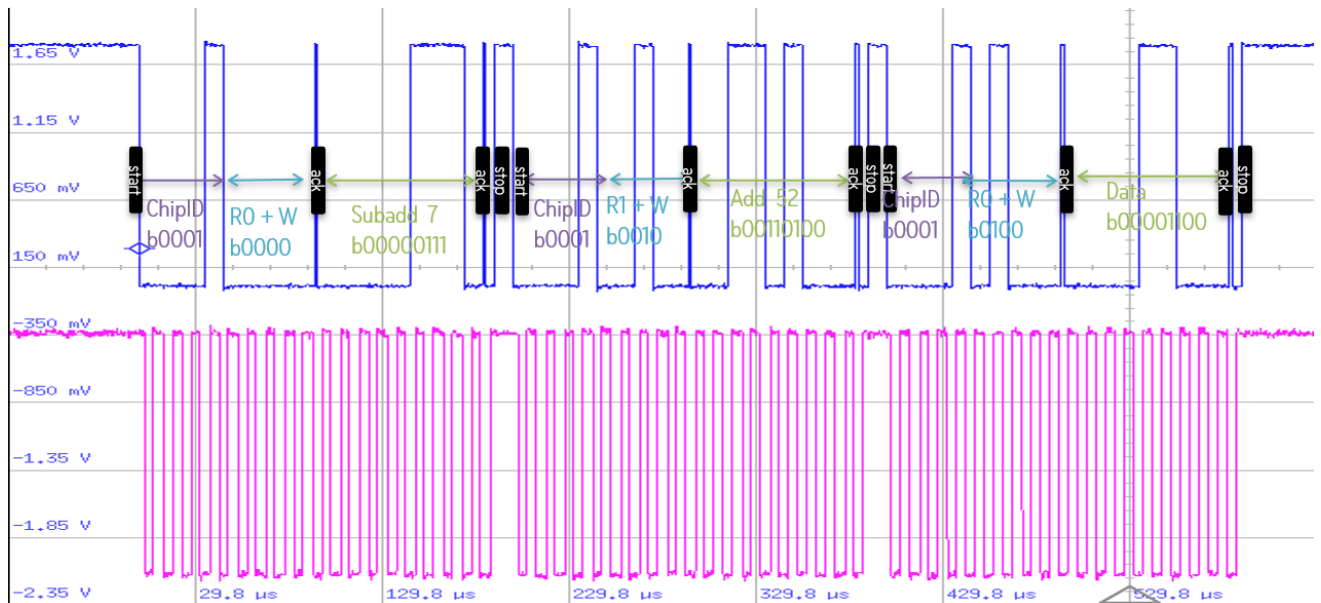


Figure 5 – SDA and SCL signals during an I2C write procedure of value 12 to address 52 sub-address 7

Slow Control parameters available for this ASIC are listed in Table 4. “NC” term denotes non used Slow Control bits. Data in “Address” and “Subadd” columns denote the sub-addresses R0 & R1 in the writing sequences respectively (Figure 4). Data payload in R2 (direct parameter addressing - Figure 3) will be based on data in “Parameters or Default Value” column. The address configuration has been arranged in the following way:

- 0-63: channelwise configuration (with the address corresponding to the channel number);
- 64: ASIC biasing;
- 65: common blocks;
- 66: outing;
- 67: event validation gating.



| Address | Subadd | Bit# | Default Value | Name | Description |
|---------|--------|-------|---------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0-63 | 0 | [7-0] | 10000000 | inDac[7:0] | Set input DAC value |
| | 1 | [7-6] | 10 | patComp[1:0], | Set preamplifier compensation capacitance. $C_{comp} = 50 \text{ fF} - 150 \text{ fF}$ |
| | | [5-0] | 100000 | patGain[5:0] | Set time preamplifier gain. $R_f = 2 \text{ k} - 126 \text{ k}$ |
| | 2 | [7-4] | 0100 | lgGain[3:0] | Set low gain charge preamplifier gain. (0,53 - 8) |
| | | [3-0] | 0100 | hgGain[3:0] | Set high gain charge preamplifier gain. (5,3 - 80) |
| | 3 | [7-4] | 0001 | tauHG[3:0] | Set high gain shaper peaking time. (20 ns - 300 ns) |
| | | [3-0] | 0001 | tauLG[3:0] | Set low gain shaper peaking time. (20 ns - 300 ns) |
| | 4 | [7-6] | 00 | NC | Not Connected |
| | | [5-0] | 000000 | calibDacT1[5:0] | Set channelwise adjustment threshold DAC 1 (low threshold). ($V_{threshold1} - (15 \text{ mV} - 0 \text{ mV})$) |
| | 5 | [7-6] | 00 | NC | Not Connected |
| | | [5-0] | 000000 | calibDacT2[5:0] | Set channelwise adjustment threshold DAC 2 (high threshold). ($V_{threshold2} - (15 \text{ mV} - 0 \text{ mV})$) |
| | 6 | 7 | 0 | DAC_select | Input DAC selection 0 – Sets 100 Ω impedance on input pin. 1 - HZ output, needs an external resistor + capacitor on the ASIC input. |
| | | 6 | 1 | EN_inDac | Enable bits for input DAC 0 – input DAC disabled 1 – input DAC enabled (default) |
| | | 5 | 1 | EN_paT | Enable time preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default) |
| | | 4 | 1 | EN_discr1 | Mask low threshold discriminator output 0 – discr1 is masked 1 – discr1 is operating (default) |
| | | 3 | 1 | EN_discr2 | Mask high threshold discriminator output 0 – discr2 is masked 1 – discr2 is operating (default) |
| | | 2 | 1 | EN_discrCharge | Mask charge threshold discriminator output 0 – discr is masked 1 – discr is operating (default) |
| | | 1 | 1 | EN_paLG | Enable low gain charge preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default) |
| | | 0 | 1 | EN_paHG | Enable high gain charge preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default) |
| | 7 | [7-5] | 000 | NC | Not Connected |



| | | | | | |
|--|----|-------|-----|------------|-------------------------------------------------------------------------------------------------------------------|
| | | 4 | 0 | EN_ctest | Enable charge injection (through 1.5 pF) 0 – disable charge injection (default) 1 – enable charge injection |
| | | 3 | 1 | EN_shLG | Enable low gain charge shaper 0 – shaper disabled 1 – shaper enabled (default) |
| | | 2 | 1 | EN_shHG | Enable high gain charge shaper 0 – shaper disabled 1 – shaper enabled (default) |
| | | 1 | 1 | EN_pdetLG | Enable low gain peak detector 0 – peak detector disabled 1 – peak detector enabled (default) |
| | | 0 | 1 | EN_pdet_HG | Enable high gain peak detector 0 – peak detector disabled 1 – peak detector enabled (default) |
| | 66 | [7-5] | 000 | NC | Not Connected |
| | | 4 | 0 | cmd_TQ | Probe switch command for charge trigger 0 – disabled (default) 1 – enabled |
| | | 3 | 0 | cmd_shhg | Probe switch command for the shaper high gain 0 – disabled (default) 1 – enabled |
| | | 2 | 0 | cmd_shlg | Probe switch command for the charge shaper low gain 0 – disabled (default) 1 – enabled |
| | | 1 | 0 | cmd_pahg | Probe switch command for the preamplifier high gain 0 – disabled (default) 1 – enabled |
| | | 0 | 0 | cmd_palg | Probe switch command for preamplifier low gain 0 – disabled (default) 1 – enabled |

| | | | | | |
|----|---|-------|------|-------------|-------------------------------------------------|
| 64 | 0 | [7-4] | 0100 | lbo_inDac0 | Set input DAC0 output stage bias |
| | | [3-0] | 0100 | lbi_inDac0 | Set input DAC0 input stage bias |
| | 1 | [7-4] | 0100 | lbo_inDac1 | Set input DAC1 output stage bias |
| | | [3-0] | 0100 | lbi_inDac1 | Set input DAC1 input stage bias |
| | 2 | [7-4] | 0100 | lb_calibDac | Set trigger threshold calibration bias |
| | | [3-0] | 0100 | lb_paT | Set pre-amp (Time Trigger) input stage bias |
| | 3 | [7-4] | 0100 | lb_paHG | Set pre-amp (High Gain Shaper) input stage bias |
| | | [3-0] | 0100 | lb_paLG | Set pre-amp (Low Gain Shaper) input stage bias |
| | 4 | [7-4] | 0100 | lbi_shHG | Set High Gain Shaper input stage bias |

| | | | | |
|----|-------|------|------------------|----------------------------------------------------------------------------|
| | [3-0] | 0100 | lbo_shHG | Set High Gain Shaper output stage bias |
| 5 | [7-4] | 0100 | lbi_shLG | Set Low Gain Shaper input stage bias |
| | [3-0] | 0100 | lbo_shLG | Set Low Gain Shaper output stage bias |
| 6 | [7-4] | 0100 | lbi_pdetector | Set peak detector input stage bias |
| | [3-0] | 0100 | lbi_pdbuffer | Set peak detector buffer stage bias |
| 7 | [7-4] | 0100 | lb_FCP_pdetector | Set peak detector differential P second stage bias |
| | [3-0] | 0100 | lb_FCN_pdetector | Set peak detector differential N second stage bias |
| 8 | [7-4] | 0100 | lb_FCP_pdbuffer | Set peak detector differential P buffer second stage bias |
| | [3-0] | 0100 | lb_FCNpdbuffer | Set peak detector differential N buffer second stage bias |
| 9 | [7-4] | 0100 | lbi_discr1 | Set discriminator (Low Th. Time Trigger) input stage bias |
| | [3-0] | 0100 | lbm1_discr1 | Set discriminator (Low Th. Time Trigger) middle stage 1 bias |
| 10 | [7-4] | 0100 | lbm2_discr1 | Set discriminator (Low Th. Time Trigger) middle stage 2 bias |
| | [3-0] | 0100 | lbi_discr2 | Set discriminator (High Th. Time Trigger) input stage bias |
| 11 | [7-4] | 0100 | lbm1_discr2 | Set discriminator (High Th. Time Trigger) middle stage 1 bias |
| | [3-0] | 0100 | lbm2_discr2 | Set discriminator (High Th. Time Trigger) middle stage 2 bias |
| 12 | [7-4] | 0100 | lbi_discrcharge | Set discriminator (Charge Trigger) input stage bias |
| | [3-0] | 0100 | lbo_discrcharge | Set discriminator (Charge Trigger) output stage bias |
| 13 | 7 | 1 | ON_inDac0 | Enable bias of Input DAC0 0 – disabled 1 – enabled (default) |
| | 6 | 1 | ON_inDac1 | Enable bias of Input DAC1 0 – disabled 1 – enabled (default) |
| | 5 | 1 | ON_paT | Enable pre-amp (Time Trigger) 0 – disabled 1 – enabled (default) |
| | 4 | 1 | ON_paHG | Enable pre-amp (High Gain Shaper) 0 – disabled 1 – enabled (default) |
| | 3 | 1 | ON_paLG | Enable pre-amp (Low Gain Shaper) 0 – disabled 1 – enabled (default) |
| | 2 | 1 | ON_shHG | Enable High Gain Shaper 0 – disabled 1 – enabled (default) |



| | | | | |
|----|-------|------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 14 | 1 | 1 | ON_shLG | Enable Low Gain Shaper 0 – disabled 1 – enabled (default) |
| | 0 | 1 | ON_pdetector | Enable peak detector 0 – disabled 1 – enabled (default) |
| | [7-5] | 111 | NC | Not Connected |
| | 4 | 1 | ON_calibDac | Enable Trigger threshold calibration stage 0 – disabled 1 – enabled (default) |
| | 3 | 1 | ON_discriCharge | Enable Charge Trigger discriminator 0 – disabled 1 – enabled (default) |
| | 2 | 1 | ON_pdBuffer | Enable peak detector buffer 0 – disabled 1 – enabled (default) |
| | 1 | 1 | ON_discri1 | Enable Low Th. Time Trigger Discriminator 0 – disabled 1 – enabled (default) |
| 0 | 1 | ON_discri2 | Enable High Th. Time Trigger Discriminator 0 – disabled 1 – enabled (default) | |

| | | | | | |
|----|---|-------|----------|------------------------|---------------------------------------------------------------------------------|
| 65 | 0 | [7-6] | 00 | NC | Not Connected |
| | | [5-0] | 100000 | bg[5:0] | Set BandGap reference voltage trimming |
| | 1 | [7-0] | 00000000 | Dac1[7-0] | Set Time Trigger threshold (Low) : Bits [7-0] |
| | | [7-2] | 0000000 | Dac2[5-0] | Set Time Trigger threshold (High) : Bits [5-0] |
| | 2 | [1-0] | 00 | Dac1[9-8] | Set Time Trigger threshold (Low) : Bits [9-8] |
| | | [7-4] | 0000 | DacQ[3-0] | Set Charge Trigger threshold : Bits [3-0] |
| | 3 | [3-0] | 0000 | Dac2[9-6] | Set Time Trigger threshold (High) : Bits [9-6] |
| | | [7-6] | 00 | NC | Not Connected |
| | 4 | [5-0] | 000000 | DacQ[9-4] | Set Charge Trigger threshold : Bits [9-4] |
| | | [7-4] | 0100 | lbi_thresholdDac[3:0] | Set Time threshold DAC input stage bias |
| | 5 | [3-0] | 0100 | lbo_thresholdDac[3:0] | Set Time threshold DAC output stage bias |
| | | [7-4] | 0100 | lbi_thresholdDacQ[3:0] | Set Charge threshold DAC input stage bias |
| | 6 | [3-0] | 0100 | lbo_thresholdDacQ[3:0] | Set Charge threshold DAC output stage bias |
| | | [7-4] | 0000 | NC | Not Connected |
| | 7 | 3 | 1 | EN_th1 | Enable Time Trigger threshold (Low) : 0 – disabled 1 – enabled (default) |
| | | 2 | 1 | EN_th2 | Enable Time Trigger threshold (High) : 0 – disabled 1 – enabled (default) |
| | | 1 | 1 | EN_thQ | Enable Charge Trigger threshold : 0 – disabled 1 – enabled (default) |



| | | | | | |
|--|----|-------|----------|-----------------------|--------------------------------------------------------------------------------------|
| | | 0 | 1 | EN_bg | Enable BandGap reference voltage : 0 – disabled 1 – enabled (default) |
| | 8 | [7-0] | 11111111 | delay[7:0] | Set delay for peak detector |
| | 9 | [7-4] | 0100 | slopeTrim[3:0] | Set delay slope value to adjust the delay dynamic range. |
| | | [3-0] | 0100 | ibi_discri_delay[3:0] | Set discriminator first stage bias current |
| | 10 | [7-4] | 0100 | ibm_discri_delay[3:0] | Set delay discriminator second |
| | | [3-0] | 0100 | ibo_discri_delay[3:0] | Set third stage bias current |
| | 11 | [7-4] | 0100 | ibi_delayDac[3:0] | Set delay threshold DAC bias current input stage |
| | | [3-0] | 0100 | ibo_delayDac[3:0] | Set delay threshold DAC bias current output stage |
| | 12 | [7-6] | 000 | NC | Not Connected |
| | | 5 | 1 | EN_delay | Enable delay cell : 0 – disabled 1 – enabled (default) |
| | | 4 | 0 | selHoldExt | Select Hold input : 0 – internal (default) 1 – external |
| | | [3-0] | 0100 | selTrig[3:0] | Trigger selection for peak detector and delay box |
| | 66 | [7-2] | 000000 | NC | Not Connected |
| | | 1 | 0 | cmd_globalTrigger | Probe switch command for the global trigger 0 – disabled (default) 1 – enabled |
| | | 0 | 0 | cmd_hold | Probe switch command for hold signals 0 – disabled (default) 1 – enabled |

| | | | | | |
|----|-----|-------|-------|--------------|-------------------------------------------------|
| 66 | 0 | [7-6] | 00 | cm[1:0], | outing selection for channel 0 |
| | | [5-4] | 00 | lvdsOut[1:0] | |
| | | [3-2] | 01 | outPad2[1:0] | |
| | | [1-0] | 00 | outPad[1:0] | |
| | 1 | [7-6] | 00 | cm[1:0], | outing selection for channel 1 |
| | | [5-4] | 00 | lvdsOut[1:0] | |
| | | [3-2] | 01 | outPad2[1:0] | |
| | | [1-0] | 00 | outPad[1:0] | |
| | ... | ... | ... | ... | ... |
| | 63 | [7-6] | 00 | cm[1:0], | outing selection for channel 63 |
| | | [5-4] | 00 | lvdsOut[1:0] | |
| | | [3-2] | 01 | outPad2[1:0] | |
| | | [1-0] | 00 | outPad[1:0] | |
| | 64 | 7 | 1 | NC | Not Connected |
| | | [6-5] | 01 | delayPE[1:0] | Setting for CLPS driver pre-emphasis delay |
| | | [4-0] | 00000 | bufSize[4:0] | Set buffer size for single ended trigger output |



| | | | | |
|----|-------|------|--------------------|----------------------------------------------------------------------------|
| 65 | [7-4] | 1111 | bufSizeClps[3:0] | Setting for CLPS driver strength |
| | [3-0] | 1111 | bufSizePE[3:0] | Setting for CLPS driver pre-emphasis |
| 66 | [7-6] | 11 | NC | Not Connected |
| | [5-4] | 11 | cmProbe[1:0] | Set compensation capacitor value for probe buffer |
| | [3-2] | 11 | cmLG[1:0] | Set compensation capacitor value for low gain buffer |
| | [1-0] | 11 | cmHG[1:0] | Set compensation capacitor value for high gain buffer |
| 67 | [7-4] | 0100 | ibi_aBuffer[3:0] | Set analog buffers first stage bias current (probe and OUT_AMUXLG/HG) |
| | [3-0] | 0100 | ibFCP_aBuffer[3:0] | Set analog buffers second stage bias current (probe and OUT_AMUXLG /HG) |
| 68 | [7-4] | 0100 | ibFCN_aBuffer[3:0] | Set analog buffers second stage bias current (probe and OUT_AMUXLG /HG) |
| | [3-0] | 0100 | ibi_outing[3:0] | Set analog buffers first stage bias current (OUT1 and OUT2) |
| 69 | [7-4] | 0100 | ibFCP_outing[3:0] | Set analog buffers second stage current (OUT1 and OUT2) |
| | [3-0] | 0100 | ibFCN_outing[3:0] | Set analog buffers second stage current (OUT1 and OUT2) |
| 70 | [7-5] | 000 | NC | Not Connected |
| | 4 | 0 | ON_outing | Power on bit for analogue buffers driving OUT1 and OUT2 |
| | 3 | 1 | ON_aBuffer | Power on bit for probe and analog multiplexer's buffers |
| | 2 | 0 | EN_probe | Enable bit for analogue probe |
| | 1 | 1 | EN_aMuxHG | Enable bit for multiplexer buffer for high gain measurement |
| | 0 | 1 | EN_aMuxLG | Enable bit for analogue probe, multiplexer buffer for low gain measurement |

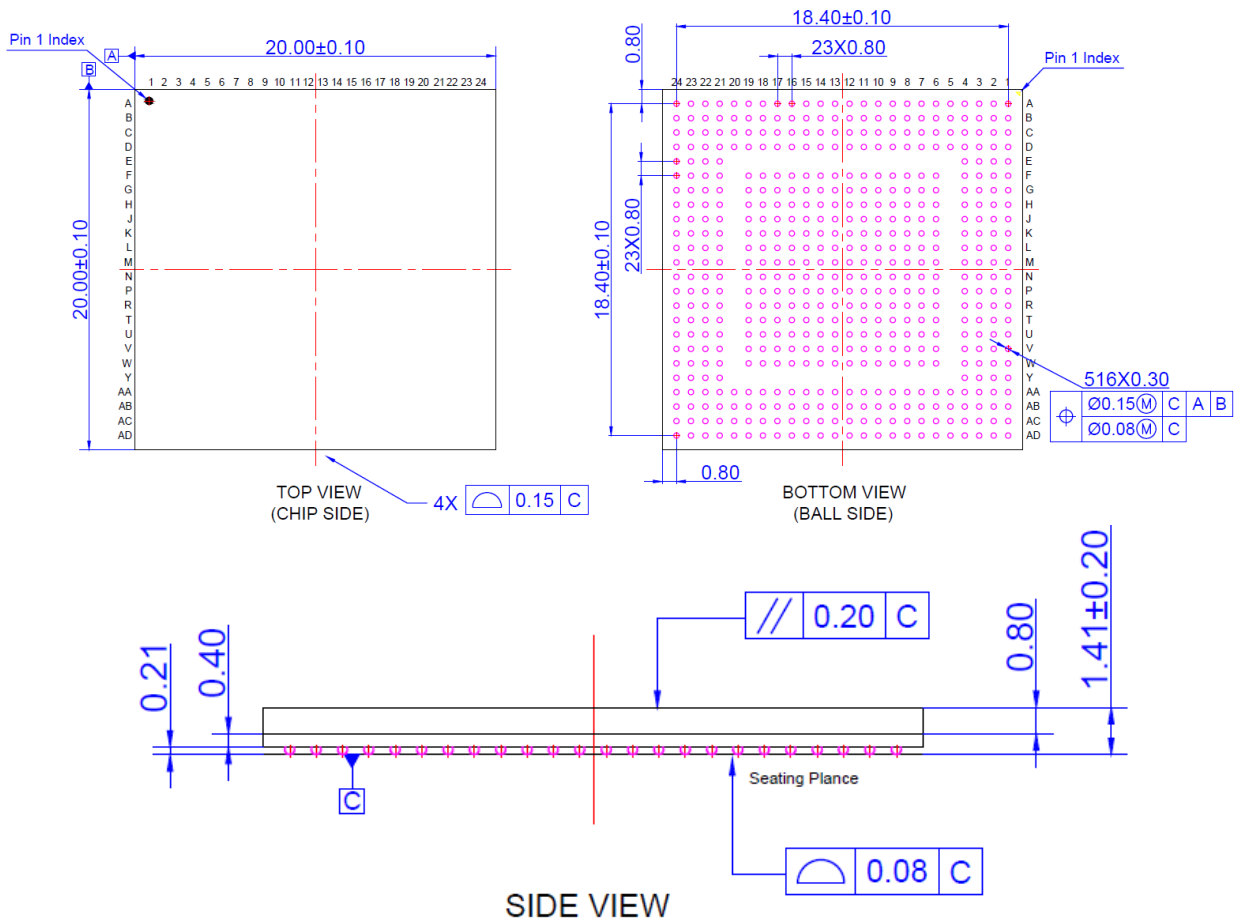
| | | | | | |
|----|---|-------|--------|---------------|------------------------------------------------------------------------------------------------------|
| 67 | 0 | [7-2] | 000000 | NC | Not Connected |
| | | 1 | 1 | EN_Rx | Enable bit for the differential receiver (valid event signal) 0 : Disable 1 : Enable (default) |
| | | 0 | 0 | Forced_ValEvt | Enable bit for forced valid event bit 0 : External (default) 1 : Internal |

Table 4 - Radioroc Slow Control list

Specifically, for Address 0-63, each subadd in this section will correspond only to the selected channel. This means that in order to have channel wide operation each Address will have to be selected when writing the Slow Control operation. All the other Addresses (64-67) operations will be effective for the whole ASIC.

Pinout, Power supplies & mechanics

Mechanics





Ball-out

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|------------|--------|-------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------|------------|----------|------------|------------|------------|--------|--------|--------|-----|-----|-----|-----|--------|--------|--------|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|--------|--------|----|-----|-----|-----|-----|--------|--------|----|-----|-----|-----|-----|--------|--------|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|--------|--------|--------|-----|-----|-----|-----|--------|--------|--------|-----|-----|-----|-----|
| A | in<53> | in<55> | in<57> | in<59> | in<61> | in<63> | in<62> | reset_n | sda | clk_sm_i2c | valevent_n | valevent_p | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | in<51> | in<52> | in<54> | in<56> | in<58> | in<60> | in_ctest | rstn_probe | rstn_i2c | scl | rstn_sc | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | in<49> | in<50> | vcp_outing | NC | NC | NC | NC | NC | NC | NC | NC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | in<47> | in<48> | vcn_outing | NC | NC | NC | NC | NC | NC | NC | NC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| E | in<45> | in<46> | vcp_aBuffer | NC | <table border="1"> <tbody> <tr><td>VDD_PA</td><td>VDD_PA</td><td>VDD_PA</td><td>VDD</td><td>VDD</td><td>VDD</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>VDD_PA</td><td>VDD</td><td>VDD</td><td>VDD</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD</td><td>VDD</td><td>NC</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>VDD_PA</td><td>VDD</td><td>VDD</td><td>VDD</td><td>GND</td></tr> <tr><td>VDD_PA</td><td>VDD_PA</td><td>VDD_PA</td><td>VDD</td><td>VDD</td><td>VDD</td><td>GND</td></tr> </tbody> </table> | | | | | | | | VDD_PA | VDD_PA | VDD_PA | VDD | VDD | VDD | GND | VDD_PA | VDD_PA | VDD_PA | VDD | VDD | VDD | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD_PA | VDD_PA | NC | GND | GND | GND | GND | VDD_PA | VDD_PA | NC | GND | GND | GND | GND | VDD_PA | VDD_PA | NC | GND | GND | GND | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD | VDD | NC | GND | GND | GND | GND | VDD_PA | VDD_PA | VDD_PA | VDD | VDD | VDD | GND | VDD_PA | VDD_PA | VDD_PA | VDD | VDD | VDD | GND |
| VDD_PA | VDD_PA | VDD_PA | VDD | VDD | | | | | | | | | VDD | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | VDD_PA | VDD | VDD | | | | | | | | | VDD | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | VDD | NC | GND | GND | | | | | | | | | GND | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | VDD_PA | VDD | VDD | | | | | | | | | VDD | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD_PA | VDD_PA | VDD_PA | VDD | VDD | | | | | | | | | VDD | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| F | in<43> | in<44> | vcn_aBuffer | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| G | in<41> | in<42> | vref_thDacQ | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| H | in<39> | in<40> | vref_thDac | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| J | in<37> | in<38> | thresholdQ | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| K | in<35> | in<36> | threshold2 | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| L | in<33> | in<34> | threshold1 | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| M | out_aMuxLG | in<32> | out_aprobe | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N | out_aMuxHG | in<30> | vref_1v | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| P | in<31> | in<28> | vbg | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R | in<29> | in<26> | vbias_1v | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T | in<27> | in<24> | vref_inDac | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| U | in<25> | in<22> | vcasc_paT | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | in<23> | in<20> | vcasc_paQ | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W | in<21> | in<18> | vref_sh | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Y | in<19> | in<16> | vcp_pdetect | NC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Z | in<17> | in<14> | vcn_pdetect | NC | NC | NC | NC | NC | NC | NC | NC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AA | in<15> | in<12> | vref_delay | NC | NC | NC | NC | NC | NC | NC | NC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AB | in<13> | in<10> | in<8> | in<6> | in<4> | in<2> | Vth_delay | ib_paT | NC | NC | NC | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AC | in<11> | in<9> | in<7> | in<5> | in<3> | in<1> | in<0> | reserved | holdExt | out_dprobe | trigExt | NOR_T1oc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Figure 6 - RADIOROC Ball-out East part



| | | | | | | | | | | | | |
|----------|-----------|----------|----------|----------|----------|----------|----------|----------|------------|------------|------------|----|
| 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |
| ck_read | rstn_read | out1<62> | out2<62> | out1<63> | out2<63> | out1<61> | out2<61> | out1<52> | out2<52> | out1<53> | out2<53> | A |
| NC | NC | out1<60> | out2<60> | out1<56> | out2<56> | out1<59> | out2<59> | out1<50> | out2<50> | out1<51> | out2<51> | B |
| NC | NC | out1<58> | out2<58> | out1<54> | out2<54> | out1<57> | out2<57> | out1<48> | out2<48> | out1<49> | out2<49> | C |
| NC | NC | NC | NC | NC | NC | out1<55> | out2<55> | out1<46> | out2<46> | out1<47> | out2<47> | D |
| | | | | | | | | out1<44> | out2<44> | out1<45> | out2<45> | E |
| | | | | | | | | out1<42> | out2<42> | out1<43> | out2<43> | F |
| DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | out1<40> | out2<40> | out1<41> | out2<41> | G |
| DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | out1<38> | out2<38> | out1<39> | out2<39> | H |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<36> | out2<36> | out1<37> | out2<37> | J |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<34> | out2<34> | out1<35> | out2<35> | K |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<32> | out2<32> | out1<33> | out2<33> | L |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | NC | NC | chip_id<0> | errorn_sc | M |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | NC | chip_id<3> | chip_id<2> | chip_id<1> | N |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<30> | out2<30> | out1<31> | out2<31> | P |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<28> | out2<28> | out1<29> | out2<29> | R |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<26> | out2<26> | out1<27> | out2<27> | T |
| GND | GND | GND | GND | GND | DVDD | DVDD | DVDD | out1<24> | out2<24> | out1<25> | out2<25> | U |
| DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | out1<22> | out2<22> | out1<23> | out2<23> | V |
| DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | DVDD | out1<20> | out2<20> | out1<21> | out2<21> | W |
| | | | | | | | | out1<18> | out2<18> | out1<19> | out2<19> | Y |
| NC | NC | NC | NC | NC | NC | out1<9> | out2<9> | out1<16> | out2<16> | out1<17> | out2<17> | Z |
| NC | NC | out1<4> | out2<4> | out1<8> | out2<8> | out1<7> | out2<7> | out1<14> | out2<14> | out1<15> | out2<15> | AA |
| NC | NC | out1<2> | out2<2> | out1<6> | out2<6> | out1<5> | out2<5> | out1<12> | out2<12> | out1<13> | out2<13> | AB |
| NOR_T2oc | NOR_T0oc | out1<0> | out2<0> | out1<1> | out2<1> | out1<3> | out2<3> | out1<10> | out2<10> | out1<11> | out2<11> | AC |
| 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | |

Figure 7 - RADIOROC ball-out West part



RADIOROC pinout

| Net Name | BGA Ball | Type |
|---------------|----------|---------------------------|
| OUT_AMUXLG | N1 | Multiplexed Analog Output |
| OUT_AMUXHG | M1 | |
| OUT_APROBE | M3 | |
| IB_PAT | AB8 | Voltage Reference |
| RESERVED | AC8 | |
| THRESHOLD1 | L3 | |
| THRESHOLD2 | K3 | |
| THRESHOLDQ | J3 | |
| VBG | P3 | |
| VBIAS_1V | R3 | |
| VCASC_PAO | V3 | |
| VCASC_PAT | U3 | |
| VCN_ABUFFER | F3 | |
| VCN_OUTING | D3 | |
| VCN_PDETECTOR | Z3 | |
| VCP_ABUFFER | E3 | |
| VCP_OUTING | C3 | |
| VCP_PDETECTOR | Y3 | |
| VREF_1V | N3 | |
| VREF_DELAY | AA3 | |
| VREF_INDAC | T3 | |
| VREF_SH | W3 | |
| VREF_THDAC | H3 | |
| VREF_THDACQ | G3 | |
| VTH_DELAY | AB7 | |
| IN_CTEST | B7 | Analog Input |
| CHIP_ID<0> | M23 | I/O Digital Single Ended |
| CHIP_ID<1> | N24 | |
| CHIP_ID<2> | N23 | |
| CHIP_ID<3> | N22 | |
| CK_READ | A13 | |
| CLK_SM_I2C | A10 | |
| ERRORN_OC | M24 | |
| HOLDEXT | AC9 | |
| NOR_T10C | AC12 | |
| NOR_T20C | AC13 | |
| NOR_T00C | AC14 | |
| OUT_DPROBE | AC10 | |

| | | | |
|------------|------|--|---------------------|
| RESET_N | A8 | | |
| RSTN_I2C | B9 | | |
| RSTN_PROBE | B8 | | |
| RSTN_READ | A14 | | |
| RSTN_SC | B11 | | |
| SCL | B10 | | |
| SDA | A9 | | |
| TRIGEXT | AC11 | | |
| DVDD | F13 | | Power Supply - DVDD |
| DVDD | F14 | | |
| DVDD | F15 | | |
| DVDD | F16 | | |
| DVDD | F17 | | |
| DVDD | F18 | | |
| DVDD | F19 | | |
| DVDD | G13 | | |
| DVDD | G14 | | |
| DVDD | G15 | | |
| DVDD | G16 | | |
| DVDD | G17 | | |
| DVDD | G18 | | |
| DVDD | G19 | | |
| DVDD | H18 | | |
| DVDD | H19 | | |
| DVDD | J18 | | |
| DVDD | J19 | | |
| DVDD | K18 | | |
| DVDD | K19 | | |
| DVDD | L18 | | |
| DVDD | L19 | | |
| DVDD | M18 | | |
| DVDD | M19 | | |
| DVDD | N18 | | |
| DVDD | N19 | | |
| DVDD | P18 | | |
| DVDD | P19 | | |
| DVDD | R18 | | |
| DVDD | R19 | | |
| DVDD | T18 | | |
| DVDD | T19 | | |



| | | | |
|------|------|--|--------|
| DVDD | U18 | | |
| DVDD | U19 | | |
| DVDD | V13 | | |
| DVDD | V14 | | |
| DVDD | V15 | | |
| DVDD | V16 | | |
| DVDD | V17 | | |
| DVDD | V18 | | |
| DVDD | V19 | | |
| DVDD | W13 | | |
| DVDD | W14 | | |
| DVDD | W15 | | |
| DVDD | W16 | | |
| DVDD | W17 | | |
| DVDD | W18 | | |
| DVDD | W19 | | |
| GND | AA12 | | Ground |
| GND | AB12 | | |
| GND | B12 | | |
| GND | C12 | | |
| GND | D12 | | |
| GND | F12 | | |
| GND | G12 | | |
| GND | H9 | | |
| GND | H10 | | |
| GND | H11 | | |
| GND | H12 | | |
| GND | H13 | | |
| GND | H14 | | |
| GND | H15 | | |
| GND | H16 | | |
| GND | H17 | | |
| GND | J9 | | |
| GND | J10 | | |
| GND | J11 | | |
| GND | J12 | | |
| GND | J13 | | |
| GND | J14 | | |
| GND | J15 | | |
| GND | J16 | | |
| GND | J17 | | |
| GND | K9 | | |

| | | |
|-----|-----|--|
| GND | K10 | |
| GND | K11 | |
| GND | K12 | |
| GND | K13 | |
| GND | K14 | |
| GND | K15 | |
| GND | K16 | |
| GND | K17 | |
| GND | L9 | |
| GND | L10 | |
| GND | L11 | |
| GND | L12 | |
| GND | L13 | |
| GND | L14 | |
| GND | L15 | |
| GND | L16 | |
| GND | L17 | |
| GND | M9 | |
| GND | M10 | |
| GND | M11 | |
| GND | M12 | |
| GND | M13 | |
| GND | M14 | |
| GND | M15 | |
| GND | M16 | |
| GND | M17 | |
| GND | N9 | |
| GND | N10 | |
| GND | N11 | |
| GND | N12 | |
| GND | N13 | |
| GND | N14 | |
| GND | N15 | |
| GND | N16 | |
| GND | N17 | |
| GND | P9 | |
| GND | P10 | |
| GND | P11 | |
| GND | P12 | |
| GND | P13 | |
| GND | P14 | |
| GND | P15 | |



| | | |
|-------|-----|--------------|
| GND | P16 | |
| GND | P17 | |
| GND | R9 | |
| GND | R10 | |
| GND | R11 | |
| GND | R12 | |
| GND | R13 | |
| GND | R14 | |
| GND | R15 | |
| GND | R16 | |
| GND | R17 | |
| GND | T9 | |
| GND | T10 | |
| GND | T11 | |
| GND | T12 | |
| GND | T13 | |
| GND | T14 | |
| GND | T15 | |
| GND | T16 | |
| GND | T17 | |
| GND | U9 | |
| GND | U10 | |
| GND | U11 | |
| GND | U12 | |
| GND | U13 | |
| GND | U14 | |
| GND | U15 | |
| GND | U16 | |
| GND | U17 | |
| GND | V12 | |
| GND | W12 | |
| GND | Z12 | |
| IN<0> | AC7 | Analog Input |
| IN<1> | AC6 | |
| IN<2> | AB6 | |
| IN<3> | AC5 | |
| IN<4> | AB5 | |
| IN<5> | AC4 | |
| IN<6> | AB4 | |
| IN<7> | AC3 | |
| IN<8> | AB3 | |
| IN<9> | AC2 | |

| | | |
|--------|-----|--|
| IN<10> | AB2 | |
| IN<11> | AC1 | |
| IN<12> | AA2 | |
| IN<13> | AB1 | |
| IN<14> | Z2 | |
| IN<15> | AA1 | |
| IN<16> | Y2 | |
| IN<17> | Z1 | |
| IN<18> | W2 | |
| IN<19> | Y1 | |
| IN<20> | V2 | |
| IN<21> | W1 | |
| IN<22> | U2 | |
| IN<23> | V1 | |
| IN<24> | T2 | |
| IN<25> | U1 | |
| IN<26> | R2 | |
| IN<27> | T1 | |
| IN<28> | P2 | |
| IN<29> | R1 | |
| IN<30> | N2 | |
| IN<31> | P1 | |
| IN<32> | M2 | |
| IN<33> | L1 | |
| IN<34> | L2 | |
| IN<35> | K1 | |
| IN<36> | K2 | |
| IN<37> | J1 | |
| IN<38> | J2 | |
| IN<39> | H1 | |
| IN<40> | H2 | |
| IN<41> | G1 | |
| IN<42> | G2 | |
| IN<43> | F1 | |
| IN<44> | F2 | |
| IN<45> | E1 | |
| IN<46> | E2 | |
| IN<47> | D1 | |
| IN<48> | D2 | |
| IN<49> | C1 | |
| IN<50> | C2 | |
| IN<51> | B1 | |



| | | |
|---------|------|---------------------------------|
| IN<52> | B2 | |
| IN<53> | A1 | |
| IN<54> | B3 | |
| IN<55> | A2 | |
| IN<56> | B4 | |
| IN<57> | A3 | |
| IN<58> | B5 | |
| IN<59> | A4 | |
| IN<60> | B6 | |
| IN<61> | A5 | |
| IN<62> | A7 | |
| IN<63> | A6 | |
| VDD_PA | F6 | |
| VDD_PA | F7 | |
| VDD_PA | F8 | |
| VDD_PA | G6 | |
| VDD_PA | G7 | |
| VDD_PA | G8 | |
| VDD_PA | L6 | |
| VDD_PA | L7 | |
| VDD_PA | M6 | |
| VDD_PA | M7 | |
| VDD_PA | N6 | |
| VDD_PA | N7 | |
| VDD_PA | P6 | |
| VDD_PA | P7 | |
| VDD_PA | V6 | |
| VDD_PA | V7 | |
| VDD_PA | V8 | |
| VDD_PA | W6 | |
| VDD_PA | W7 | |
| VDD_PA | W8 | |
| OUT2<0> | AC16 | I/O Digital Differential (1GHz) |
| OUT2<1> | AC18 | |
| OUT2<2> | AB16 | |
| OUT2<3> | AC20 | |
| OUT2<4> | AA16 | |
| OUT2<5> | AB20 | |
| OUT2<6> | AB18 | |
| OUT2<7> | AA20 | |
| OUT2<8> | AA18 | |
| OUT2<9> | Z20 | |

| | | |
|----------|------|--|
| OUT2<10> | AC22 | |
| OUT2<11> | AC24 | |
| OUT2<12> | AB22 | |
| OUT2<13> | AB24 | |
| OUT2<14> | AA22 | |
| OUT2<15> | AA24 | |
| OUT2<16> | Z22 | |
| OUT2<17> | Z24 | |
| OUT2<18> | Y22 | |
| OUT2<19> | Y24 | |
| OUT2<20> | W22 | |
| OUT2<21> | W24 | |
| OUT2<22> | V22 | |
| OUT2<23> | V24 | |
| OUT2<24> | U22 | |
| OUT2<25> | U24 | |
| OUT2<26> | T22 | |
| OUT2<27> | T24 | |
| OUT2<28> | R22 | |
| OUT2<29> | R24 | |
| OUT2<30> | P22 | |
| OUT2<31> | P24 | |
| OUT2<32> | L22 | |
| OUT2<33> | L24 | |
| OUT2<34> | K22 | |
| OUT2<35> | K24 | |
| OUT2<36> | J22 | |
| OUT2<37> | J24 | |
| OUT2<38> | H22 | |
| OUT2<39> | H24 | |
| OUT2<40> | G22 | |
| OUT2<41> | G24 | |
| OUT2<42> | F22 | |
| OUT2<43> | F24 | |
| OUT2<44> | E22 | |
| OUT2<45> | E24 | |
| OUT2<46> | D22 | |
| OUT2<47> | D24 | |
| OUT2<48> | C22 | |
| OUT2<49> | C24 | |
| OUT2<50> | B22 | |
| OUT2<51> | B24 | |



| | |
|----------|------|
| OUT2<52> | A22 |
| OUT2<53> | A24 |
| OUT2<54> | C18 |
| OUT2<55> | D20 |
| OUT2<56> | B18 |
| OUT2<57> | C20 |
| OUT2<58> | C16 |
| OUT2<59> | B20 |
| OUT2<60> | B16 |
| OUT2<61> | A20 |
| OUT2<62> | A16 |
| OUT2<63> | A18 |
| OUT1<0> | AC15 |
| OUT1<1> | AC17 |
| OUT1<2> | AB15 |
| OUT1<3> | AC19 |
| OUT1<4> | AA15 |
| OUT1<5> | AB19 |
| OUT1<6> | AB17 |
| OUT1<7> | AA19 |
| OUT1<8> | AA17 |
| OUT1<9> | Z19 |
| OUT1<10> | AC21 |
| OUT1<11> | AC23 |
| OUT1<12> | AB21 |
| OUT1<13> | AB23 |
| OUT1<14> | AA21 |
| OUT1<15> | AA23 |
| OUT1<16> | Z21 |
| OUT1<17> | Z23 |
| OUT1<18> | Y21 |
| OUT1<19> | Y23 |
| OUT1<20> | W21 |
| OUT1<21> | W23 |
| OUT1<22> | V21 |
| OUT1<23> | V23 |
| OUT1<24> | U21 |
| OUT1<25> | U23 |
| OUT1<26> | T21 |
| OUT1<27> | T23 |
| OUT1<28> | R21 |
| OUT1<29> | R23 |

| | | |
|------------|-----|----------------------------------|
| OUT1<30> | P21 | |
| OUT1<31> | P23 | |
| OUT1<32> | L21 | |
| OUT1<33> | L23 | |
| OUT1<34> | K21 | |
| OUT1<35> | K23 | |
| OUT1<36> | J21 | |
| OUT1<37> | J23 | |
| OUT1<38> | H21 | |
| OUT1<39> | H23 | |
| OUT1<40> | G21 | |
| OUT1<41> | G23 | |
| OUT1<42> | F21 | |
| OUT1<43> | F23 | |
| OUT1<44> | E21 | |
| OUT1<45> | E23 | |
| OUT1<46> | D21 | |
| OUT1<47> | D23 | |
| OUT1<48> | C21 | |
| OUT1<49> | C23 | |
| OUT1<50> | B21 | |
| OUT1<51> | B23 | |
| OUT1<52> | A21 | |
| OUT1<53> | A23 | |
| OUT1<54> | C17 | |
| OUT1<55> | D19 | |
| OUT1<56> | B17 | |
| OUT1<57> | C19 | |
| OUT1<58> | C15 | |
| OUT1<59> | B19 | |
| OUT1<60> | B15 | |
| OUT1<61> | A19 | |
| OUT1<62> | A15 | |
| OUT1<63> | A17 | |
| VALEVENT_N | A11 | I/O Digital Differential (50MHz) |
| VALEVENT_P | A12 | |
| VDD | F9 | Power Supply - VDD |
| VDD | F10 | |
| VDD | F11 | |
| VDD | G9 | |
| VDD | G10 | |
| VDD | G11 | |



| | | |
|-----|----|--|
| VDD | H6 | |
| VDD | H7 | |
| VDD | J6 | |
| VDD | J7 | |
| VDD | K6 | |
| VDD | K7 | |
| VDD | R6 | |
| VDD | R7 | |
| VDD | T6 | |

| | | |
|-----|-----|--|
| VDD | T7 | |
| VDD | U6 | |
| VDD | U7 | |
| VDD | V9 | |
| VDD | V10 | |
| VDD | V11 | |
| VDD | W9 | |
| VDD | W10 | |
| VDD | W11 | |

Table 5 - Radioroc ASIC pin list

RADIOROC ASIC floorplan & packaging

Preliminary mechanics give a naked die size of 4.72 mm x 11.12 mm including scribe line giving a die area of 52.5 mm². The ASIC has 515 bump pads which will be bonded to BGA substrate.

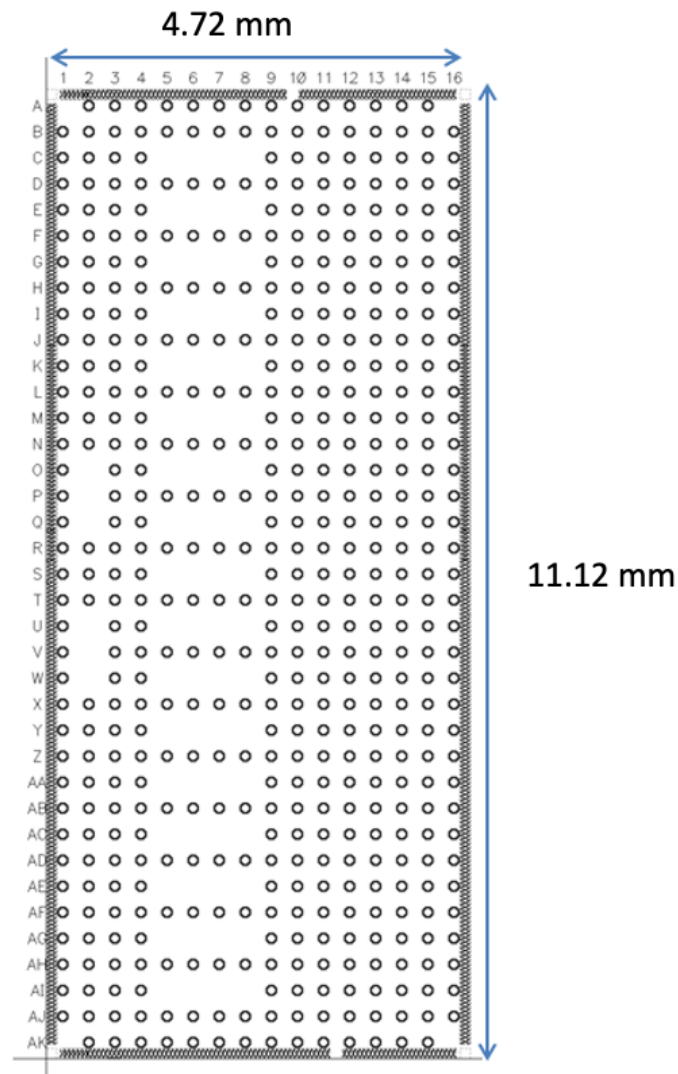


Figure 8 - Preliminary padding and form factor

Power supply

The core of the ASIC is powered by 1.2 V and power supplies are separated in several zone to reduce EMC influence from various sections of the ASIC. It is recommended to at least separate the digital power supply from the analog power supply and to use decoupling capacitors for stabilizing & filtering of the power supply.

| Pin Name | Pin Type | Description | Connected to |
|----------|--------------|--------------------------|--------------|
| VDD_PA | Power Supply | Input stage power supply | 1.2V |
| VDD | Power Supply | Analog power supply | 1.2V |
| DVDD | Power Supply | Digital power supply | 1.2V |
| GND | Ground | Ground | 0 |

Input connection

The input pins are solely reserved for the detector inputs (SiPM). Short distance of traces for routing the input signal is highly recommended. Suggestions of the input connection are shown in Figure 9 and Figure 10.

| Pin Name | Ball Map | Description | Connected to |
|----------|-------------------------------------|------------------------|-----------------------------|
| in<0:63> | Various location (refer to Table 5) | Connection to detector | Detector anodes or cathodes |

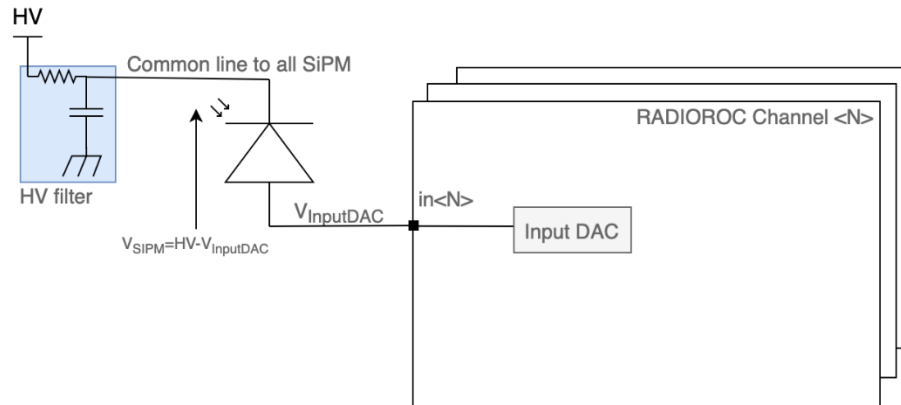


Figure 9 - SiPM connection suggestion without external impedance

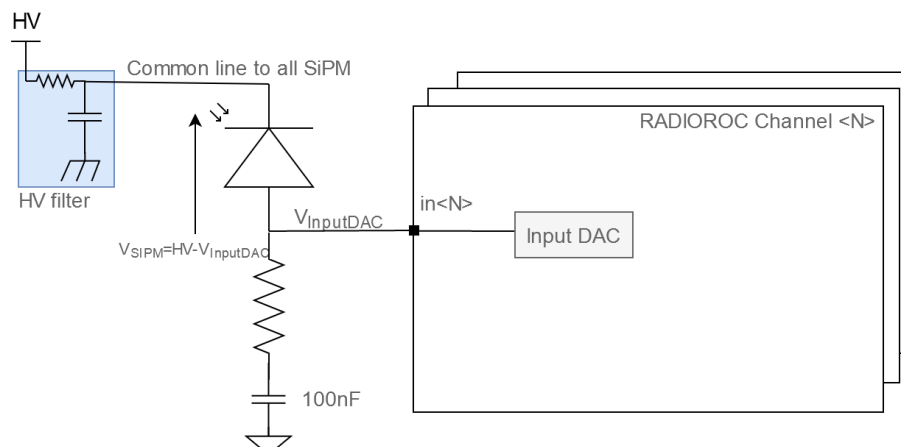


Figure 10 - SiPM connection suggestion with external impedance

Biasing & debugging connections

Biasing pins are mostly optional I/Os which are available for debugging and modifying analog section biasing if required. It could be left open or connected to decoupling capacitors in most cases. However, if a biasing modification is required, it is also possible to connect the pin to resistor-based voltage divider (refer Figure 11). The expected DC value of each pin can be found in Table 2. Additionally, the proposed connection for debugging and analog readout pins (OUT_AMUXLG, OUT_AMUXHG, OUT_APROBE & IN_CTEST) is shown in Figure 12 and Figure 13.

| Pin Name | Ball Map | Description | Connected to |
|------------|----------|-------------------------------------|----------------------------------|
| OUT_AMUXLG | N1 | Multiplexed Low Gain Shaper output | ADC/ Analog buffer /Oscilloscope |
| OUT_AMUXHG | M1 | Multiplexed High Gain Shaper output | ADC/ Analog buffer /Oscilloscope |



| | | | |
|---------------|------------------|------------------------------------------------|------------------------------------------------------------|
| OUT_APROBE | M3 | Analog Probe monitoring output | Analog buffer & oscilloscope |
| IB_PAT | AB8 | Input stage Time Trigger pre-amp bias | Not connected, decoupling capacitor and/or voltage divider |
| OUT1<0:63> | Various location | High Gain/Low Gain output | ADC/ Analog buffer /Oscilloscope |
| OUT2<0:63> | Various location | High Gain/Low Gain output | ADC/ Analog buffer /Oscilloscope |
| THRESHOLD1 | L3 | Time Trigger threshold (low) | Decoupling capacitor |
| THRESHOLD2 | K3 | Time Trigger threshold (high) | Decoupling capacitor |
| THRESHOLDQ | J3 | Charge Trigger threshold | Decoupling capacitor |
| VBG | P3 | Bandgap output | Decoupling capacitor |
| VBIAS_1V | R3 | 1V low impedance bias output | Decoupling capacitor |
| VCASC_PAQ | V3 | Shaper pre-amp cascode voltage | Decoupling capacitor and/or voltage divider |
| VCASC_PAT | U3 | Pre-amp cascode voltage | Decoupling capacitor and/or voltage divider |
| VCN_ABUFFER | F3 | Analog buffer amp cascode N voltage | Decoupling capacitor and/or voltage divider |
| VCN_OUTING | D3 | Output buffer amp cascode N voltage | Decoupling capacitor and/or voltage divider |
| VCN_PDETECTOR | Z3 | Peak detector cascode N voltage | Decoupling capacitor and/or voltage divider |
| VCP_ABUFFER | E3 | Analog buffer amp cascode P voltage | Decoupling capacitor and/or voltage divider |
| VCP_OUTING | C3 | Output buffer amp cascode P voltage | Decoupling capacitor and/or voltage divider |
| VCP_PDETECTOR | Y3 | Peak detector cascode P voltage | Decoupling capacitor and/or voltage divider |
| VREF_1V | N3 | 1V low impedance ref output | Decoupling capacitor |
| VREF_DELAY | AA3 | Delay cell reference voltage | Decoupling capacitor and/or voltage divider |
| VREF_INDAC | T3 | Input DAC reference voltage | Decoupling capacitor and/or voltage divider |
| VREF_SH | W3 | Shaper reference voltage | Decoupling capacitor and/or voltage divider |
| VREF_THDAC | H3 | Time Trigger threshold DAC reference voltage | Decoupling capacitor and/or voltage divider |
| VREF_THDACQ | G3 | Charge Trigger threshold DAC reference voltage | Decoupling capacitor and/or voltage divider |
| VTH_DELAY | AB7 | Delay cell threshold output | Decoupling capacitor |
| IN_CTEST | B7 | Charge injection input | Waveform generator or pulser |

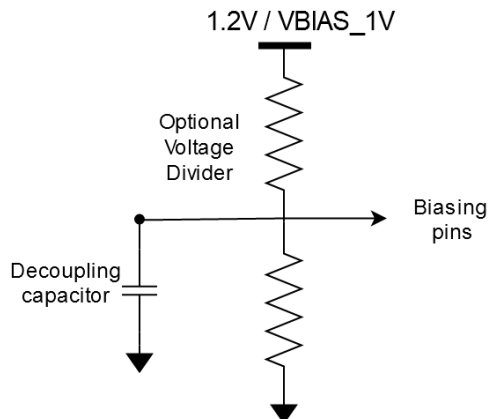


Figure 11 - Proposed connection for biasing points.

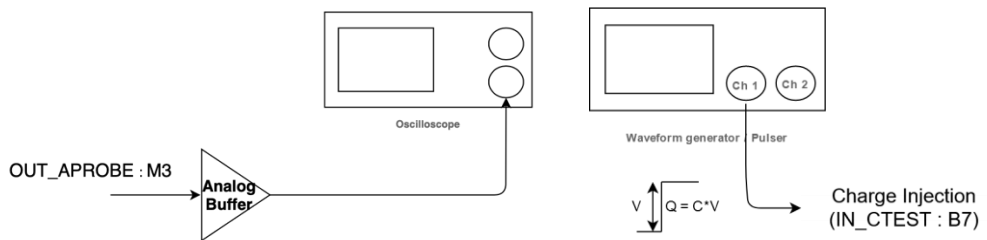


Figure 12 - Proposed connection for OUT_APROBE (Left figure) and IN_CTEST (Right figure)

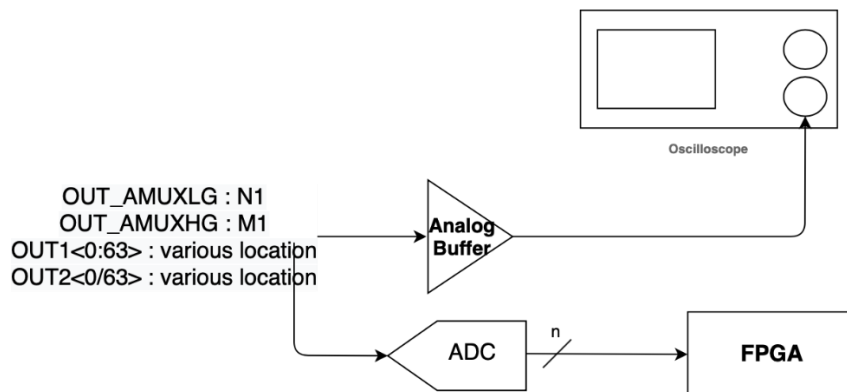


Figure 13 - Proposed connection for OUT_AMUXLG, OUT_AMUXHG, OUT1<0:63> and OUT2<0:63>



Digital connections

The digital I/Os are divided into 3 types : single-ended, bidirectional and differential (CLPS²). The proposed connection for bidirectional and differential pins are shown in Figure 14. The pins are active high unless it is stated to be active low. Additionally, suggestions of connecting various digital I/Os are also shown in Figure 15 and Figure 16.

| Pin Name | Ball Map | Description | Connected to |
|--------------|----------------------|----------------------------------------------------------------------------------------------------|-----------------------------------------------|
| CHIP_ID<0:3> | M23,N24, N23, N22 | Chip ID for I2C (RADIOROC CHIP_ID<0:3> = "0001") : Single Ended | FPGA |
| CLK_SM_I2C | A10 | Clock for I2C slave core : Single Ended | FPGA |
| ERRORN_SC | M24 | Slow Control reset error : Single Ended, active low | FPGA |
| CK_READ | A13 | Clock for read register : Single Ended | FPGA |
| RSTN_READ | A14 | Low level reset for read register : Single Ended, active low | FPGA |
| RESET_N | A8 | Low level reset for digital part : Single Ended, active low | FPGA |
| RSTN_PROBE | B8 | Low level reset for probe (analog debugging & signal monitoring) : Single Ended, active low. | FPGA |
| RSTN_I2C | B9 | Low level reset for I2C slave core : Single Ended, active low. | FPGA |
| SCL | B10 | SCL line for I2C : Bidir | FGPA with 47k Ohm pull up resistor to 1.2V |
| SCA | A9 | SDA line for I2C : Bidir | FGPA with 47k Ohm pull up resistor to 1.2V |
| NOR_T10C | AC12 | NOR gate Time trigger output (Low threshold) : Single Ended, open collector | FPGA/Oscilloscope |
| NOR_T20C | AC13 | NOR gate Time trigger output (High threshold) : Single Ended, open collector | FPGA/Oscilloscope |
| NOR_TQOC | AC14 | NOR gate Charge trigger output : Single Ended, open collector | FPGA/Oscilloscope |
| OUT_DPROBE | AC10 | Multiplexed digital probe(monitored) output : Single Ended | FPGA/Oscilloscope |
| HOLDEXT | AC9 | External hold signal for peak detector : Single Ended | FPGA/Waveform generator |
| TRIGEXT | AC11 | External trigger: Single Ended | FPGA/Waveform generator |
| RSTN_SC | B11 | Low level reset for trigger Slow Control : Single Ended, active low | FPGA |
| VALEVENT_N/P | A11/12 | Differential fast discriminator masking inputs : CLPS | FPGA |

² CLPS stand for CERN Low Power Signaling. It is not a fairly common digital I/Os standard. The common voltage is set at 0.6V with signal swing of 300mV.

| | | | |
|------------|------------------|------------------------------------------------------|------|
| OUT1<0:63> | Various location | Single ended/Differential (refer to readout setting) | FPGA |
| OUT2<0:63> | Various location | Single ended/Differential (refer to readout setting) | FPGA |

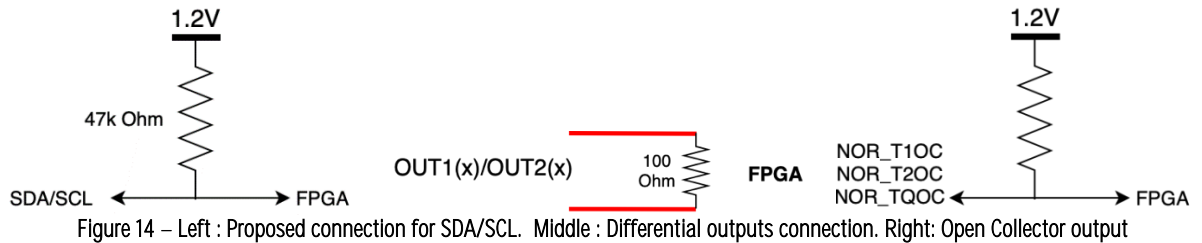


Figure 14 – Left : Proposed connection for SDA/SCL. Middle : Differential outputs connection. Right: Open Collector output

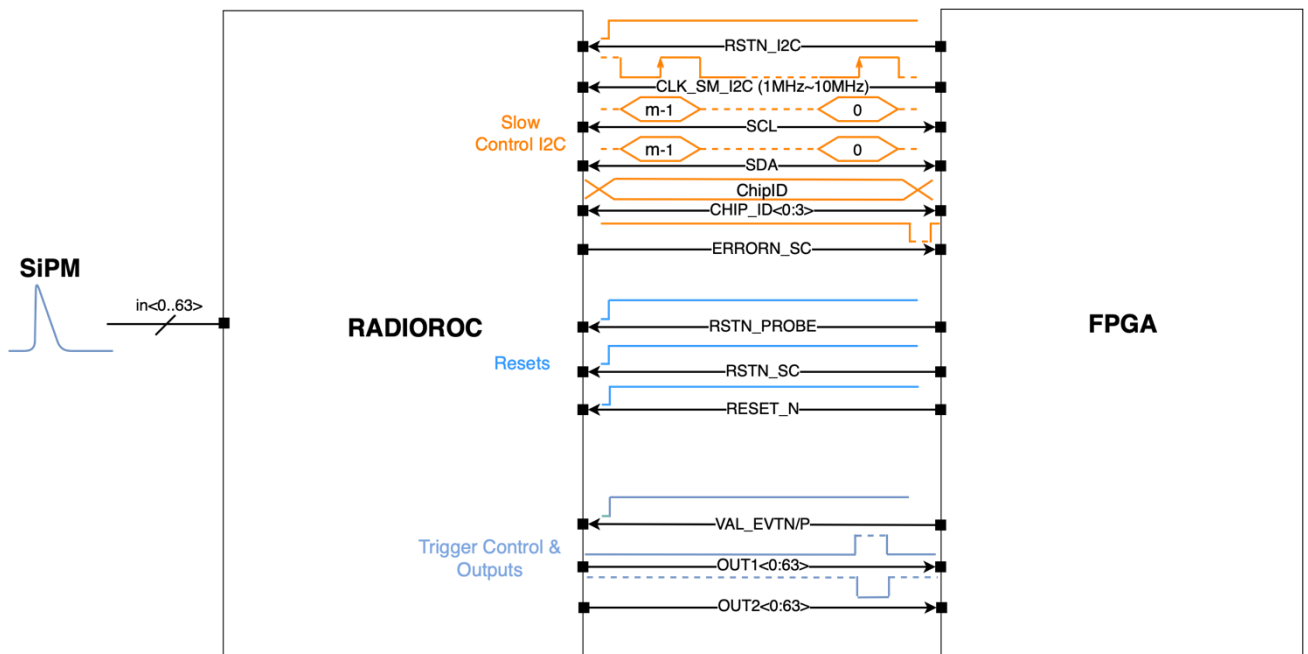


Figure 15 – Trigger outputs, Resets and I2C for Slow Control connections suggestion

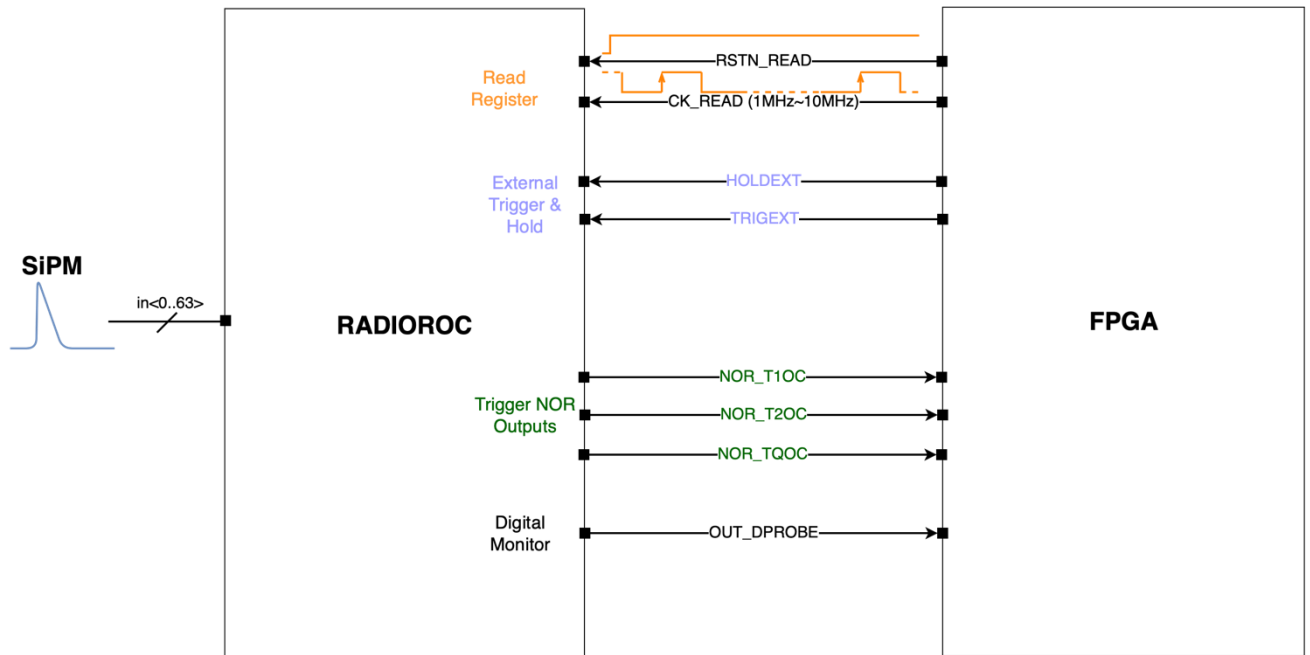


Figure 16 – Read Register, external control inputs, NOR trigger outputs and Digital monitor connections suggestion

RADIOROC analog operation

The analog part of RADIOROC is composed of the input DAC, pre-amplifier for input signal discrimination & triggering, and finally two shapers (High Gain and Low Gain). Schematic diagram of the analog section is shown in Figure 17.

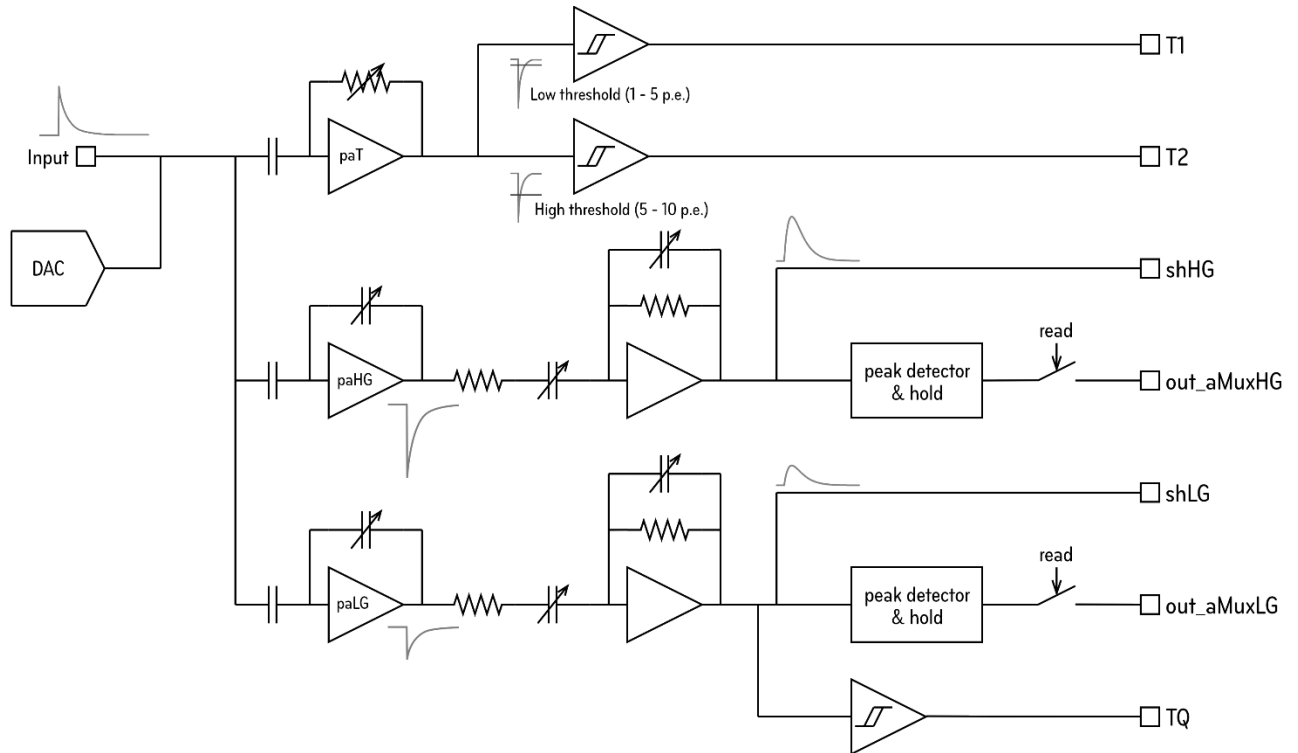


Figure 17 - RADIOROC Analog Section

Input DAC

The input DAC can be used to adjust the SiPM overvoltage channel per channel. This feature can be used to correct the detector non-uniformity. An example of SiPM connection is illustrated in the Figure 9. The input DAC value can be set through the following Slow Control bits:

- *InDAC* (Address: 0-63; Subadd: 0; Bits: 7-0). Voltage span: 50mV ~ 600mV. Step ~2mV.

It is worth noting that two input DAC are available. One can provide a 100 Ohm impedance at the ASIC input meaning the user can plug a SiPM directly on the ASIC input without the need of an external resistor. The other one has a high impedance output so an external resistor is needed, in series with a 100 nF capacitor to the ground to preserve the DC level at the DAC output. Both DAC have the same dynamic range and LSB values. The DAC selection is done by the Slow Control bit:

- *DAC_select* (Address: 0-63; Subadd: 6; Bits: 7).

When using the DAC providing a 100 Ohm impedance, beware that large input signals can saturate the pre-amplifier, impeding the input impedance by creating a high frequency resonance and thus high frequency oscillations.

Time pre-amplifier

This ASIC only accepts positive polarity inputs and the output of the “time” pre-amplifier is fed into two discriminators. This pre-amplifier has a variable gain adjustment accessible through Slow Control bits:

- *patGain* (Address: 0-63; Subadd: 1; Bits: 5-0). Close-loop gain span: 15 (central bandwidth frequency = 480 MHz) ~ 100 (central bandwidth frequency = 55 MHz).

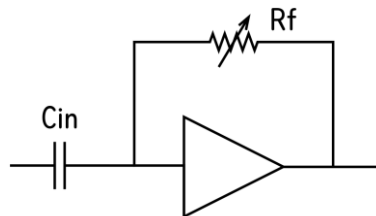


Figure 18 – Time pre-amplifier block diagram

The Slow Control bits (*patGain* (Address: 0-63; Subadd: 1; Bits: 5-0)) will change the value of feedback resistor R_f of the pre-amp. As shown in Figure 19, this will change the gain and also bandwidth of the pre-amplifier. The low-cut frequency is quite high so the pre-amplifier get back to the DC baseline quickly after an event. This allows high frequency photon counting foreseen to be up to 100 MHz.

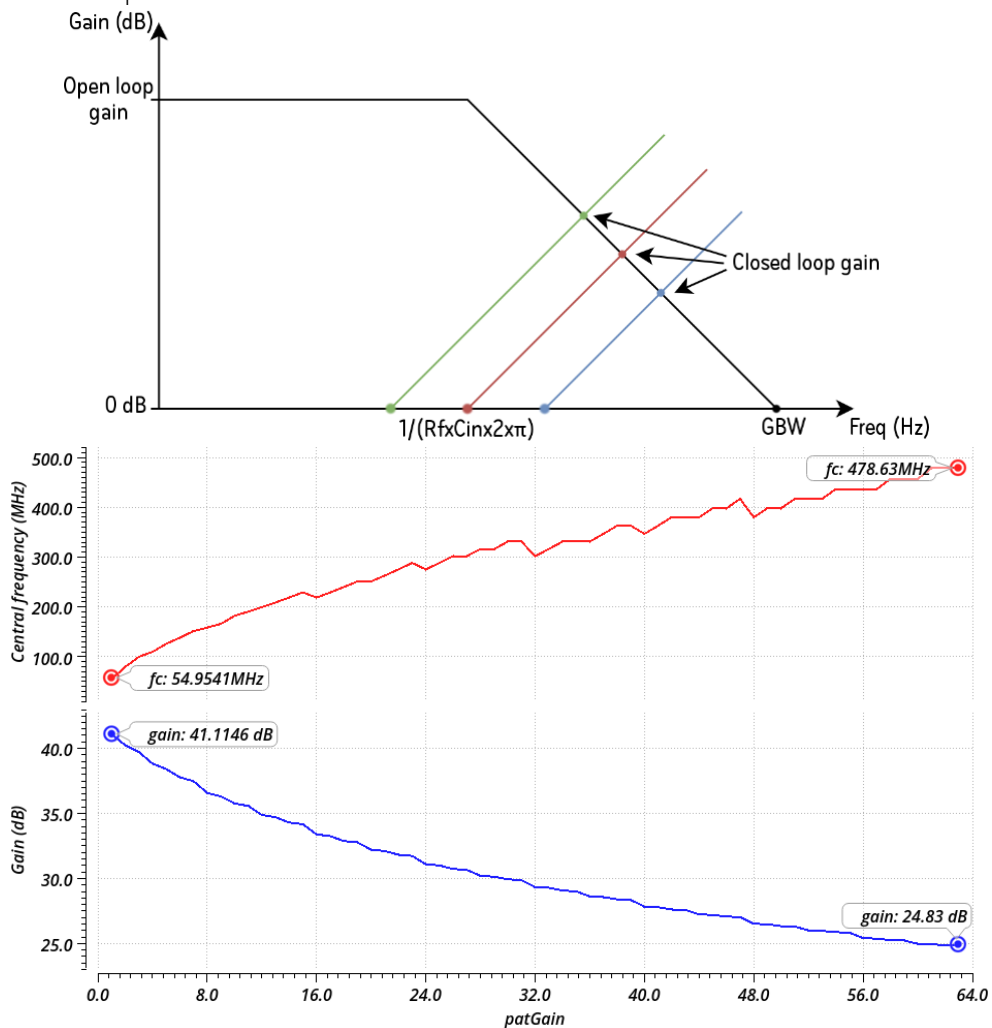


Figure 19 - R_f trimming effect on the closed-loop gain. Simulation results from the layout extracted cell with R and C parasitics.

Discriminators

The first discriminator will generate Low threshold (*DAC1*) Time Trigger output (Trigger T1). The second discriminator will be set with High Threshold (*DAC2*) in order to produce a secondary Time Trigger output (Trigger T2). Threshold value for both triggers can be set from 256mV to 534mV with a step of 0.27mV. The Slow Control bits for both thresholds are as follow :

- (*DAC1*, Address: 65; Subadd: 2; Bits: 1-0 & Subadd: 1; Bits: 7-0). Voltage span: 256mV ~ 534mV. Step = 0.27mV.
- (*DAC2*, Address: 65; Subadd: 3; Bits: 3-0 & Subadd: 2; Bits: 7-2). Voltage span: 256mV ~ 534mV. Step = 0.27mV.

The pre-amplifier output DC value is about 490mV. The schematic diagram of the trigger line is shown in Figure 20.

Both of the trigger outputs are sent into the backend of the ASIC (refer to RADIOROC backend operation). The backend selection will set either one or both triggers on the ASIC output pins.

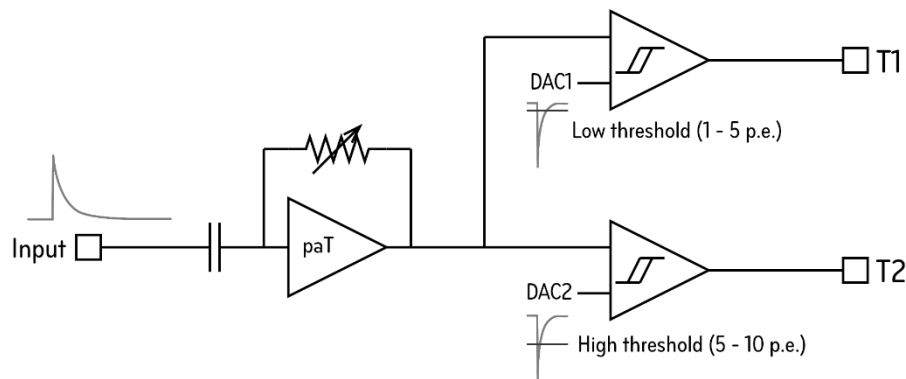


Figure 20 - Pre-amp and Time Trigger block diagram

It is worth noting that the two discriminators can actually be used indiscriminately as their designs and the DAC used to generate the threshold are the exact same. The "Low" and "High" threshold can be inverted to be T2 and T1 respectively. One of the perks of dual threshold triggering is to maximize the time measurement with the Low threshold (less time walk) while filtering dark noise/low energy events with the High threshold. The user can then trigger on single photons and use T1 for time measurement but validate the acquisition only if the second trigger T2 set at 3 p.e. is hit.

Shapers

This ASIC also embeds two shapers (High Gain & Low Gain) which are connected directly to the ASIC input. Both of the shapers have a variable gain pre-amp stage & variable shaping time. The shapers gain can be adjusted channel per channel through Slow Control bits *hgGain* for High Gain shaper and *lgGain* for Low Gain shaper. The Slow Control bits for adjusting the shaper pre-amp gain are the following:

- *hgGain* (Address: 0-63; Subadd: 2; Bits: 3-0). Gain span: 5 ~ 80.
- *lgGain* (Address: 0-63; Subadd: 2; Bits: 7-4). Gain span: 0.5 ~ 8.

The shaping time for both shapers can be adjusted using the Slow Control bits *tauHG* (Address: 0-63; Subadd: 3; Bits: 7-4) for the High Gain shaper and *tauLG* (Address: 0-63; Subadd: 3; Bits: 3-0) for the Low Gain shaper. The Slow Control bits adjusting the shaping time are:

- *tauHG* (Address: 0-63; Subadd: 3; Bits: 7-4). Shaping time span: 20 ns ~ 300 ns. Step = 20 ns
- *tauLG* (Address: 0-63; Subadd: 3; Bits: 3-0). Shaping time span: 20 ns ~ 300 ns. Step = 20 ns

Each of the shaper output will be sent to a peak detector cell which will be connected to an analog multiplexer for external amplitude (charge) measurements. Additionally, the Low Gain shaper signal can be used to generate a “charge” Trigger (TQ) which will be the highest threshold trigger relative to the input signal. The threshold can be set through the following Slow Control bits:

- *DACQ* (Address: 65; Subadd: 4; Bits: 5-0 & Subadd: 3; Bits: 7-4). Voltage span: 75 mV ~ 1,2 V. Step = 1 mV

The DC output level of both shapers is about 100 mV. An illustration of the shapers is depicted in Figure 21.

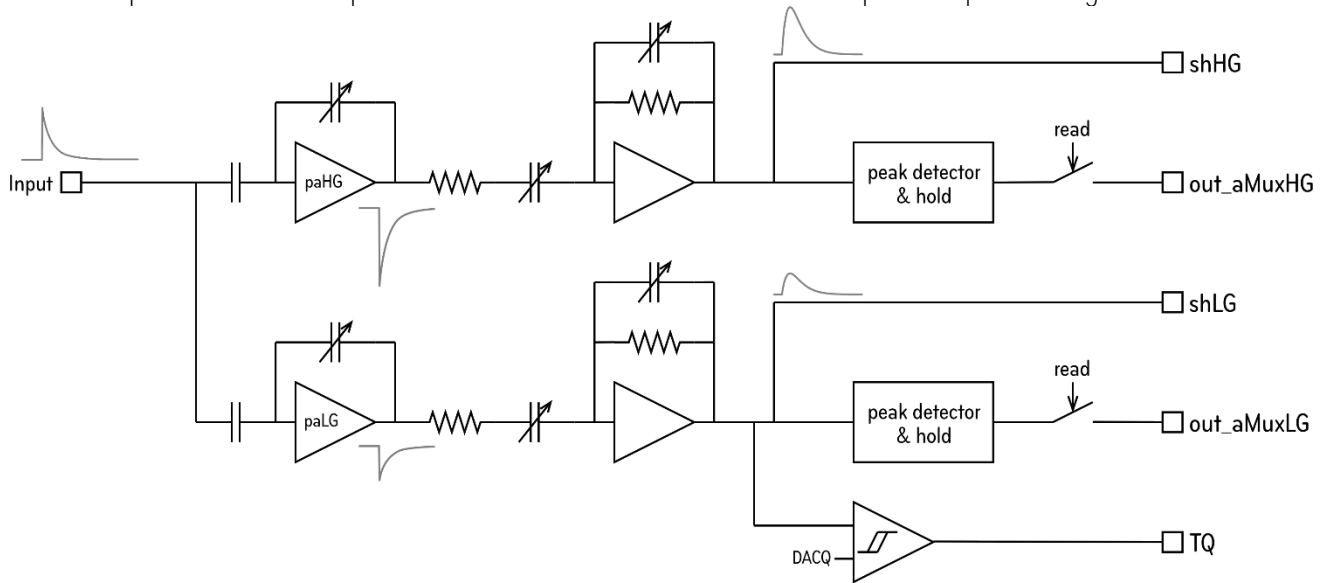


Figure 21 – Charge measurement block diagram.

Peak detectors

Peak detectors are used to sample the amplitude of the shaper signal by conserving the peak analog value of this signal. The operation of the peak detector is illustrated in the Figure 23. Shaper output will be fed into the peak detector cell and Time or Charge trigger (localized or global) will be used as an acquisition trigger to start peak detection. Refer to Figure 22 for acquisition trigger logic. Local trigger denotes the trigger generated within the hit channel and global ASIC trigger denotes the OR output of any trigger in the ASIC. This selection can be done with the following Slow Control bits:

- *selTrig<1:0>* (Address: 65; Subadd: 12 ; Bits: 1-0). The following triggers can be selected:
 - “00” Global ASIC trigger (Refer to *selTrig<3:2>* Slow Control bit) (default);
 - “01” Local Low Threshold Time Trigger T1;
 - “10” Local High Threshold Time Trigger T2;
 - “11” Local Charge Trigger.

When the “*selTrig<1:0>*” is set to “00”, the acquisition trigger enabling the peak detectors is ASIC wide. Therefore, there are several signals which can be used for this purpose and can be set through the following Slow Control bits:

- *selTrig<3:2>* (Address: 65; Subadd: 12; Bits: 3-2). The following triggers can be selected:
 - “00” Ground (meant to be used with TRIGEXT (AC11));
 - “01” Global Low Threshold Time Trigger, T1 (default);
 - “10” Global High Threshold Time Trigger, T2;
 - “11” Global Charge Trigger.

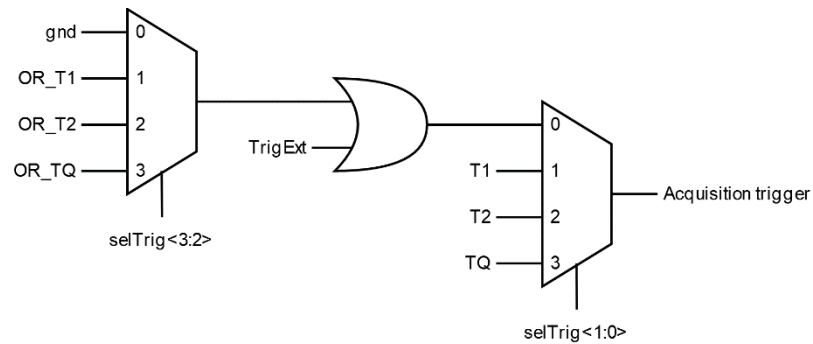


Figure 22 - Acquisition trigger logic.

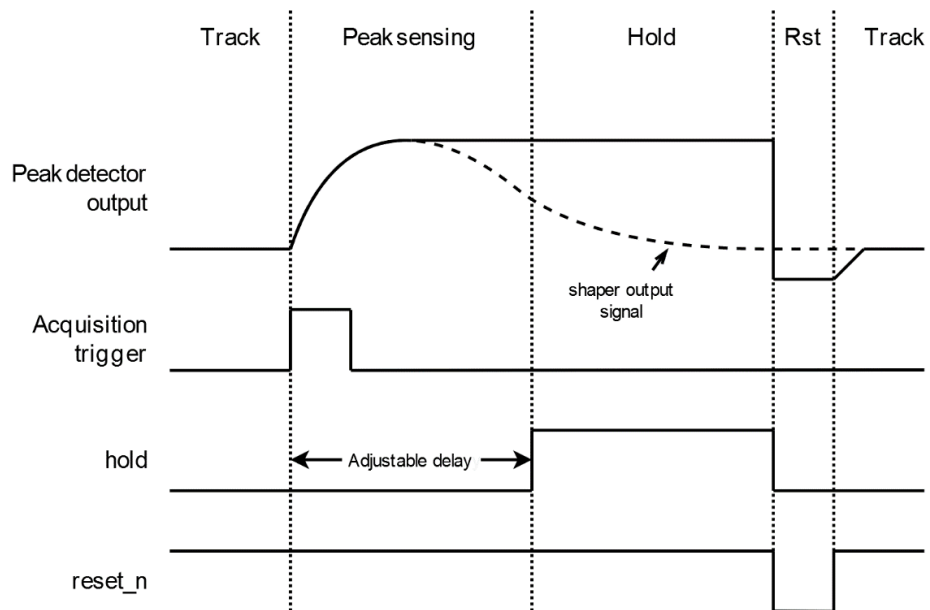


Figure 23 - Illustration of peak detection in RADIOROC.

Additionally, a delay cell (at ASIC level) is used to generate a “hold” signal that opens the input of the peak detector, making it blind to any subsequent event, before sending it to the analog multiplexer output. This delay cell will take as input the acquisition trigger chosen by user (Slow Control bits: *selTrig* (Address: 65; Subadd: 12; Bits: 3-0)). Then a delay can be applied to this trigger using the following Slow Control bits:

- *Delay* (Address: 65; Subadd: 8; Bits: 7-0). Delay span : 2 ns–2.6 μ s. Step size depends on *slopeTrim*,
- *SlopeTrim* (Address: 65; Subadd: 9; bits: 7-4). @0x0 max delay = 60 ns; @0xF max delay = 2.6 μ s.

The hold signal can be fed externally by setting the SC bit *selHoldExt* to '1' (address: 65; subadd: 12; Bit: 4) and using the pin HOLDEXT (AC9, active high).

RADIOROC trigger and backend operation

Outing selection

There are 128 programmable output pins on RADIOROC (2 per channel) and 5 hard-wired. The 5 hard-wired outputs are the 3 logic NOR of the triggers (open collector output), NOR_T1OC (AC12, for T1), NOR_T2OC (AC13, for T2) and NOR_TQOC (AC14, for TQ) and two multiplexed analog outputs OUT_AMUXHG (M1, for High Gain charge measurement), and OUT_AMUXLG (N1, for Low Gain charge measurement). Those two analog outputs are used to read out the analog values stored in the "peak detector and hold" cells.

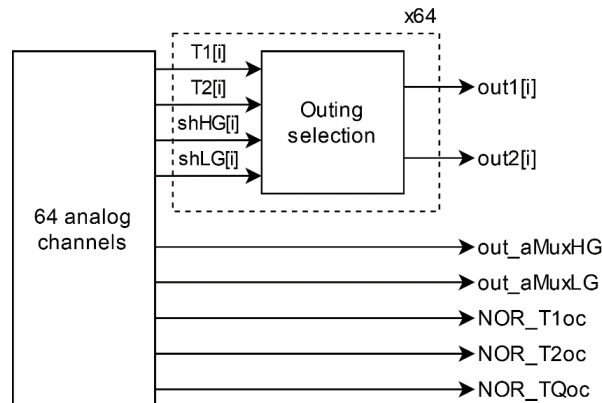


Figure 24 – RADIOROC output schematic.

The following Slow Control bits are used to select the per channel output to be sent to OUT1<0:63> and OUT2<0:63> ballout:

- *IvdsOut[1:0]* (Address: 66; Subadd: 0; Bits: 5-4)
- *outPad1[1:0]* (Address: 66; Subadd: 0; Bits: 1-0)
- *outPad2[1:0]* (Address: 66; Subadd: 0; Bits: 3-2)

IvdsOut has the priority over the *outPad1* and *outPad2* meaning it must be set to "00" to output non-differential signals. It should be noted the differential outputs are only available for both Time Trigger outputs (T1 & T2).

The following values are available for *IvdsOut* Slow Control bits:

- 00 = Differential output disabled, refer to *outPad1* and *outPad2* Slow Control settings;
- 01 = Differential output for Trigger T1;
- 10 = Differential output for Trigger T2;
- 11 = disable all outputs.

The following settings are available for *outPad1* and *outPad2* Slow Control bits:

- 00 = single-ended output for Trigger T1;
- 01 = single-ended output for Trigger T2;
- 10 = High gain slow shaper output;
- 11 = Low gain slow shaper output.

Some examples:

| <i>IvdsOut[1:0]</i> | <i>outPad1[1:0]</i> | <i>outPad2[1:0]</i> | OUT1[i] | OUT2[i] |
|---------------------|---------------------|---------------------|-----------|----------------|
| 00 | 00 | 01 | T1 | T2 |
| 01 | xx | xx | CLPS T1_n | CLPS T1_p |
| 00 | 00 | 10 | T1 | HG slow shaper |

Outputs are programmable channel per channel. For instance, users could choose to output the triggers T1/T2 on OUT1[m]/OUT2[m] and the slow shaper high gain/low gain outputs on OUT1[n]/OUT2[n], etc.

Read register

Operating the analog multiplexers (OUT_AMUXLG and OUT_AMUXHG) for the shapers can be done by accessing the read registers through CK_READ (A13) and RSTN_READ (A14) pins. Operating these registers requires only a low-level reset (RSTN_READ) and a certain number of clock (CK_READ) to be sent to the ASIC. The timing diagram and the expected outputs on OUT_AMUXLG and OUT_AMUXHG pads are shown in Figure 25. This operation should be performed when the peak detector is in hold mode. At the end of the reading procedure the RESET_N pin (A8) should be asserted during 20 ns to reset the peak detectors and delay cell.

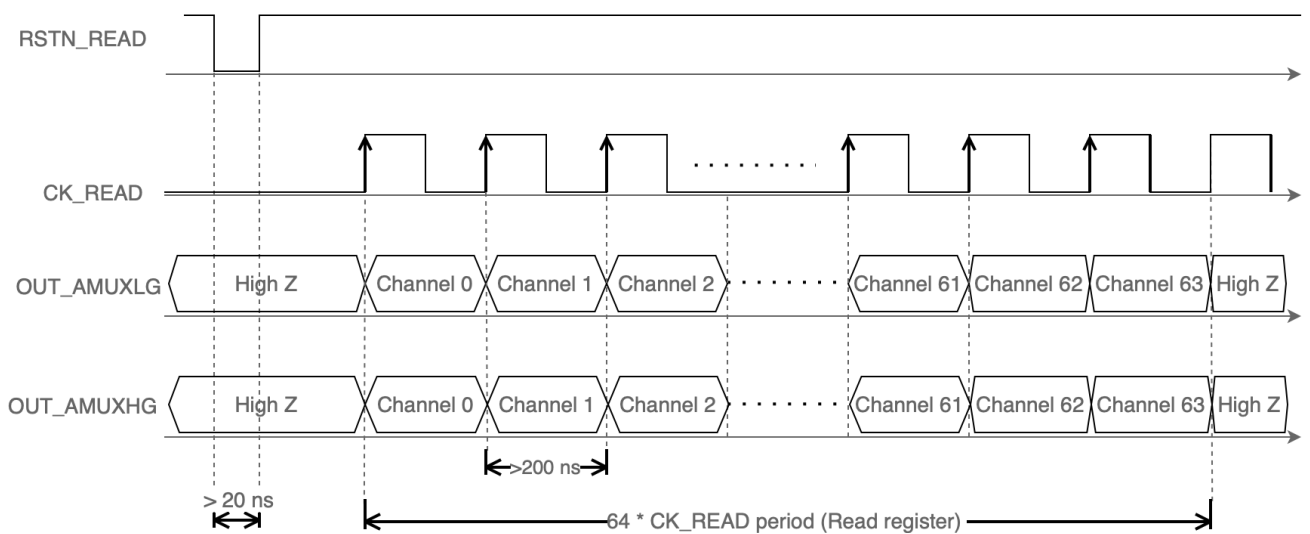


Figure 25 - Analog multiplexer for High Gain and Low Gain shapers readout timing diagram

The RSTN_READ pin can be asserted at the beginning or the end of the data acquisition. The read register just have to be reset between two acquisitions to ensure its correct positioning (see Figure 26).

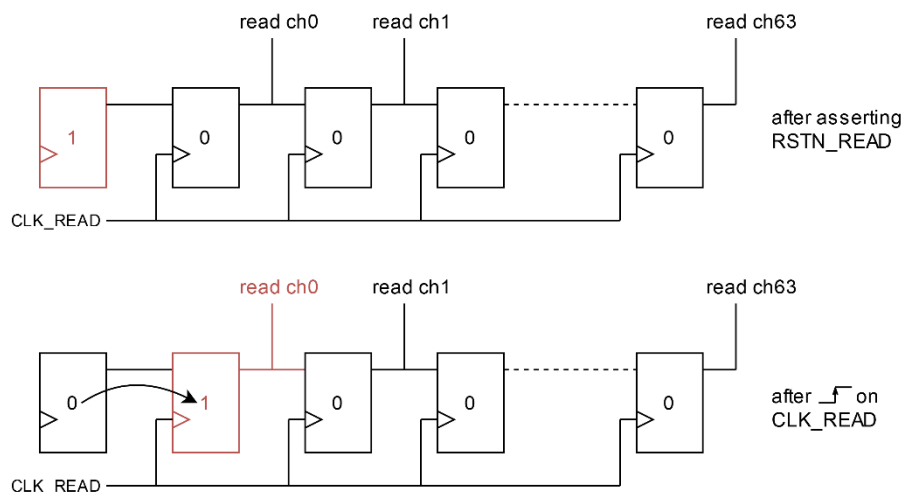


Figure 26 - read register operation.

Data acquisition examples

Example 1: default configuration

On example 1 is considered that the default SC settings are kept for acquisition. The acquisition trigger is the logic OR of trigger T1 with *selTrig* = "0100". The "hold" signal is generated internally by the delay box and after its assertion the DAQ can be started by the user. Please note that the hold signal can't be monitored. The output NOR_T10C has to be monitored to know when an acquisition is started by the ASIC. The user must wait for a selected time depending on the chosen delay before starting to assert the CLK_READ pin. Figure 27 shows an example with an input signal on IN<2>. An external ADC must be used to digitize the analog data on OUT_AMUXHG and OUT_AMUXLG. If the user wants to speed up the DAQ process the CLK_READ can be used to fast forward the read register up to the desired channel (without the need to wait 200 ns per channel) and the ADC will be used to digitize only the channel hit.

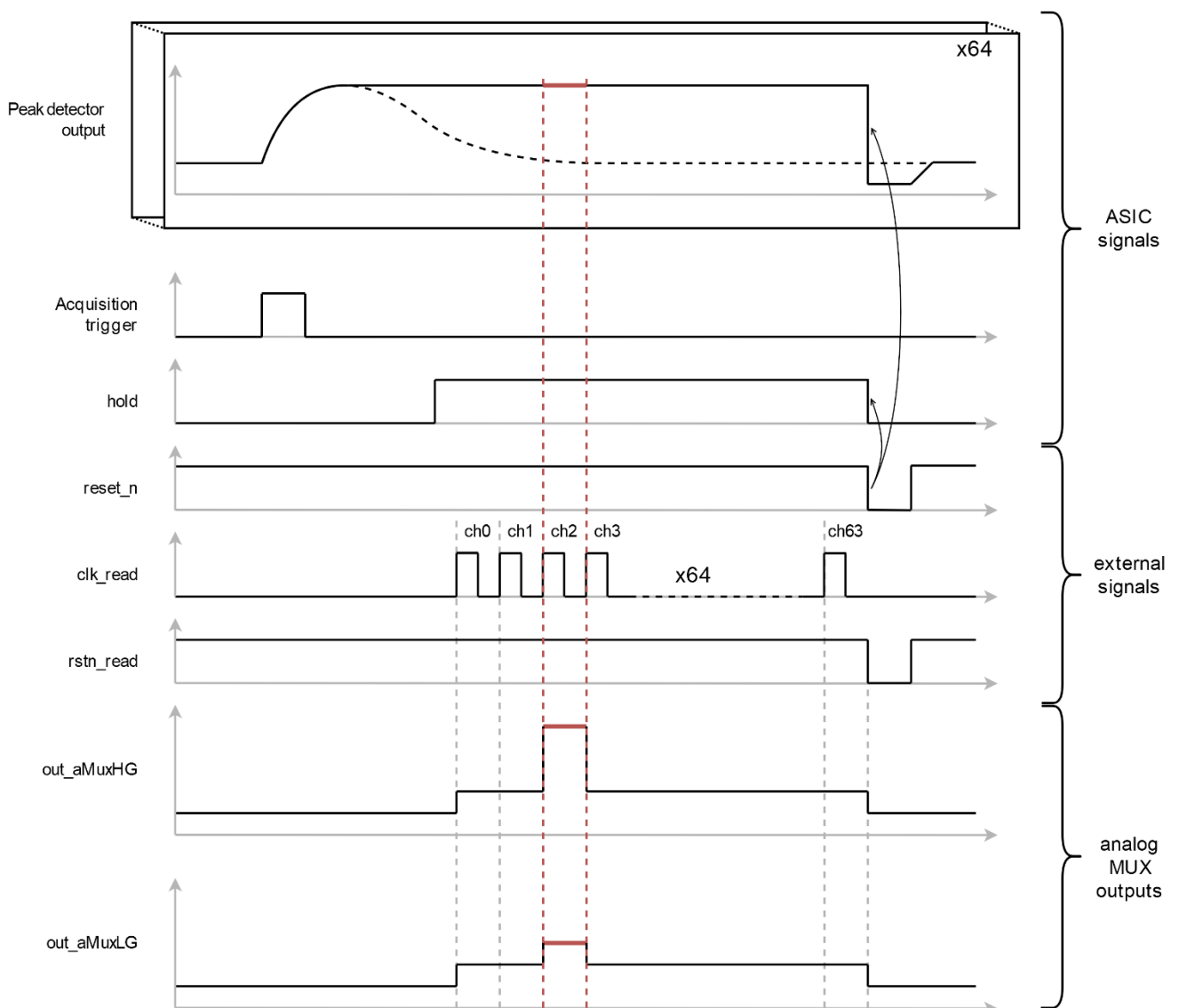


Figure 27 - Example 1 DAQ timing diagram.

Example 2: Charge measurement with custom topological trigger

On example 2 it is assumed that the user wants to trigger an acquisition when 2 or more channels are hit under a 1 ns period. An FPGA is used to implement the trigger logic so when the channels 1 and 2 are hit the pin TRIGEXT (AC11) is asserted by the FPGA. The slow control parameter *selTrig* is set to "0000" to use the TRIGEXT pin as the acquisition trigger. The outing can be set to either output LVDS T1 (*lvdsOut* = "01") or a single ended T1 (*lvdsOut* = "00" and *outPad1* or *outPad2* = "00"). The external trigger starts the delay box and after a given time the user can start the read-out procedure similarly to example 1.

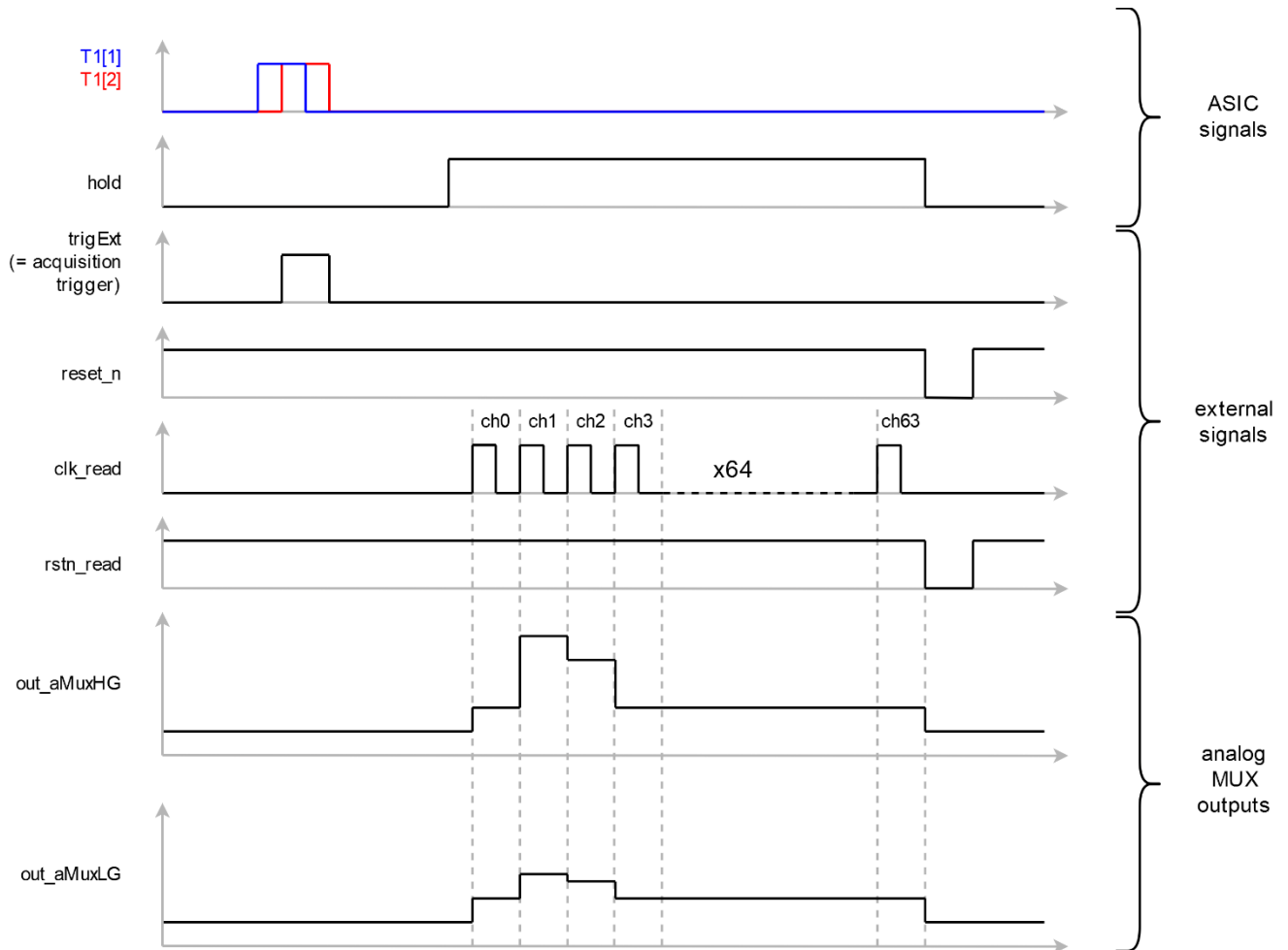


Figure 28 - Example 2 DAQ timing diagram.

Example 3: Photocounting

To maximize the photocounting rate the differential trigger output must be used. Triggers T1 or T2 can be used indiscriminately (*lvdsOut* = "00" with T1 or "01" with T2). The charge measurement blocks can be switched off for power consumption considerations by setting to '0' the following SC bits:

- address 64; subadd 13; bit 4-0 (*ON_paHG*, *ON_paLG*, *ON_shHG*, *ON_shLG*, *ON_pdetector*)
- address 64; subadd 14; bit 3-2 (*ON_discrCharge*, *ON_pdBuffer*)
- address 65; subadd 7; bit 1 (*EN_th0*)
- address 65; subadd 12; bit 5 (*EN_delay*)
- address 66; subadd 70; bit 4-3 (*ON_outing*, *ON_aBuffer*)

One external counter per channel must be implemented.



Datasheet version history

| Version | Date | Information |
|---------|------------|--------------------------------------------------------------------------------|
| 1.0 | 21/01/2021 | Initial release |
| 1.1 | 04/02/2021 | Added info & figure corrections |
| 1.3 | 20/12/2021 | Updated first page based on measurement results |
| 1.4 | 21/8/2023 | Correction table in "Outing selection" section concerning CLPS signal polarity |
| 1.5 | 27/03/2024 | Updated I ² C section |