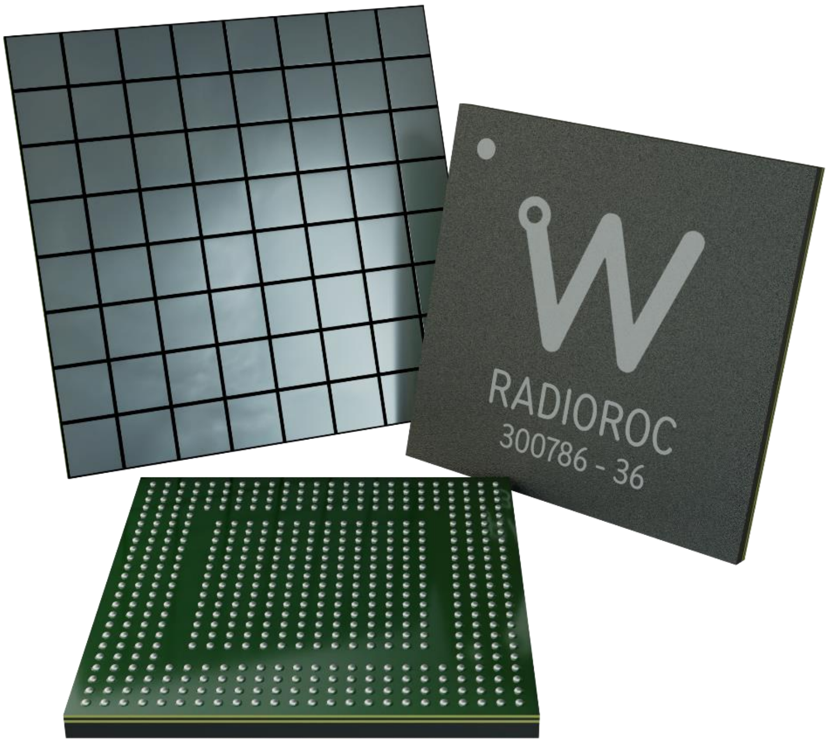
RADIOROC

SOFTWARE & TEST BOARD USER GUIDE

Version: 16 May 2025

RADIOROC is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM). RADIOROC allows triggering down to 1/3 p.e. and provides dual-gain energy measurement with excellent Signal-to-noise ratio on the high gain (SNR over 10 for single p.e.) and large dynamic range on the low gain

This guide explains how to install and use the test board for RADIOROC and how to operate with the associated software.



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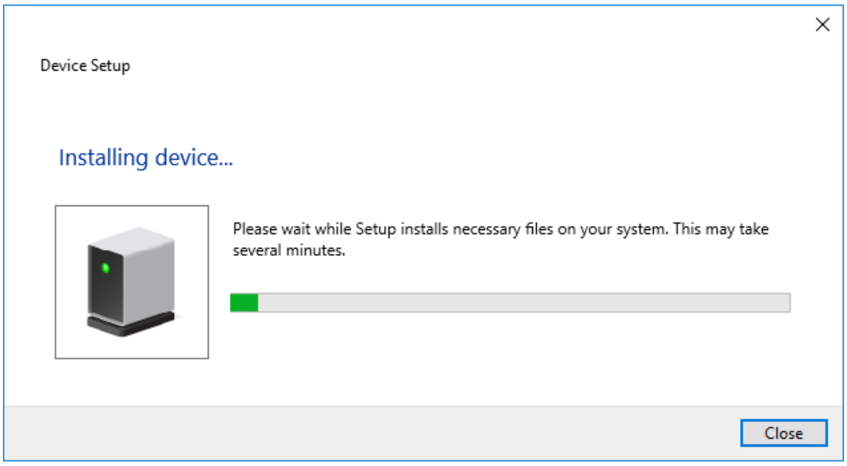
1 Installation & Test of the Test Board

1.1 Pre requisites

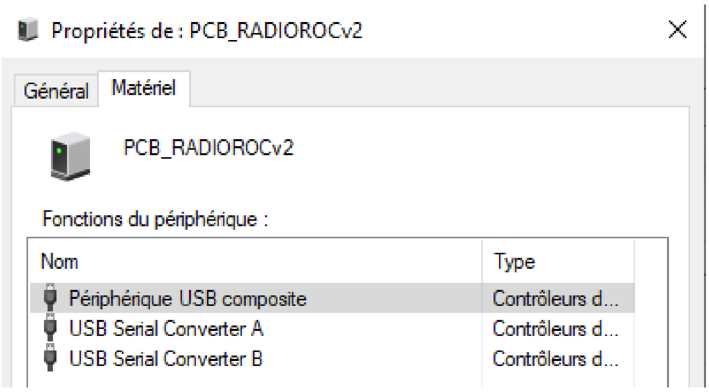
The use of this evaluation board requires:

- A computer (Microsoft Windows 10 or later) with USB connection
- A USB-A to mini-USB cable
- A positive output power supply (delivering 5V - 1A)

The first time a Weeroc testboard is plugged, the following message should prompt.



In order to verify that the drivers are correctly installed, go to the control panel under the "Devices and Printers" window. the PCB_RADIOROCv2 device should appear as follow:



1.2 Installation guide

Before running the software for the first time, please verify that the PCB is correctly identified in the "Devices and Printers" window under the control panel. The latest release of the RADIOROC user interface can be found in the Weeroc download center on the website http://www.weeroc.com. If assistance is required, please contact the Weeroc support by sending an e-mail at support@weeroc.com.

2 Evaluation board description

The evaluation board has mainly been developed to allow characterization and debug of the RADIOROC ASIC. Some features were added on the board or in the firmware/software to allow versatility and its use with real detectors or within an experiment. The schematics of the evaluation board, the firmware and software sources can be provided, users can modify anything they need to fit their own requirements.

- This board provides easy access to each RADIOROC pin, as all analog pins are connected to through-hole test points and as all digitals I/Os are connected to probes between the ASIC and the FPGA.
- Many test points are also connected to the FPGA, outputting digital signals.
- 1 analogue buffer provides ASIC's analogue probe output on an SMA connectors (Analog_Probe).
- The board needs to be externally powered by a 5V/1A supply.
- This board can be used with a SiPM board that is connected through the HSEC6-042-01-S-DV-WT-TR.
    - Schematic available on the website

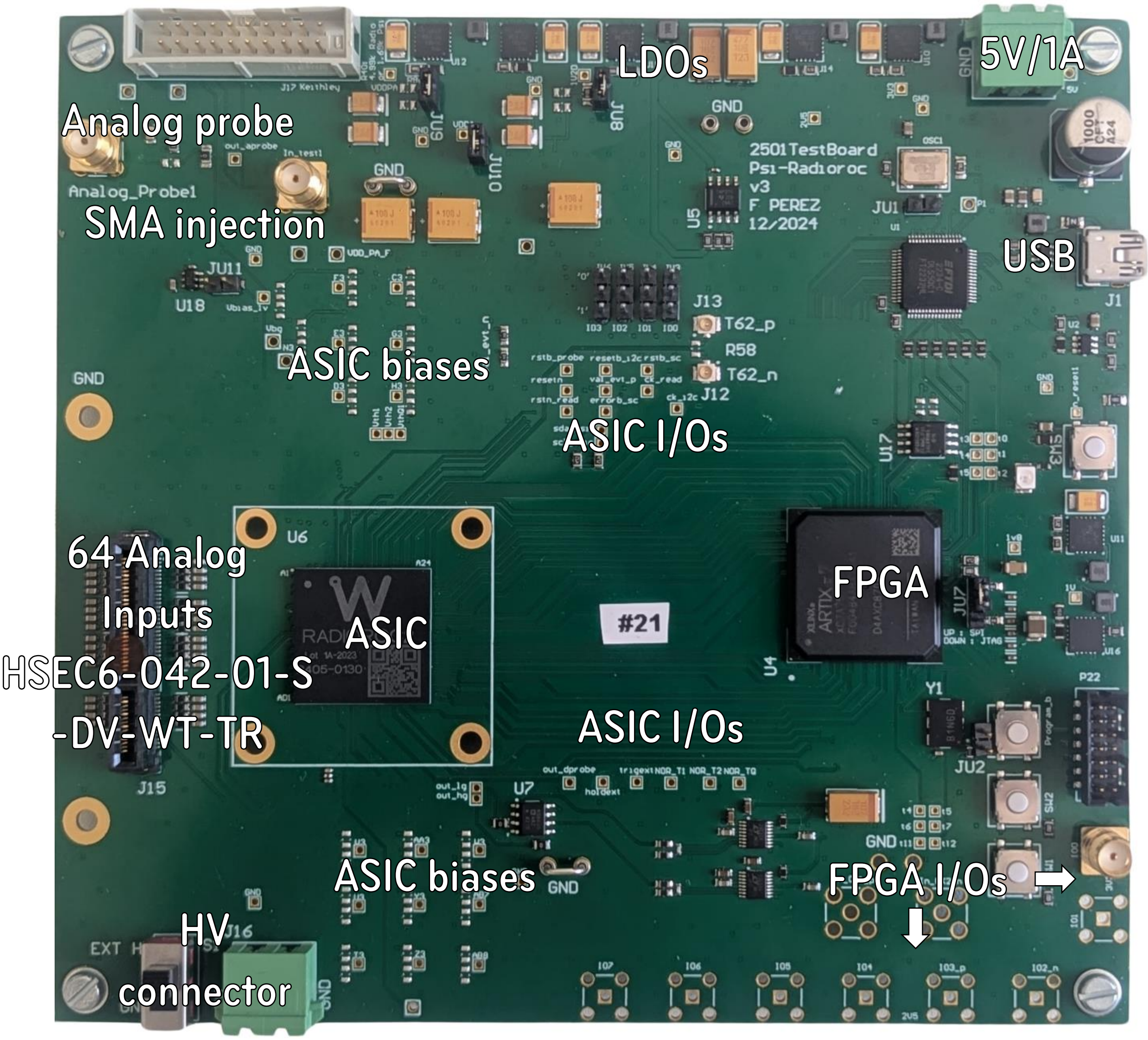


Figure 1– RADIOROC evaluation board.

3 User Interface description

The software has been written in python language. The source code is available on demand in order to help users to comprehend the functionality of the software. This is especially useful if users aim to develop their own data acquisition (DAQ) system.

To start the evaluation board, users need to:

1. Connect the USB cable from the evaluation board to your computer.
2. Provide power supply to the evaluation board (top-right connector) using an external power supply (5V/1A).
3. Start the software and click on the round button in the bottom left

When connecting the evaluation board, drivers for the USB device should install automatically. If it is not the case, the drivers can be found on the FTDI website (http://www.ftdichip.com/Drivers/D2XX.htm).

When the software is started, the user should be prompted by the following screen.

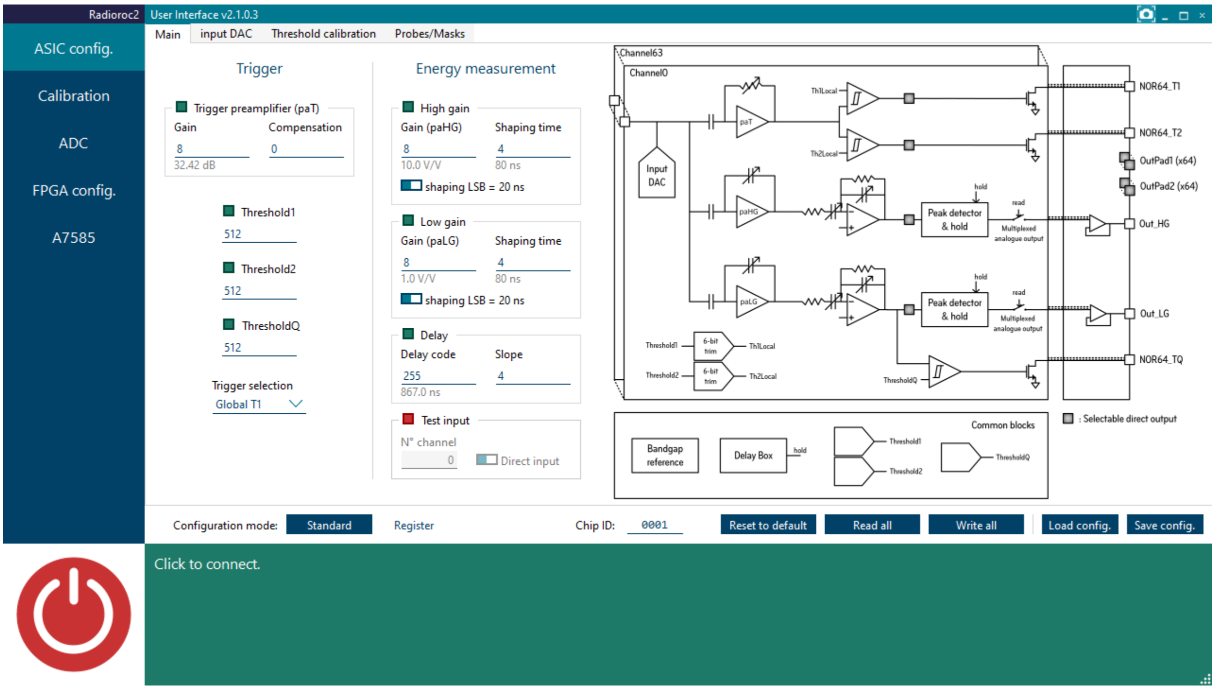


Figure 2 – Software main page.

When the software is running and the button clicked, no error should occur, meaning that the installation has been done successfully and all the drivers have been found.

While this user guide will help the user with the software and evaluation board, it should be noted that there is an embedded help in the software. By hovering controls with the mouse, the bottom part will be filled with information on the object being hovered.

The firmware version is automatically detected by the software and is written to the interface. The expected firmware version should correspond to the last number in the software version. The latest firmware version is 3, while the software version is 2.1.0.3.

If the evaluation board is plugged and powered, the USB connection is automatically performed and the prompted screen would be as shown on Figure 3.

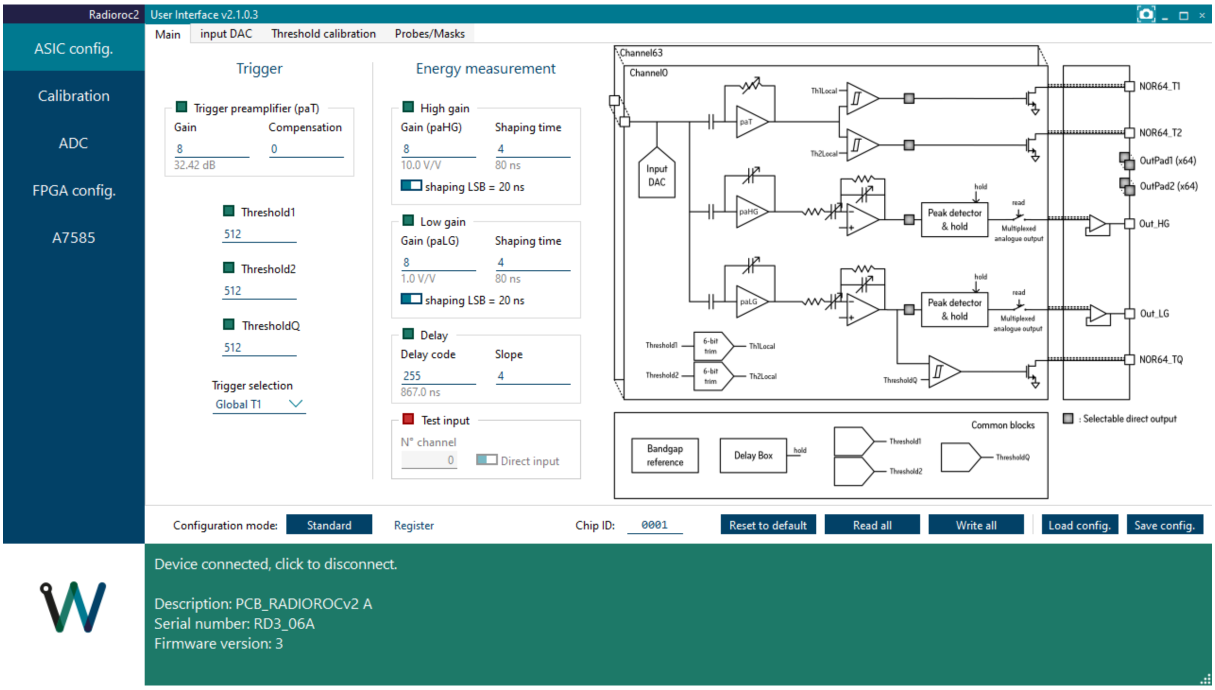


Figure 3 – Connection status

The button becomes the Weeroc logo and information about the board are displayed in the embedded help. To show that information at any moment, just hover the Weeroc logo in the lower left screen.

3.1 ASIC configuration (Commonly referred to as slow control/I²C configuration)

The home page of the software is the ASIC configuration tab. In this tab users can modify the ASIC parameters to adjust its behavior to their needs (pre-amplifier gain, shapers shaping time, trigger threshold, etc.). The embedded help is particularly handy here because the description of parameters is given to the user when hovering the corresponding control as shown on Figure 4.

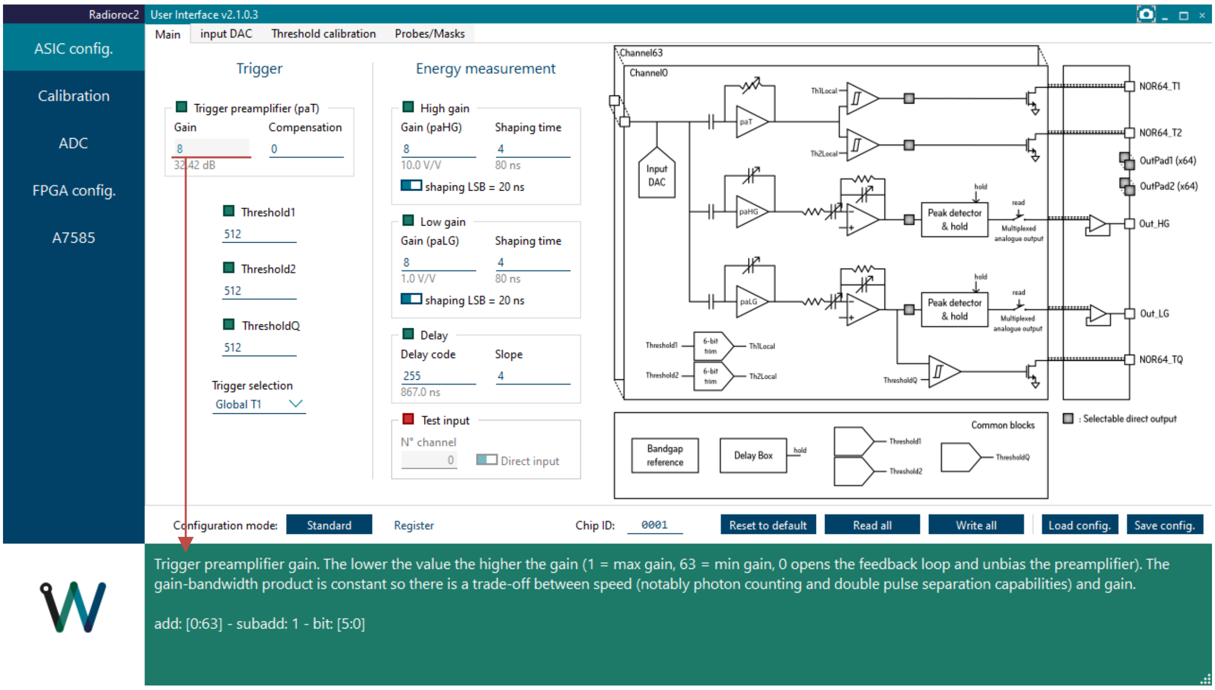


Figure 4 – Embedded help for ASIC configuration.

On the left side of the Main page the parameters are organized between "Trigger" and "Energy measurement" and on the right side the schematic of the ASIC is displayed for quick reference. More specific parameters can be found on other tabs for calibration purposes or signal probing for instance.

ASIC configurations can be saved and loaded back using the "Load config." And "Save config." Buttons in the bottom right. Alternatively, the configuration files can be drag and dropped in the UI. To quickly reset the I^{2}C registers to their default state the user can click the "Reset to default" button without having to manually load the default configuration file.

The "Read all" and "Write all" are here for debug purposes as in nominal operations the displayed I^{2}C should always match the ASIC registers. The parameters are sent to the ASIC and read back for validation at each interaction (If the board is plugged and powered).

TextBox being edited:

TextBox after validation (Enter/Return pressed or TextBox lost focus):

The displayed data is the one read back from the ASIC, not the one inputted by the user, although they should match. It shall be noted that while the board isn't connected the configuration can be edited freely and the edited configuration will be loaded in the ASIC when connecting the board.

There are two configuration modes, either the "Standard" one where only the most relevant parameters are exposed to the user and layout in a user-friendly way, or the "Register" mode where the user can modify directly the binary content of every

I^2C register in the ASIC. To switch from one to the other the user has to click the bottom left buttons on the tab. In this mode the embedded help shows the content of the data in the register.

3.1.1 Main parameters

The standard mode slow control page brings together many ASIC parameters. Gain and compensation can be changed for the trigger preamplifier. Changing the preamplifier gain will result in changing the bandwidth of the preamplifier (the gain-bandwidth product is a constant). Compensation can be added using a 2 bits control.

- Gain (6-bit): Range: 41dB- 24.8dB
- Compensation (2-bit): Capacitance Range = 50 fF - 150 fF, Step = Compensation Value * 50fF

The DC level of the preamplifier is about 490mV (with default setting) and the output signal will be fed directly into a discriminator. In order to modify the trigger threshold, 10-bit DACs are used as a common threshold for both discriminators (2 DACs, generating the Threshold1 and Threshold2). Low Gain Shaper output signal is fed to a discriminator to generate a "charge" trigger which will be the highest threshold trigger relative to the input signal.

- Threshold1, Threshold2 (10-bit) Voltage span: 270mV ~ 530mV. Step = 0.25mV * DAC value.
- ThresholdQ (10-bit) Voltage span: 75 mV ~ 1,1 V. Step = 1 mV * DAC value

Peak detectors are used to sample the amplitude of the shaper signal. An acquisition trigger is generated to start the DAQ and this trigger can be selected through the following options:

- Local Low Threshold Time Trigger T1
- Local High Threshold Time Trigger T2
- Local Charge Trigger
- Global Low Threshold Time Trigger T1
- Global Low Threshold Time Trigger T2
- Global Charge Trigger
- Trigger External

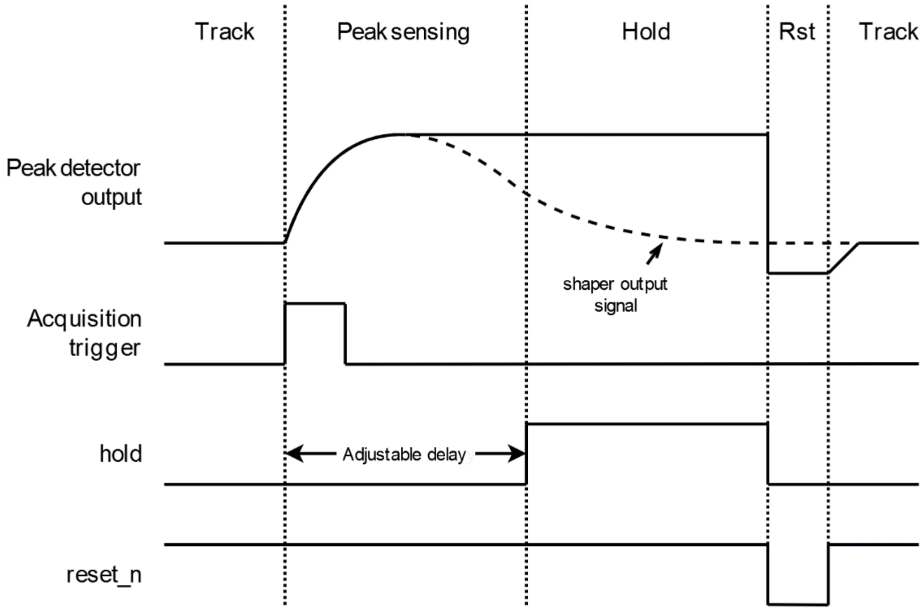


Figure 5 - Illustration of peak detection in RADIOROC.

Gain for both preamplifiers of the shapers can be adjusted using 4-bits parameters:

- Low Gain (4-bit). Gain span: 5 (1) ~ 80 (15).
- High Gain (4-bit). Gain span: 0,5 (1) ~ 8 (15).

Shaping time for both shapers can be adjusted using these parameters:

- Shaping Time High Gain (4-bits): Shaping time span: 20 ns ~300 ns. Step = 20 ns * Shaping Time Value
- Shaping Time Low Gain (4-bits): Shaping time span: 20 ns ~300 ns. Step = 20 ns * Shaping Time Value

Additionally, a delay cell is used to generate the "hold" signal (delay started by the acquisition trigger) latching the output value of the peak detector before sending it to the analog multiplexer output. This delay can be configured using this option:

- Delay(8-bit): Delay span: 2 ns~2.6 µs. Step size depends on Delay Slope Trimming
- Delay Slope Trimming (4-bit): Range = 60 ns (0) - 2.6 µs (15).

It is possible to toggle the hold signal by using the external pin (AC9, Active high) instead of relying on the internal delay box.

It is possible to enable the test input for a specified channel. Using the "direct input" option, the in_test pin is directly tied to the target channel input pin, meaning that the injected signal will be seen on the corresponding input pin. Using the "use Ctest" option, the input signal will be sent through a 1.5 pF injection capacitor.

3.1.2 Input DAC

The input DAC tab allows users to tune the DC value of the ASIC inputs. When using RADIOROC with SiPM arrays, the input DAC provides the possibility to the user of correcting pixel gain dispersion by adjusting individually the high voltage biasing of each input channel. The number next to the textbox corresponds to the channel number. These channels may differ from the SiPM channel number allocation.

Input DAC DC value can be roughly calculated using the following equation:

Input DAC range = 50mV ~ 600mV, Step ~2mV * Input DAC Value.

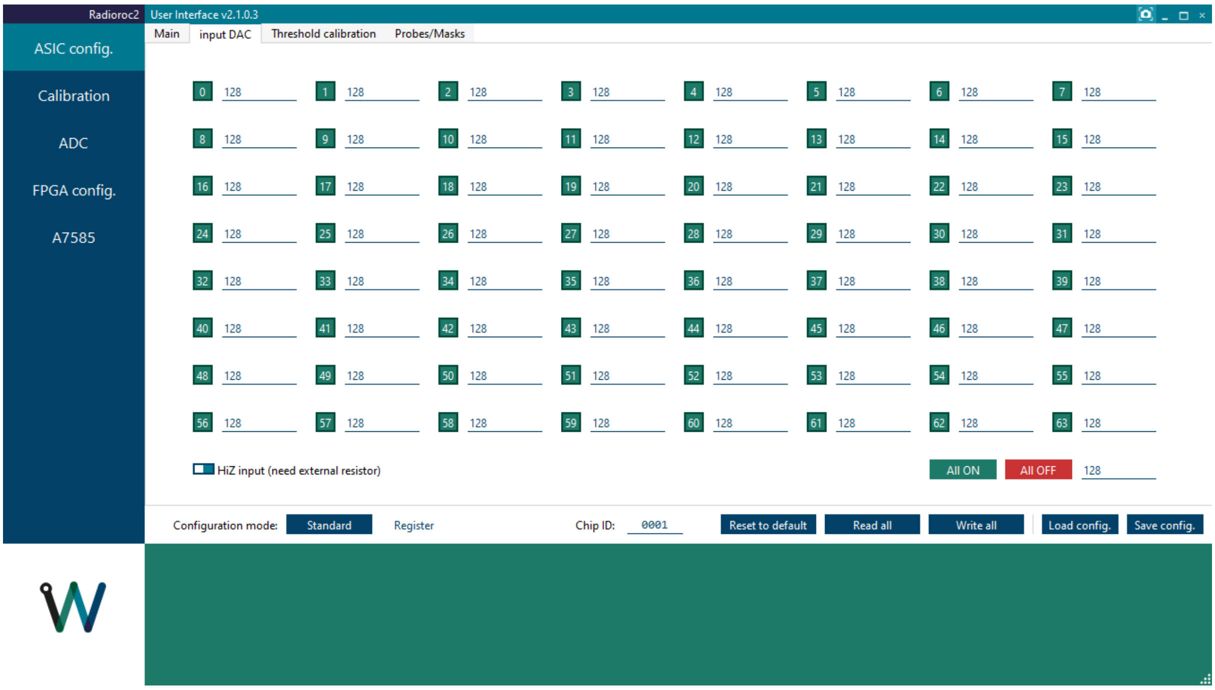


Figure 6 – Slow control standard mode – input DAC

Input DACs can be disabled channel by channel. They can be toggled between high impedance and low impedance (~150 Ohm) input through the switch at the bottom-left of the tab. Note that the embedded 150 Ohm impedance is intended to be used when there are no 50 Ohm termination on the inputs.

3.1.3 Threshold calibration

Since the discriminator thresholds 1&2 are common to all channels and there are DC dispersion from channel to channel because of manufacturing mismatches, 6-bit adjustment DACs have been added in each channel to align local thresholds. Threshold calibration can be automatically performed using the Calibration → S-curves → autocalibration button. The calibration values will be automatically filled after the calibration process is done.

Result of such calibration process can be seen on Figure 8.

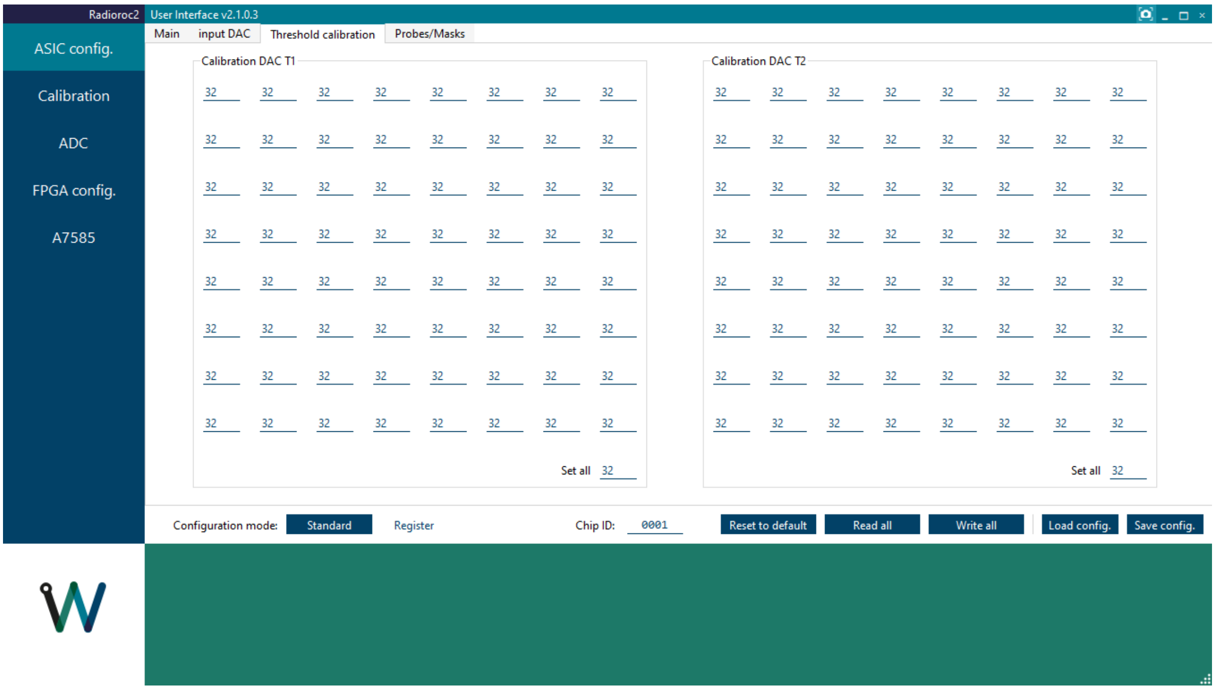


Figure 7 – Slow control standard mode – Threshold calibration

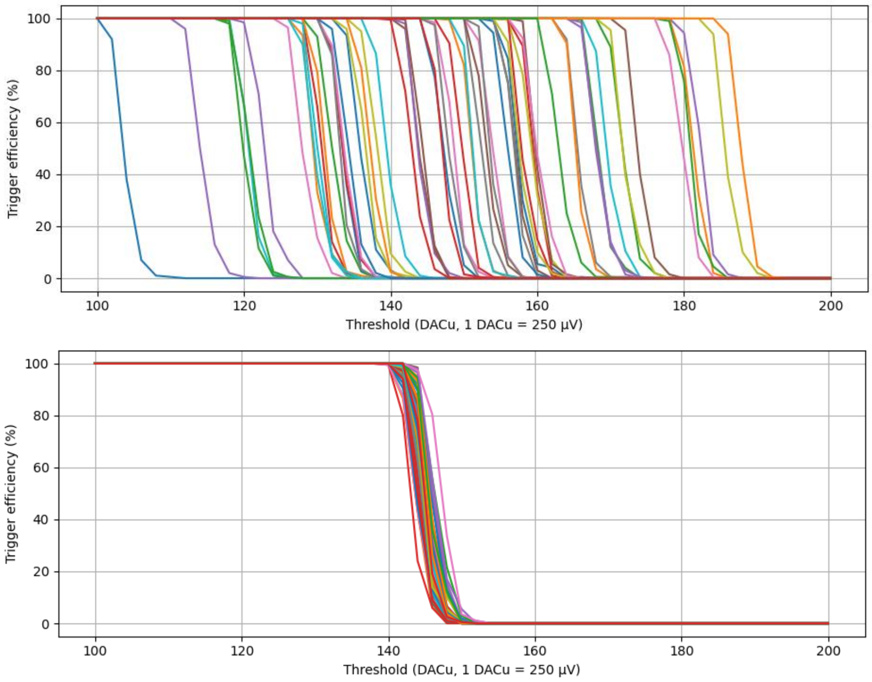


Figure 8 – S-curves before and after autocalibration.

3.1.4 Probes/Mask

This tab allows to mask/unmask channel-wise triggers for T1, T2 and TQ.

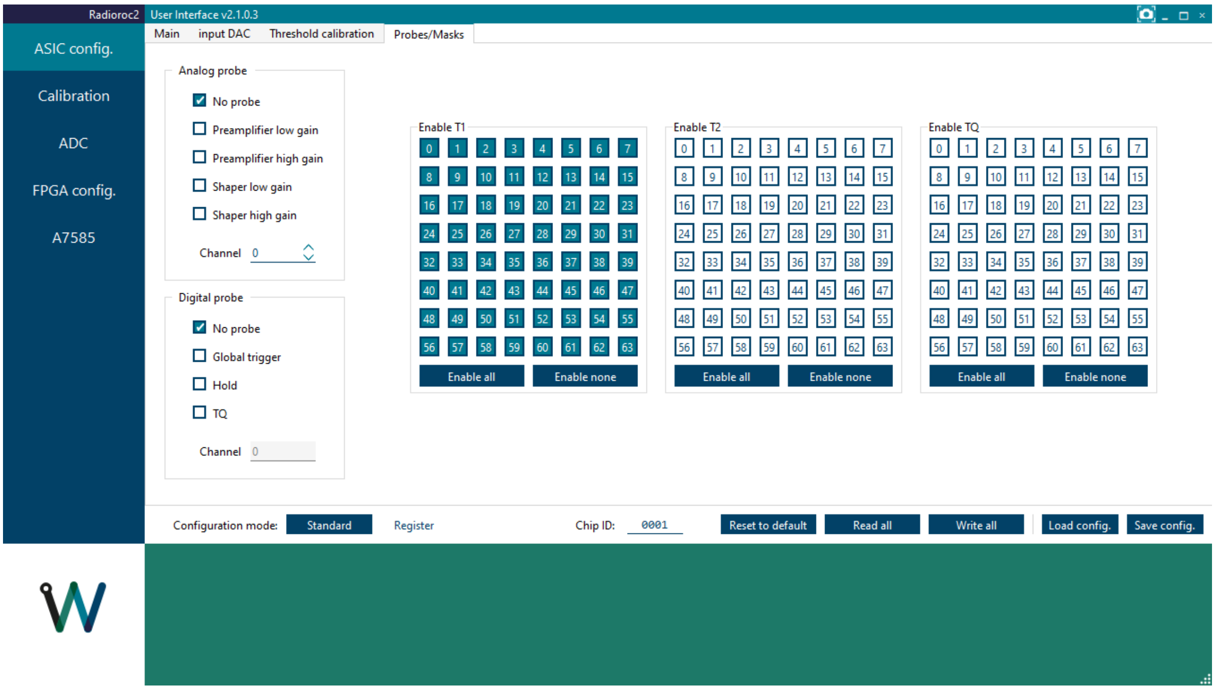


Figure 9 – Slow control standard mode – Mask

An internal ASIC probing multiplexer allows to monitor each channel pre-amp and shaper output signals and to display them on the oscilloscope. User can choose to monitor the output of the low gain and high gain preamplifier output as well as the low gain and high gain shaper output for a specified channel.

In typical ASIC operation, it is advised to turn off the probe register ("No probe" checked) to avoid performance degradation.

3.1.5 Register mode

By toggling the "Configuration Mode" switch in the bottom-left corner, the interface will change into "Register Mode" where each I^{2}C register is directly accessible. The large textbox on the right displays the hexadecimal values of all the registers in the ASIC. On the right side of the register tab the full register content is displayed by address number in a compact hexadecimal way. Sub-addresses are organized by ascending order from left to right e.g. for address 0:

```
add 00: 80 08 88 44 17 20 f3 0f 00
```

The sub-addresses (refer to datasheet for sub-adresses values) and their respective data are:

- 0 : 0x80
- 1 : 0x08
- 2 : 0x88
- 3 : 0x44
- 4 : 0x17
- 5 : 0x20
- 6 : 0xf3
- 7 : 0x0f
- 66 : 0x00

The sub-address 66 isn't part of the editable textboxes because this register sub-address is reserved for probes and only one bit per probe (analog and digital) of all registers should be '1' to avoid contentions. Having '1' on more than one bit would connect together amplifiers outputs (analog probe) or buffer outputs (digital probe) in the ASIC. For probe operations it is recommended to use the dedicated tab in the standard configuration mode.

Refer to the datasheet for a description of the register parameters and addresses.

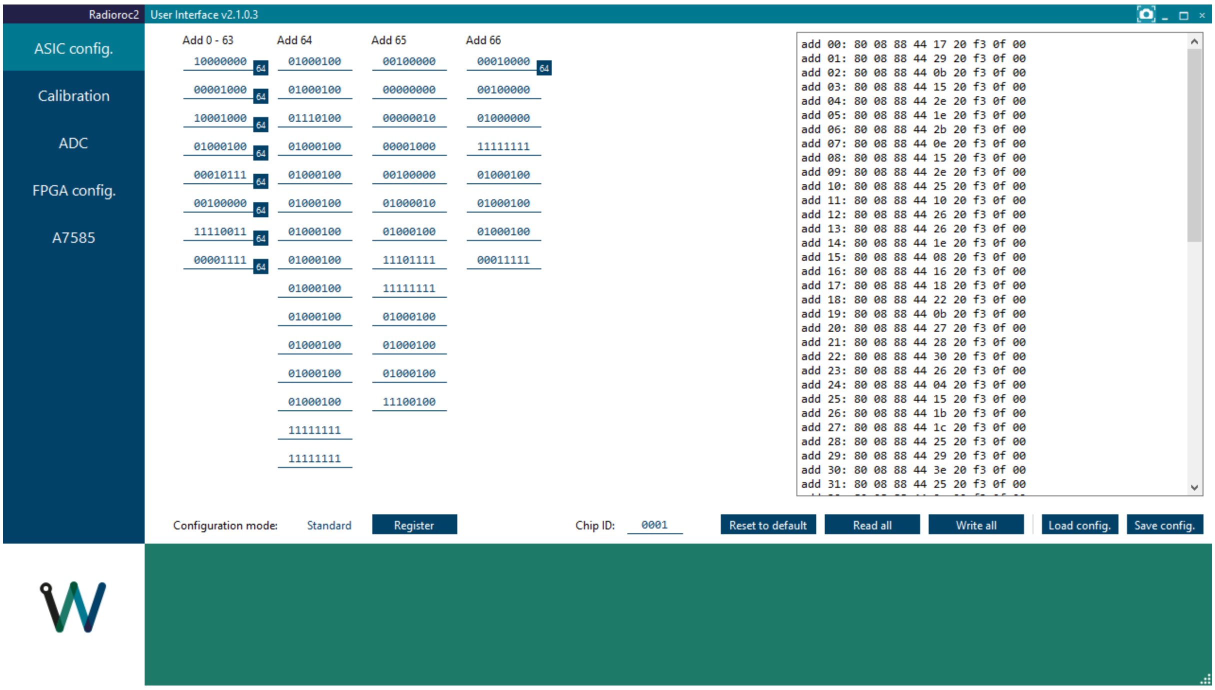


Figure 10 – Register Mode

3.2 Calibration page

3.2.1 S-curves

The first tab in this page is called "S-curves" and its purpose is to perform a trigger efficiency test (named S-curves). It is done by scanning through several values of threshold and measuring if a trigger happens. The acquisitions are windowed by a clock. If a trigger happens outside the clock window, it will not be taken into account.

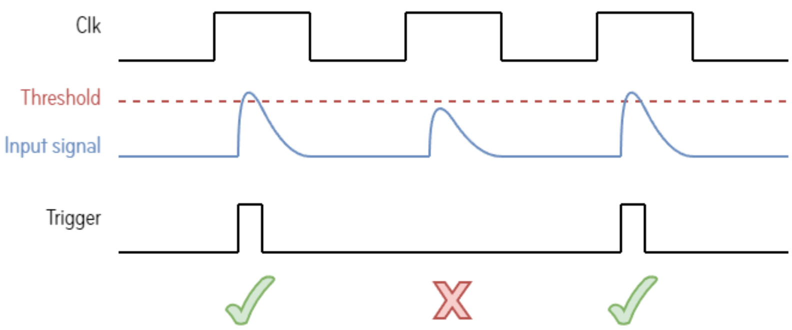


Figure 11 - S-curves acquisition chronogram

When the threshold is way below the signal amplitude, the trigger efficiency will be 100%. With a threshold way over the signal, trigger efficiency drops to 0%. On Figure 11, the threshold is set near the tip of the signal so the ASIC will have a

~50% chance of triggering depending on the noise. Following the Figure 11, the ASIC would trigger 2 times in 3 acquisition windows, resulting with a 67 % trigger efficiency.

The acquisition is started by clicking on the “start” button. With default settings it will give the result shown on Figure 12.

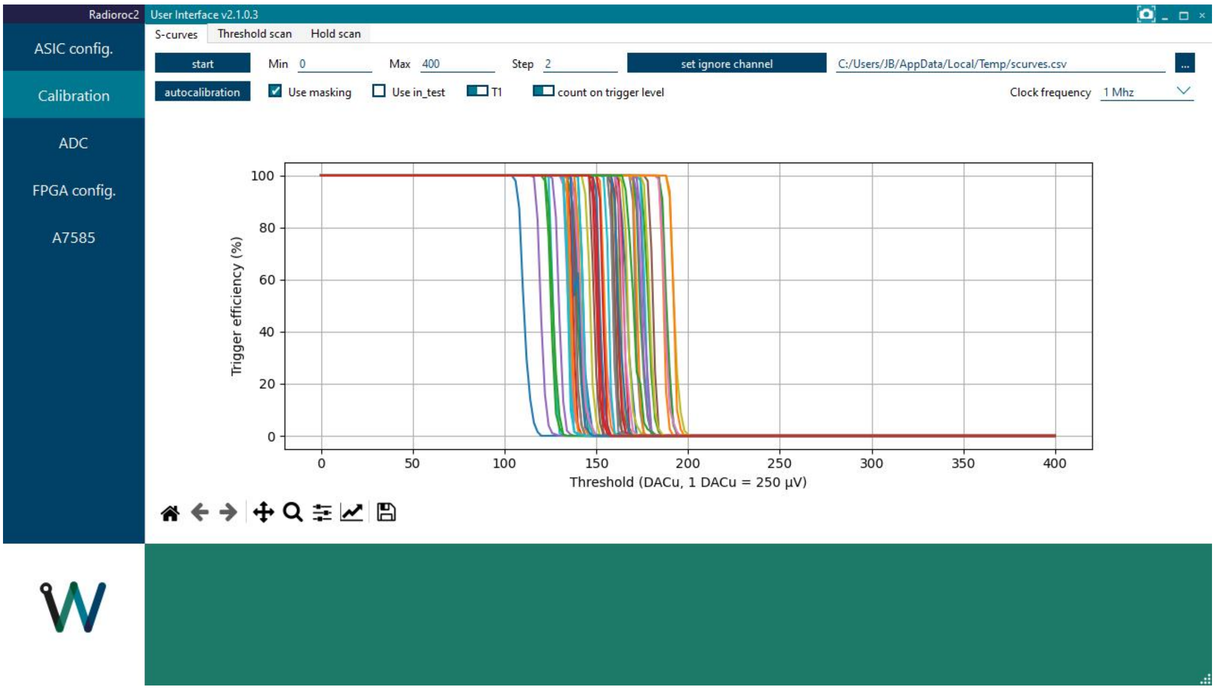


Figure 12 – S-curves tab.

Clicking on the autocalibration button will start an automated multi-step process threshold alignment. The alignment results will be written in the ASIC configuration → threshold calibration and sent to the ASIC via I^2C as explained in section 3.1.3.

There are 4 checkboxes that allow to adjust the behavior of the S-curves measurement as shown on Figure 13.

Figure 13 – Behaviour checkboxes for S-curves.

The S-curves measurement can be done on T1 or T2 by toggling the switchbox ③.

By default, all but the measured channel triggers are masked to avoid seeing the effect of crosstalk. This can be changed by unchecking the “Use masking” checkbox ①. Note that if doing this measurement on T2 the measurement will use the masking specified in the ASIC configuration that masks every channel by default so the user would have to modify the masks setup to see S-curves on T2 if “Use masking” is unchecked.

To plot the S-curves on a signal checking the “use in_test” checkbox ② the user will need to inject signal through the “in_test” connector. The injected signal must be synchronized with the clock signal available on the FPGA I/Os (default IO0, see FPGA config. tab) to send the signal in each acquisition window as shown on Figure 11.

Finally, checkbox ④ allows to perform the measurement on trigger level or trigger edge. The difference is only visible when below the pedestal. If the measurement is done on trigger level the trigger efficiency will be 100 % when the threshold is below the pedestal. If done on trigger level the trigger efficiency will drop to 0 when the threshold is below pedestal. The difference is shown on Figure 14.

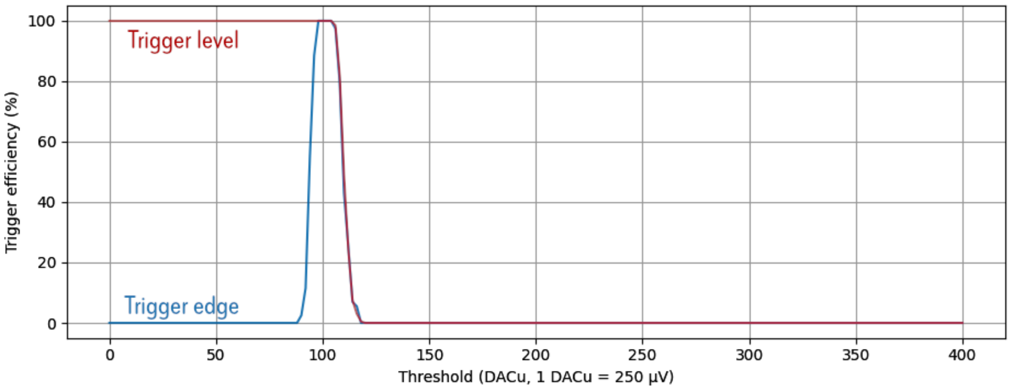


Figure 14 – S-curves on trigger level versus trigger edge.

The "Clock frequency" combo box allows to modify the clock frequency used for the S-curves measurement. Refer to the appendix on S-curves for more information about the effects of the clock frequency.

It is also possible to plot only chosen channels using "set ignore channel". Plotting the S-curve on a single channel will be 64 times faster than doing it on the 64 channels because each channel is measured sequentially.

3.2.1 Threshold scan

The threshold scan is similar to the S-curves measurement but here the total number of triggers happening in a time window is counted and the trigger frequency for each threshold value is calculated. This gives the trigger frequency as a function of the threshold value.

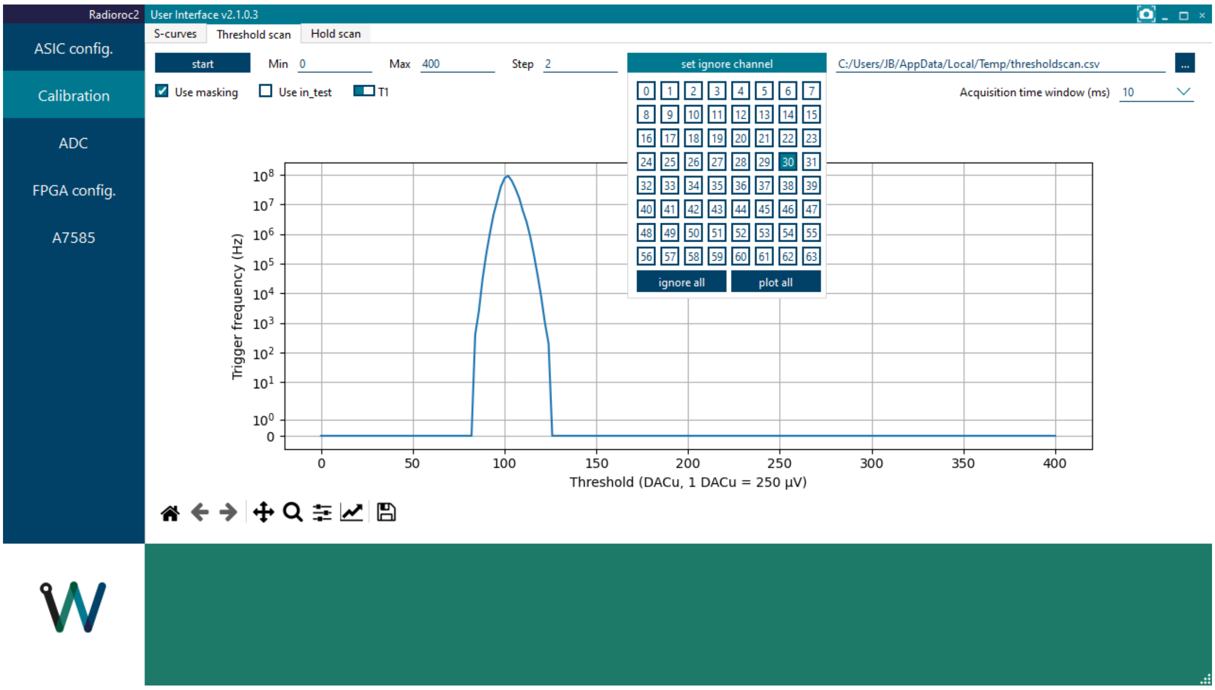


Figure 15 – Threshold scan of a single channel pedestal noise gaussian. Note that the gaussian appears pointy because of the discriminator hysteresis.

The checkboxes "Use masking", "Use in_test" and the switchbox T1/T2 behave the same as in the S-curves measurement. The acquisition time window can be modified, there is a trade-off between the acquisition duration and the data statistics (longer window = more statistics but longer measurement)

When injecting a signal, the user can observe the pedestal noise gaussian followed by a plateau of frequency equal to the input signal.

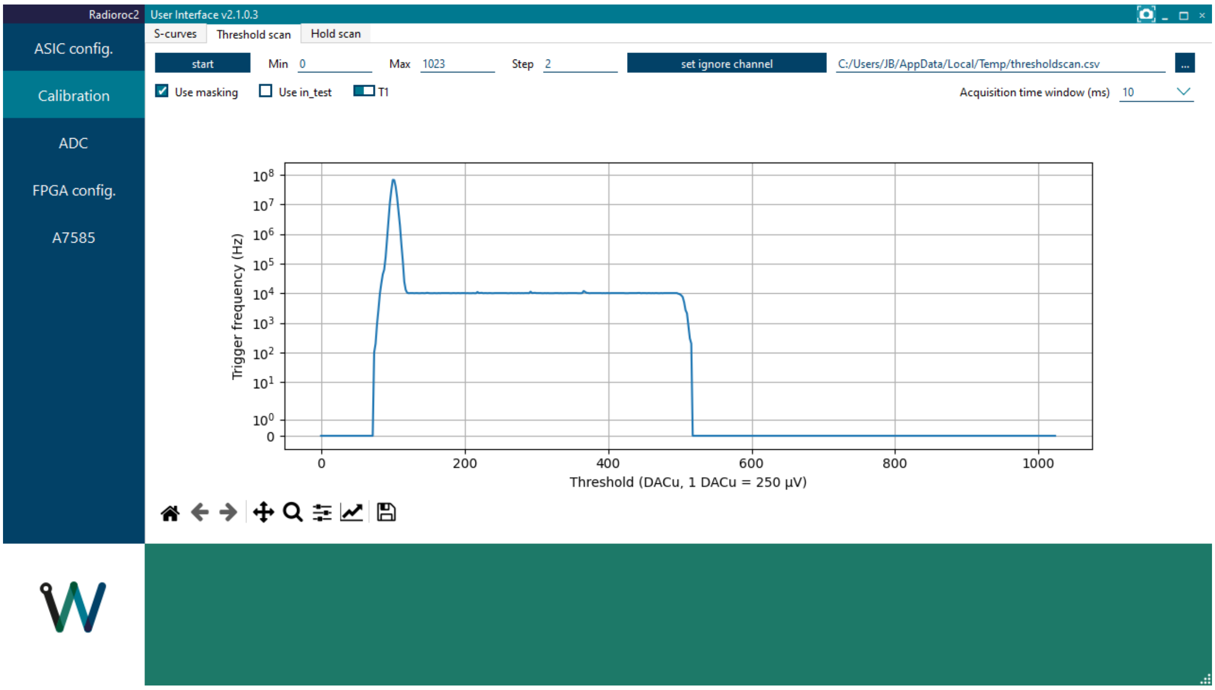


Figure 16 – Threshold scan with 10 kHz sawtooth signal injection.

The SiPM staircase measurement (see Figure 17) is performed with the threshold scan and is used to locate the pedestal and 1, 2, 3 photoelectrons position relative to the threshold DAC code. The SiPM must be plugged on the board and set in the dark with no parasitic light. A scan through the threshold DAC values will allow locating the pedestal and the first photoelectrons values thanks to the dark noise of the SiPM. Those values can be used to choose the threshold or to calibrate the gain of the 64 SiPM cells thanks to the input DACs.

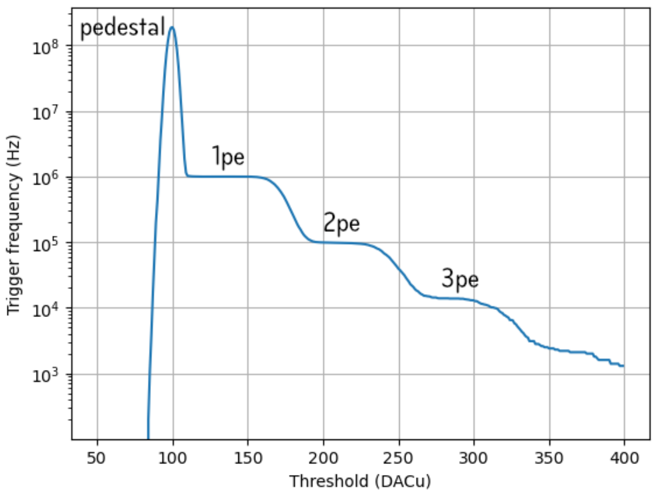


Figure 17 – Staircase plot.

3.2.2 Hold scan

Hold scan is a test done by sweeping through the hold delay value (delay between a trigger and the hold assertion). It can be done with the internal delay box to reconstruct the signal at peak detector output as seen by the DAQ (Figure 18) or with an external hold to avoid triggering the peak detector and reconstruct the shaper output signal (Figure 19). Note that the first values for the internal hold plot are too low and thus invalid hence why it gives incoherent results in peak sensing mode.

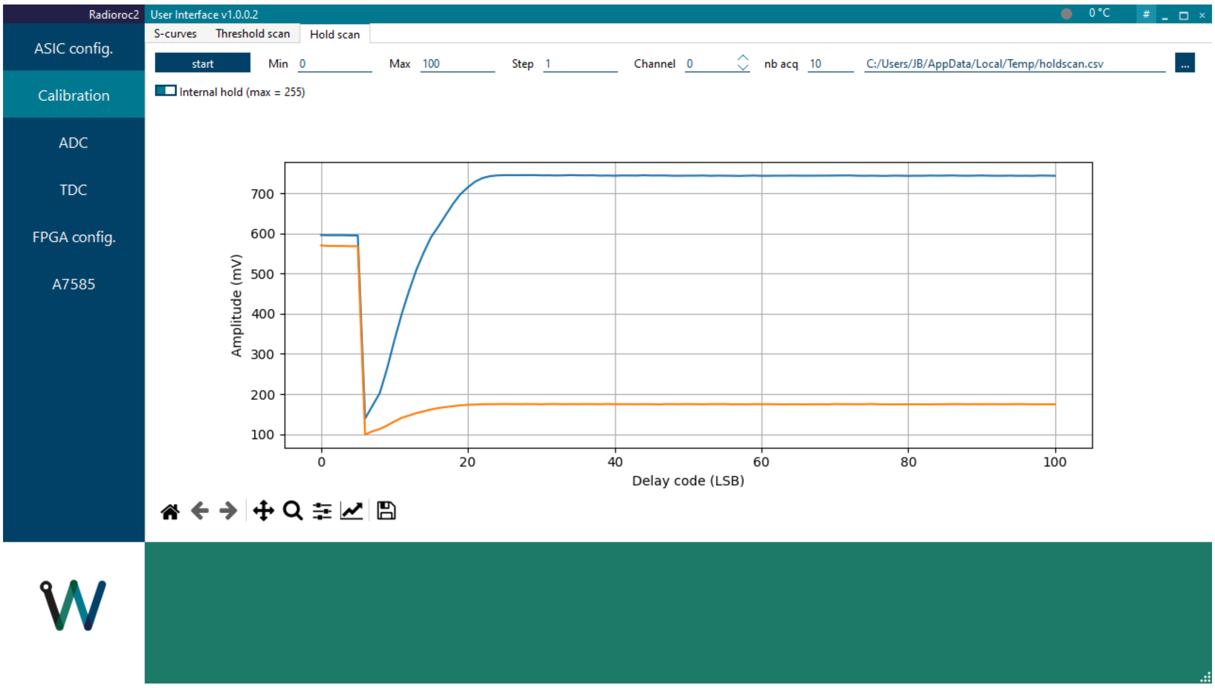


Figure 18 – Internal hold (using embedded delay cell and peak sensing)

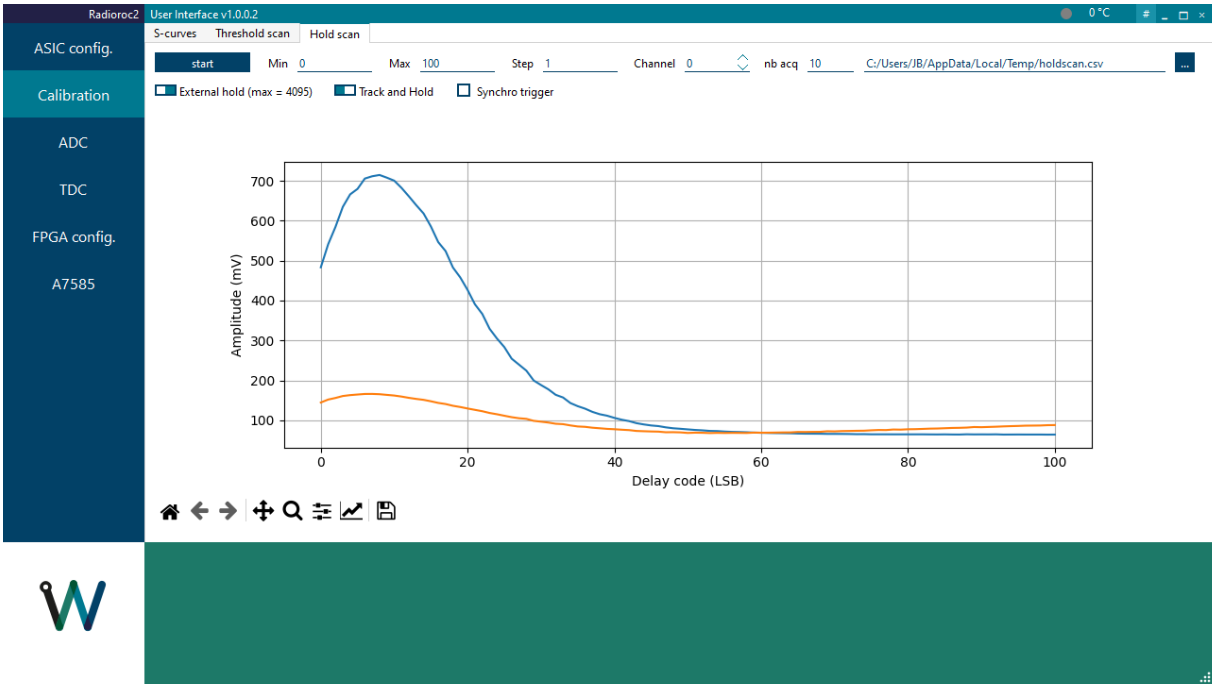


Figure 19 – External hold as track & hold.

The acquisition only starts after a trigger and this trigger signal has to go to the FPGA before the FPGA can send back the "hold" signal so the beginning of the signal is missing. It's possible to circumvent this to have the full signal by externally triggering the DAQ before the signal arrival. To do that the user will need to use the firmware "synchro trigger" signal available by default on IO1 and use this signal to trigger an external pulsed signal. Result can be seen on Figure 20 and Figure 21.

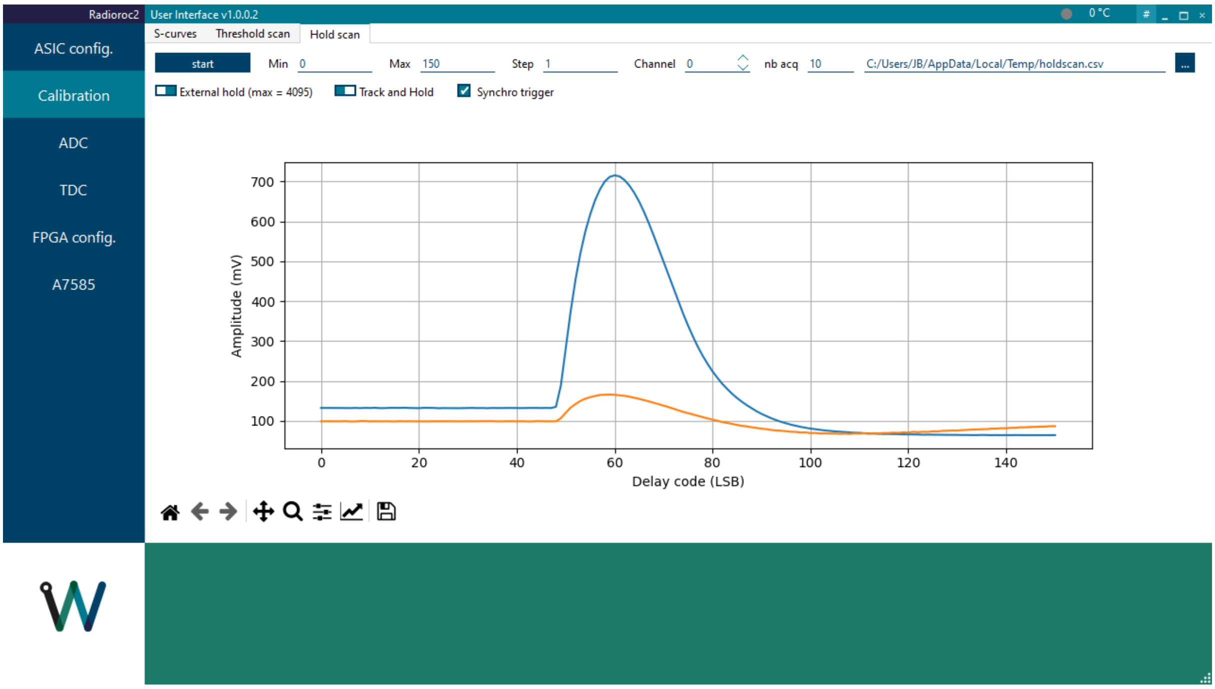


Figure 20 – Hold scan with synchro trigger in track & hold mode.

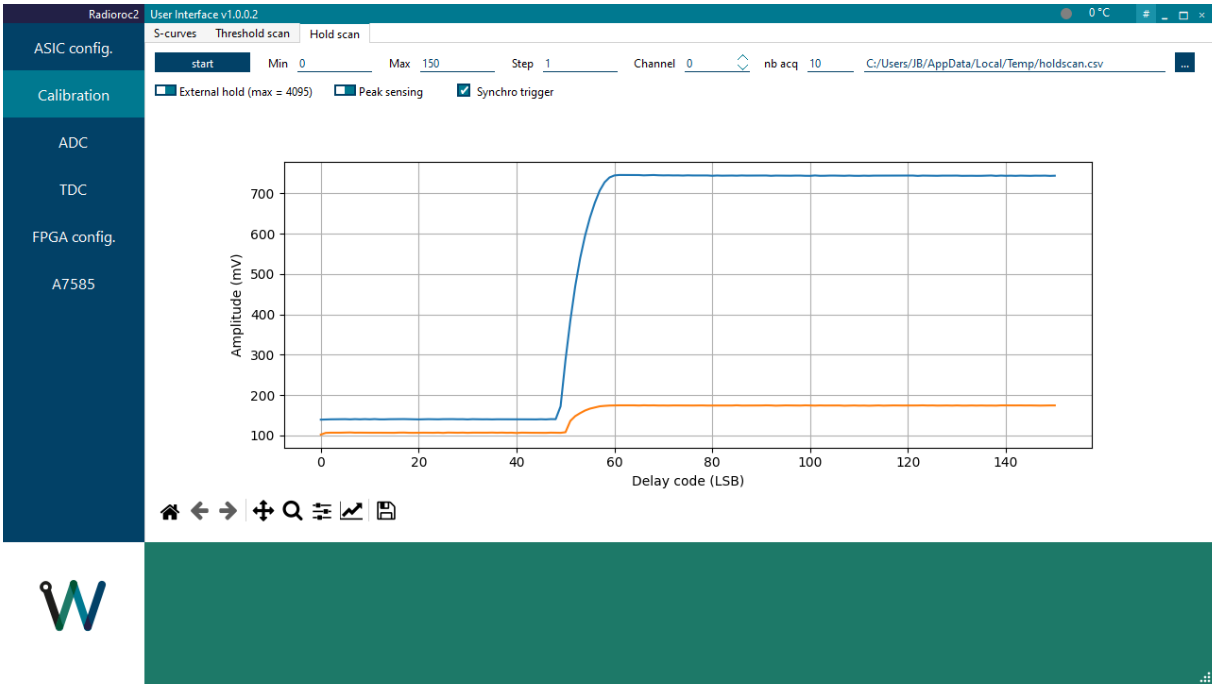


Figure 21 – Hold scan with synchro trigger in peak sensing mode.

This test is performed to find the ideal hold value for the delay. In the case of using the peak detector the hold must be superior to the peaking time of the signal. If the cell is used as a track and hold the hold must be chosen to be precisely the peaking time to sample the maximal value of the shaper output. When using the internal hold, the LSB shall be calculated using the slow control parameter of the delay slope (adjustable LSB). When using the external hold, the LSB is 5 ns.

3.3 Data acquisition

The ADC DAQ tab is prompted as shown on Figure 22. On the left panel of the setup tab, the DAQ trigger signal can be chosen to be a single trigger, a coincidence between two selected triggers, or a number of triggers in a time window (see Figure 23).

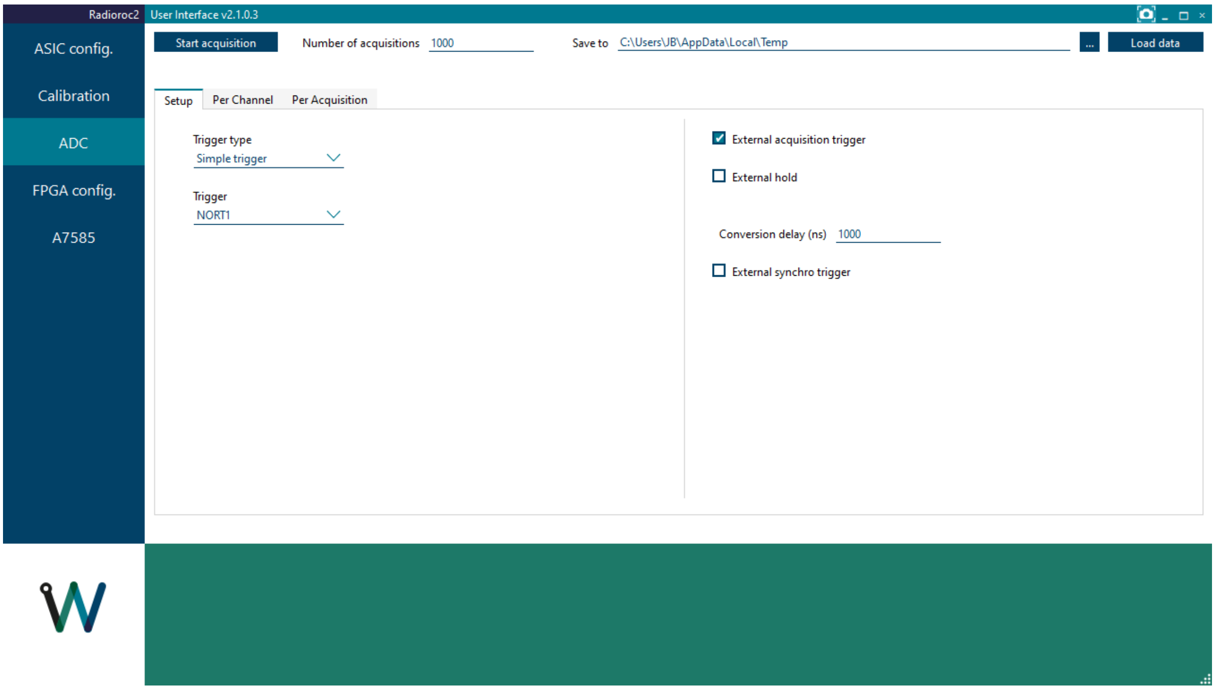


Figure 22 – ADC DAQ tab.

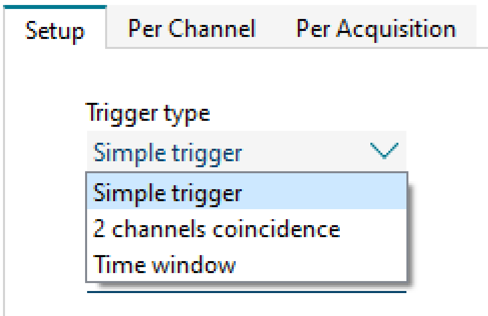


Figure 23 – Trigger type combo box.

In "Simple trigger" mode the trigger starting the DAQ can be of different types (see Figure 24).

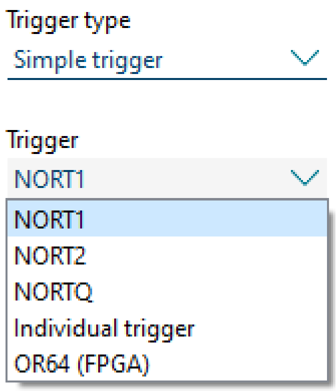


Figure 24 – Trigger used to start the DAQ.

Figure 25 shows a configuration for the trigger coincidence. Here the coincidence is set between channel 0 and channel 1 with a coincidence window of 5 ns.

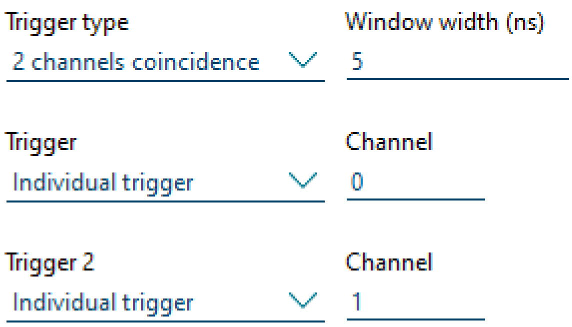


Figure 25 – Trigger coincidence example.

Figure 26 shows the default setting of the time window trigger. Here the DAQ is triggered by having N triggers in a given time window.

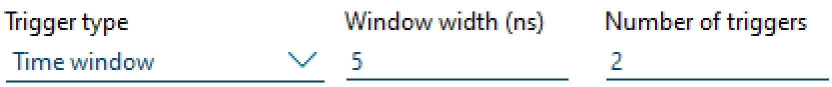


Figure 26 – Time window default settings.

On the right panel of the setup tab, some DAQ options are available to the user (see Figure 27). Here the user can choose to have the ASIC acquisition trigger set to internal or external. The hold signal for the peak detector can also be configured as either internal or external. The conversion delay is the time interval between the acquisition trigger and the ADC conversion—this corresponds to the delay between the acquisition trigger and conversion when using internal hold, or between the external hold signal and conversion when using external hold. When internal hold is selected, this delay must account for the ASIC's inherent internal delay (e.g., if the internal hold delay is 800 ns and the conversion delay is 100 ns, conversion will begin before the hold is asserted). The external synchro trigger is an external signal sent both to the ASIC and an FPGA I/O, and can be used to synchronize a pulser with the DAQ or to force triggers in the ASIC for pedestal acquisition. External Hold and External Synchro are respectively routed to SMA connectors IO_FPGA7 and IO_FPGA6, allowing the DAQ to be controlled via a 2.5V TTL signal.

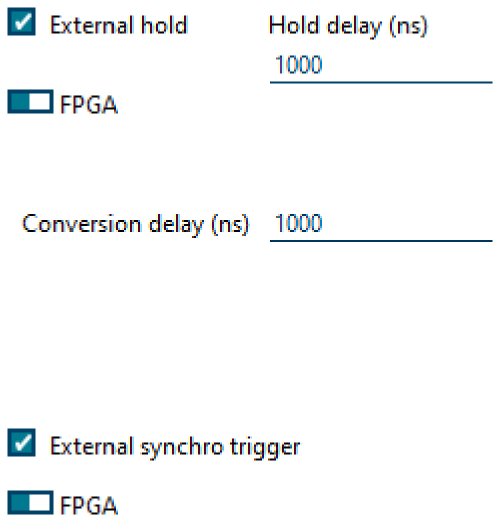


Figure 27 – Acquisition behavior options.

The following acquisitions have been performed by injecting in channel 30 using the SMA connector through a 10 pF injection capacitance (soldered by default on the PCB bottom layer) a 50 mV sawtooth pulse (500mV positive step, 20 dB attenuation → 50 mV × 10 pF = 500 fC) with the default DAQ setup and default ASIC configuration.

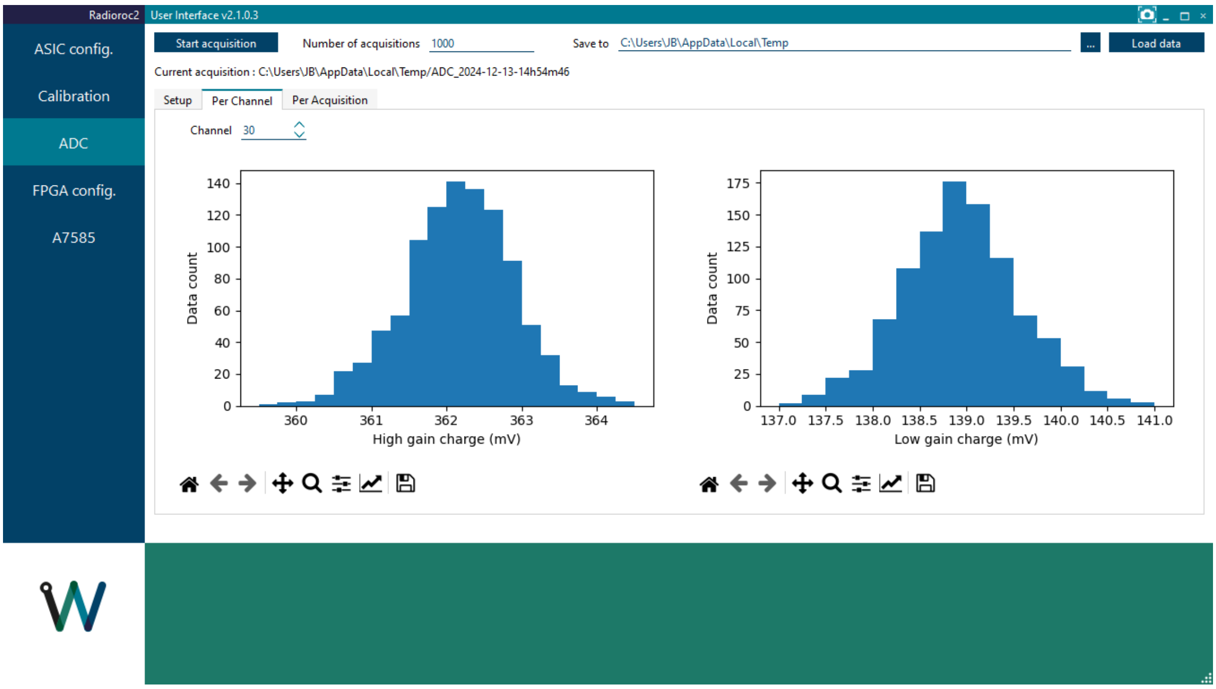


Figure 28 – DAQ result per channel (charge spectrum histogram).

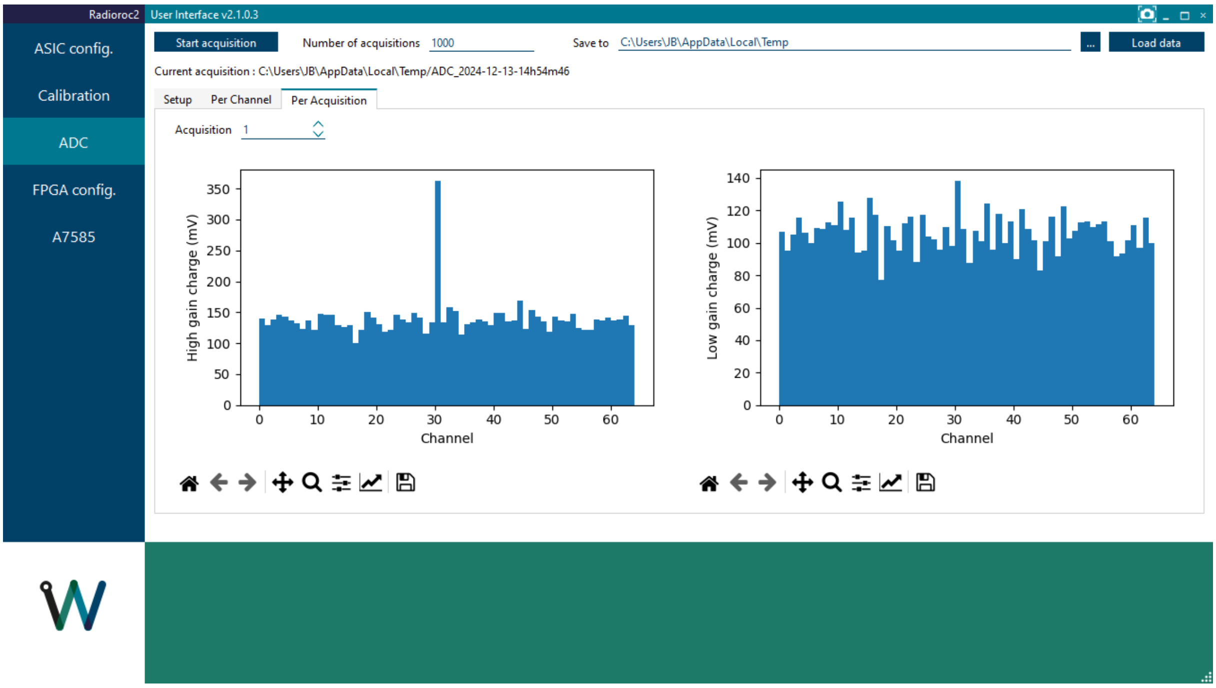


Figure 29 – DAQ result per acquisition.

3.4 FPGA config. page

FPGA I/Os are located in the bottom-right corner of the board. Output signals can be selected using combo boxes. The IO0 is by default the synchronization clock for the S-curves test (when using in_test). Synchro trigger on IO1 is the synchronization trigger for the external hold scan.

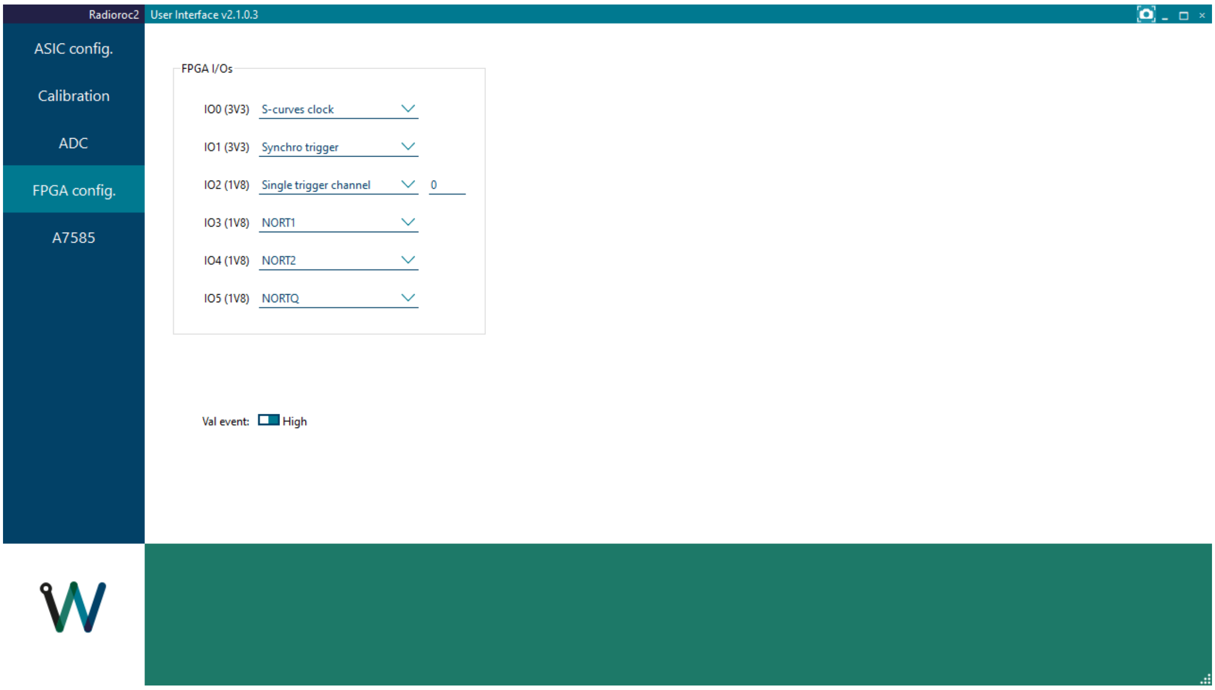


Figure 30 – FPGA config.

3.5 A7585

The A7585 is a power module sold by CAEN (https://www.caen.it/products/a7585/) used to provide the high voltage to SiPMs. A dedicated software (ZEUS) exists to use this module but it has been embedded inside the software to facilitate operations when the power module is used in conjunction with RADIOROC.

3.6 Board Options

Few options are available on the board.

The trigger of channel 62 is available on an UMCC connector:

Figure 31 - Trigger 62 options.

0 Ohm Resistors on R45 and R110 pads will allow to send the differential trigger to the FPGA. R128 is left open as there is already a 100 Ohm adaptation resistor close to the FPGA receiver.

On the other hand, wiring a 100 Ohm resistor (R128) between the 2 UMCC connectors and removing R110 and R45 will allow the user to have the LVDS trigger (_p and _n) available on the connectors for direct read-out, disconnecting it from the FPGA.

Removing all resistors will allow to monitor any single-ended signal from the ASIC on these connectors. The ASIC outputs are programmable and the single ended triggers or analog shaper outputs can be sent on these. This board has been designed with the goal of reading the LVDS triggers but the ASIC is capable of more, hence why these test points exist.

Figure 32 - SMA input injectors and Analog_Probe output (top-left corner of the board).

An internal ASIC system using registers and multiplexers allows to monitor each channel probe node and to display them on an oscilloscope. User can choose to monitor the output of the low gain and high gain preamplifier as well as the output of the high gain and low gain shaper using the analogue probe register. The analogue signal is outputted and buffered to the "Analog_Probe" SMA connector.

In typical operation, it is advised to turn off the probe register (Reset Probe) in order to avoid analogue performances degradation.

3.7 Setup to inject signals

3.7.1 Injection of a voltage step

First tests to be more familiar with the board and the software should be done using the following setup. A positive voltage step can be injected in one channel in series with a capacitor to create a charge injection. It could be injected into each channel through input connector (HE13 - 2x32pins). Alternatively, the "Ctest" input can be used for easier testing but the slow control needs to be sent in order to take into account any change in the injected channel. The capacitance here is 1.5 pF and the signal doesn't go through the input capacitance of the voltage preamplifier.

The waveform of the injected signal is displayed Figure 33. A slow negative ramp allows to inject no significant signal in the ASIC before the next step. A voltage attenuator is needed to diminish the noise from the waveform generator. With a 10 pF injector, a 16 mV voltage step in a channel corresponds more or less to 1 photoelectron with a SiPM of gain $1 \cdot 10^6$.

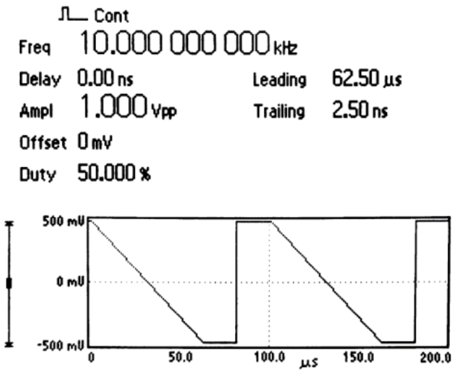


Figure 33 – Injection in each channel

Appendix

S-curves

Two Gaussians are plotted on Figure 34. The red Gaussian stands for the noise probability density function around the pedestal of the signal with the average set at x = 0 and the standard deviation **σ** = 1. In the case of a perfect Gaussian distribution, the RMS noise corresponds to the standard deviation **σ** so here is represented a signal with an RMS noise of 1. The blue Gaussian represent a signal with an RMS noise of 1 and the signal over noise ratio is 10.

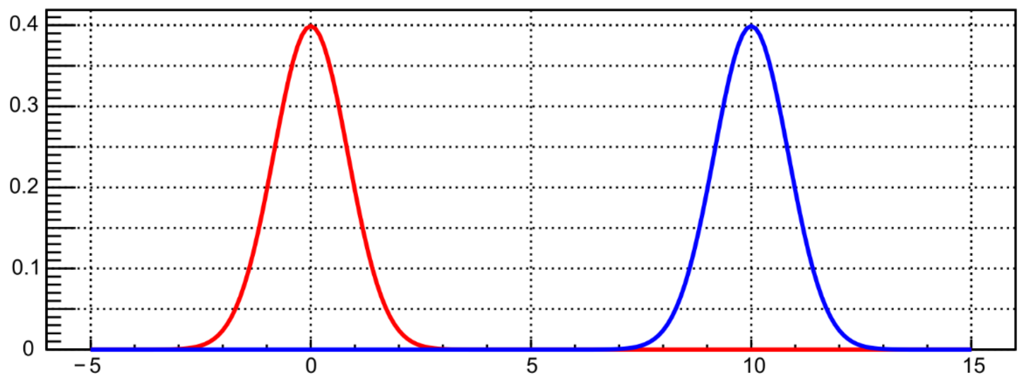


Figure 34 – Red: Normalized Gaussian with average = 0 and σ = 1 (arbitrary units). Blue: Normalized Gaussian with average = 10 and σ = 1.

By setting a threshold at x = 5 and by checking the position of the signals noise at a random time, the probability for the noise of the pedestal to be over the threshold is

$$0{,}5 \times \mathrm{erfc}\left(\frac{5}{\sqrt{2}}\right) = 2{,}8665 \cdot 10^{-7} \tag{1}$$

With *erfc()* the complementary error function. This result corresponds to one chance in 3.5 million. On the other hand, the probability for the noise on the signal to be under the threshold is also 1/3.5M. The above equation is the complementary cumulative distribution function of the normal distribution evaluated at x = 5, μ = 0 and **σ** = 1. This function is written

$$S(x) = 0{,}5 \times \mathrm{erfc}\left(\frac{x - \mu}{\sigma\sqrt{2}}\right) \tag{2}$$

With μ the mean (average of the signal or pedestal here) and **σ** the standard deviation (equivalent to the RMS noise). This function allows to evaluate the probability for an event to happen over a set threshold. The graphical representation of this function is shown on Figure 35.

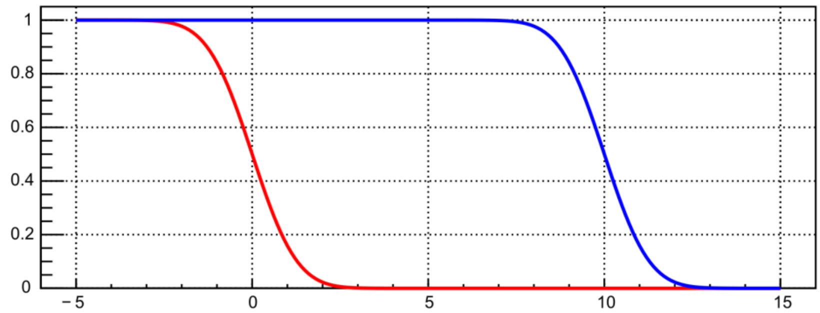


Figure 35 – "S-curve" representation of the signals shown on Figure 34.

This describes the probability to trigger on a discrete signal but concerning the pedestal it is a bit more complex because the trigger probability depends on the acquisition time as demonstrated on Figure 36 with a threshold at 5 whose trigger happens at the beginning and a threshold at t = 10 which triggers at t = 900 (arbitrary units).

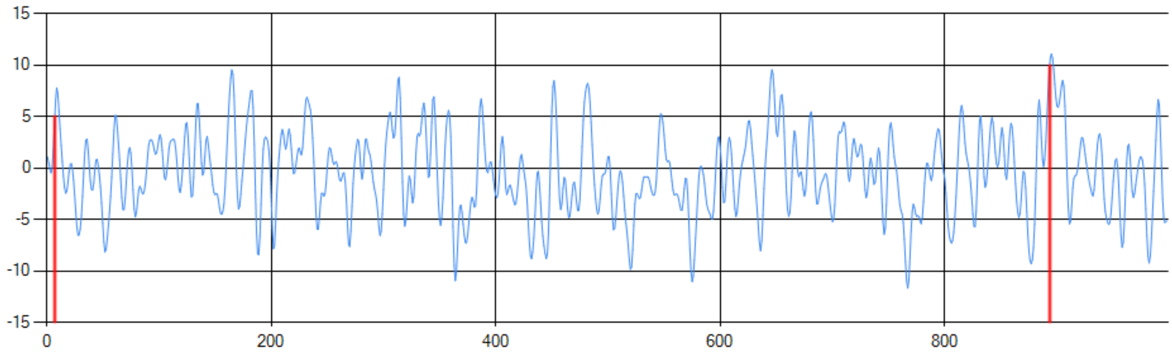


Figure 36

A study shown in *Mathematical Analysis of Random Noise* by S.O. Rice give a zero-crossing frequency as

$$f_0 = 2\left[\frac{1}{3}\frac{f_b^3 - f_a^3}{f_b - f_a}\right]^{\frac{1}{2}} \tag{3}$$

With f_b and f_a being respectively the high-cut and low-cut frequencies. In the case of an ideal CRRC bandpass filter the zero frequency is near 3 times the center frequency f_c = 1/(2πRC). Noise crosses zero in both ascending and descending ways so the number of triggers on zero N_0 would be half the number of crossings 0.5 × f_0 × T = 1.5 × f_c × T with T the time interval.

From P. Da Silva, «Élaboration d'un banc de tests pour l'électronique front-end du détecteur de particules MICROMEGAS pour l'expérience COMPASS.» (2000) it is known that the number of triggers on a threshold x during a time interval T is

$$N = N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \tag{4}$$

With N_0 = 1.5 x f_c × T and μ the pedestal position. Supposing that this crossing number is a Poisson process, the probability to have k occurrences within T is as

$$P(k) = \frac{N^k e^{-N}}{k!} \tag{5}$$

Probability of having 0 events within T is

$$P(0) = e^{-N} \tag{6}$$

Hence the probability of having at least one event during T is

$$P(k \geq 1) = 1 - P(0) \tag{7}$$

$$P(k \geq 1) = 1 - e^{-N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \tag{8}$$

The noise trigger probability on a certain threshold within T is then

$$P(x) = 1 - e^{-N_0 \times \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)} \tag{9}$$

This is valid reasoning only in the case of a Gaussian distribution of noise. This study allows to plot the trigger efficiencies on pedestal for various acquisition window lengths (10 µs, 100 µs, 1 ms).

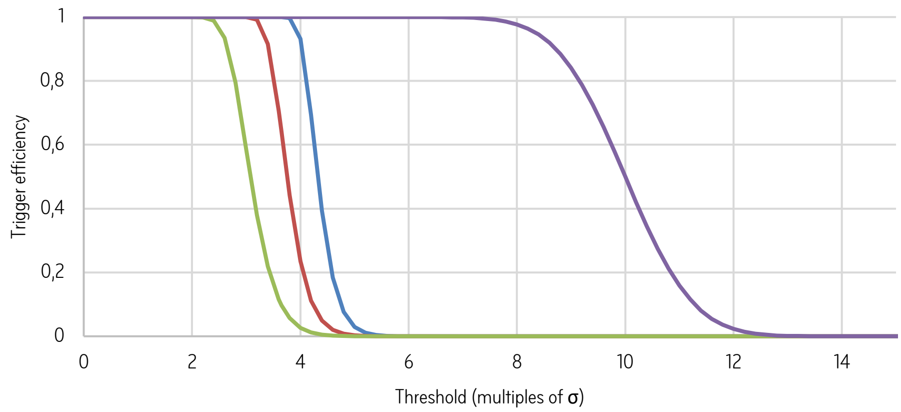


Figure 37 – Trigger efficiency on pedestal noise depending on threshold value for an acquisition window of 10 µs (green); 100 µs (red) and 1 ms (blue). Purple: S-curve of a signal with µ = 10 and σ = 1 (SNR = 10). The pedestal position is 0.

Hence having a wider acquisition window will shift the trigger efficiency along the x-axis in the case of the pedestal trigger efficiency acquisition.

4 User guide version history

Version	Date	Information
1.0	22/11/2022	Initial release of Radioroc Testboard v1 (with Cyclone V FPGA)
2.0	27/03/2024	Adaptation to Radioroc Testboard v2 (with Artix 7 FPGA)
2.1	21/08/2024	Daq description addition
2.1.0.3	13/12/2024	Update with new software/firmware functionnalities
2.1.0.3a	02/01/2024	Update the i2c main page