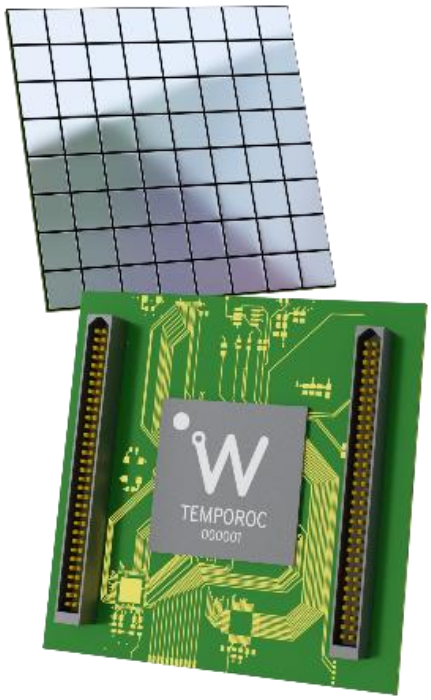
TEMPOROC2
TSMC 013G

V 1.1



Temporoc2 is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) for particle time-of-flight measurement applications. Temporoc2 combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 50ps-bin TDC. In total, Temporoc2 is capable of providing two distinct time tagging and two energy measurement of each event.

The concept of this ASIC is combining two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration. Additionally, Temporoc2 features clustering triggers readout which could be useful for particle detection with monolithic scintillator.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. Temporoc2 is suitable for any application that requires both accurate time resolution and precise energy measurement such as time-of-flight gamma detection. Temporoc2 is available in naked dies or BGA.

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on first photo-electron
Timing Resolution	20 ps rms (TBC)
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging & Dimension	Naked die – 4.9 x 11.2mm – 54.9mm^2 BGA (20x20mm, 500 balls – TBC)
Power Consumption	Power supply: 1.2V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (dual ADC and dual TDC per channel) – selectable transmission mode. 1 multiplexed time trigger output 2 ASIC trigger 0R outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), time trigger threshold adjustment (10bits), charge measurement tuning, ADC Peak Sensing, 64 trigger masks, internal temperature

	sensor, channel by channel output enable, trigger latch, programmable data output

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Maximum ratings

001	Operating Temperature	ASIC operating temperature	-40	25	120	C
002	Power Supply	VDD_PA, VDD, DVDD	1.08	1.2	1.32	V
003	Ground	GND	0	0	0	V
OO4	Analog Inputs	IN<0:63>	0	-	1.5	V
005	Digital Inputs (Single ended)	CHIP_ID<0:3>, clk_sm_i2c, ck_read, rstn_read, rstn_probe, resetn, Power_On, resetn_i2c, rstn_sc, ADCSample, ADCselectn, conv_systRO, enable_RO, trig_ext, rstn_latch,	0	-	1.5	V
006	Digital Inputs (Differential - Common Mode)	TDCstop_N/P, clk320M_N/P, valevent_n/p	520	580	640	mV
007	Digital Inputs (Differential - Swing)	TDCstop_N/P, clk320M_N/P, valevent_n/p	300	410	410	mV
008	Digital Outputs (Single Ended)	errorb_sc, scl, sda, ADCOUT<9 :0>, ADCConvDone, TDC_Fine<6:0>, TDC_Fine_ovf, TDC_Coarse<4:0>, TDC_Coarse_ovf, TDC_PD, TDC_start, TrigT_L_mux_Out, T_H_mux_Out, TrigQ_mux_Out, NORTrigQ_Out, NORTrigQ_RS_out, NORTrigT_L_RS_Out, NORTrigT_H_RS_Out, DigitalProbe_Out, ovf_time_cpt<3:0>	1.08	1.2	1.32	V
009	Digital Outputs (Differential - Common Mode)	DataROChn0_15N/P, clk_DataROChn0_15N/P, DataROChn16_31N/P, clk_DataROChn16_31N/P, DataROChn32_47N/P, clk_DataROChn32_47N/P, DataROChn48_63N/P, clk_DataROChn48_63N/P, TDC_Fast_ClkN/P, TDC_Slow_ClkN/P	520	580	640	mV
010	Digital Outputs (Differential - Swing)	DataROChn0_15N/P, clk_DataROChn0_15N/P, DataROChn16_31N/P, clk_DataROChn16_31N/P, DataROChn32_47N/P, clk_DataROChn32_47N/P, DataROChn48_63N/P, clk_DataROChn48_63N/P,	300	410	410	mV

TDC_Fast_ClkN/P
TDC_Slow_ClkN/P

Table 1 - Maximum ratings

ASIC Architecture

The block diagram of the ASIC, shown in Figure 1, where the design is a mixed signal ASIC. The channels have been arranged in 4 blocks of "clusters", where each individual block contains 16 channels of analog and digital section.

The analog part consists of input DAC, time trigger pre-amplifier with dual threshold trigger output and shapers (Low gain & High Gain). Additionally, there is a charge trigger output taken directly from Low Gain shaper. Each of the shapers has a dedicated peak detector cell.

For the digital side, there are two TDCs for each trigger output of the pre-amplifier. For the charge measurement from the shapers, there are also two ADCs embedded in this ASIC. There are 4 data transmission bank and each bank will correspond to the associated cluster. Each data output will be associated with the data frame clock and the data is transmitted at 320MHz.

Other block containing digital design is I2C slave core IP which is used for sending Slow Control[1] parameters.

This ASIC offers trigger outputs through multiplexed outputs or OR gate outputs.

[1] Slow Control stands for the register (TMR) storing the data for analog block parameters.

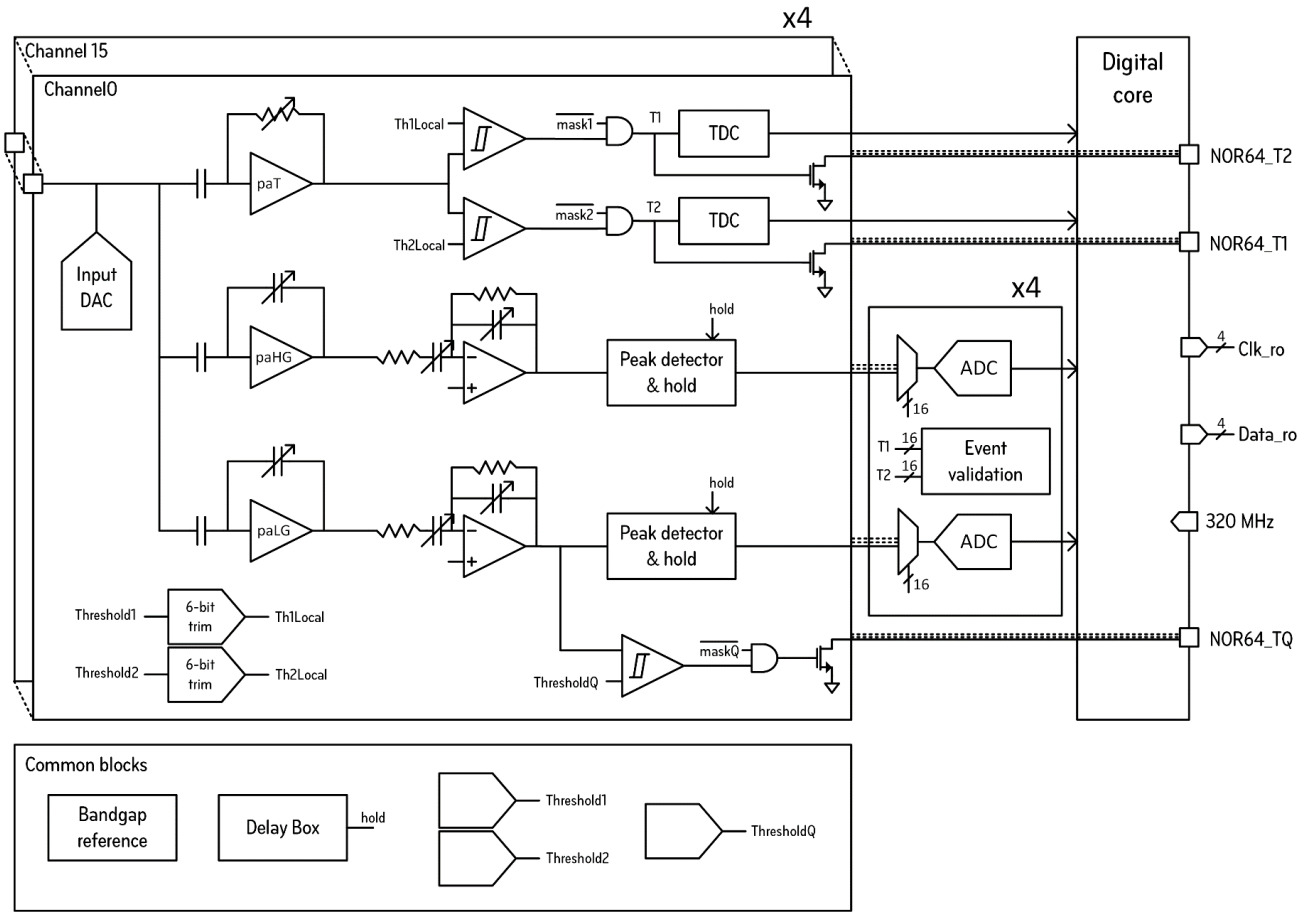


Figure 1 - ASIC block diagram

This ASIC design is designed for SiPM signal with positive polarity, ranging from 1 photoelectrons (p.e) up to 2500 p.e.

The design effort is mostly focused on the mixed signal operation of this ASIC. Most of the critical parts of the ASIC have been simulated at least in typical, best-case and worst-case corners. In typical, power supply is nominal at 1.2V, components are at nominal speed and temperature is equivalent to 27°C. In best-case, the components are set at fast speed, temperature is minimum at -40°C and power supply is boosted by 10% at 1.32 V. Lastly in worst-case, the components are set at slow speed, temperature is maximum at 125°C and power supply is reduced by 10% at 1.08 V.

Power consumption & DC levels

Following DC levels are observed at the references and biasing point of TEMPOROC2 :

Signal name	*Description*	*Sim @ 27°C*	*Sim @-40°C*	*Sim @125°C*
Vbg	Bandgap output	618.6m	618m	618.3m
Vref_1v	1V low impedance ref output	996.9m	995.9m	996m
Vbias_1v	1V low impedance bias output	990.7m	990.3m	988.1m

Vref_thresholdDac	Time Trigger threshold voltage reference	533m	570.9m	483m
Vref_thresholdDacQ	Charge Trigger threshold voltage reference	74.2m	74m	74.6m
Vref_sh	Shaper reference voltage	99m	99m	98.7m
Vref_inDac	Input DAC reference voltage	593m	592.6m	591.6m
Vref_delay	Delay cell reference voltage	101.5m	99m	131.9m
Vcp_pdetector	Peak detector P cascode	791m	790.9m	789.3m
Vcn_pdetector	Peak detector N cascode	395.3m	395m	394.3m
Vcasc_rx	LVDS receiver cascode	545.8m	545.1m	546.6m
Vcasc_paT	Pre-amp cascode voltage	841m	840.6m	839m
Vcasc_paQ	Shaper pre-amp cascode voltage	276.8m	276.7m	276.1m
ThresholdQ	Charge Trigger threshold	393.5m	390.2m	392.4m
Threshold2	Time Trigger threshold (high)	463.7m	501.5m	414m
Threshold1	Time Trigger threshold (low)	463.8m	501.5m	414m
Vthreshold_delay	Delay cell threshold output	747m	781m	698.7m
Ibp_paT	Input stage Time Trigger pre-amp bias	495.5m	510.9m	478.3m
Ibp_paLG	Input stage LG shaper pre-amp bias	530.7m	541m	514m
Ibp_paHG	Input stage HG shaper pre-amp bias	530.7m	541m	514m
Ibo_rx	Output stage differential driver bias	316m	327.2m	305.4m
Ibi_rx	Input stage differential driver bias	888m	868.7	908.7m

Table 2 - DC points

Power consumption of static power (biasing) has been simulated at 266mA over 1.2V thus 320mW for the full chip at room temperature. Power consumption is 243mA (292mW) at -40°C and 263mA (316mW) at 125°C.

I²C configuration

This ASIC can be configured using I2C interface. The I2C slave core for sending Slow Control parameters is an inherited design IP from Omega lab. This core has been designed with SEU mitigations in place. Block diagrams, list of registers and registers writing sequences are depicted in Figure 2, Table 3 and Figure 3 respectively.
Features of this IP are the following:

- Triplicated Design
- 256 addresses for the channel numbers
- 256 addresses for the register numbers
- 15 Chip ID numbers

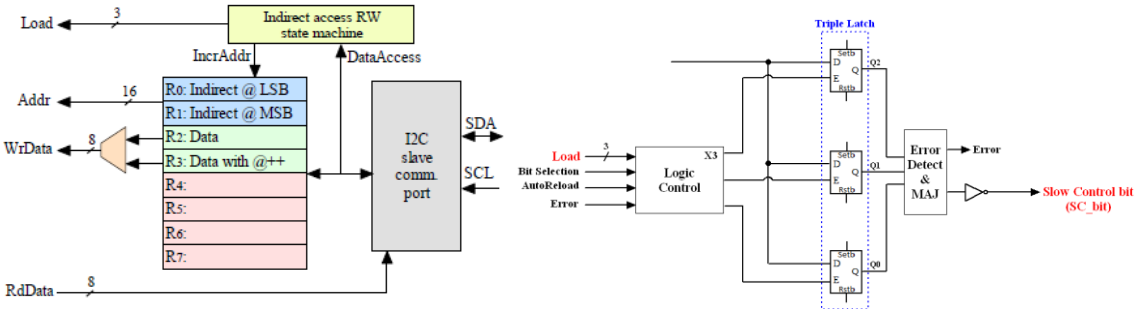


Figure 2 - Left: I2C slave core registers. Right : Slow Control bit cell design

I2C Address	Register
0	ASIC parameter address (LSB): Channel
1	ASIC parameter address (MSB): Register
2	Data Read/to Write
3	Data with auto-incremental Address
4-5-6	TBD
7	Status register (error, parity)

Table 3 - I2C slave core register descriptions

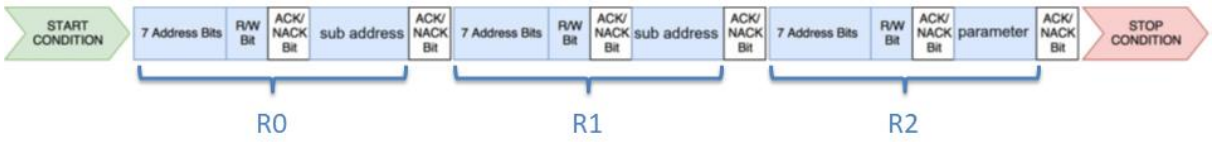
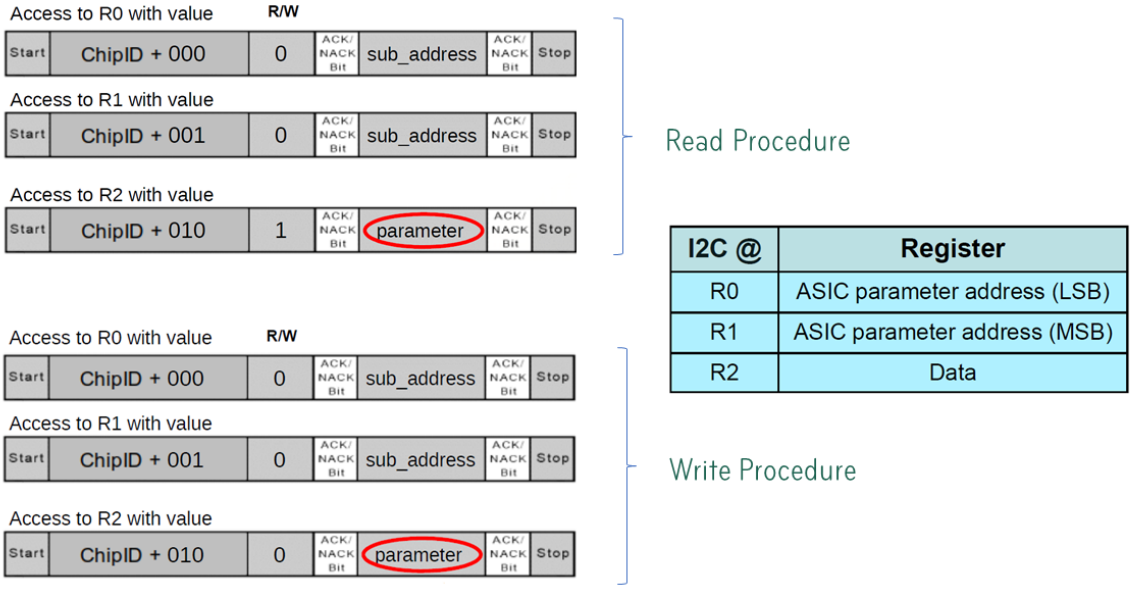


Figure 3 - I2C registers writing sequences.

Two interesting features available for addressing the Slow Control parameter sub-address. The first feature is, user can read or write each sub-address directly as depicted in Figure 4. The second feature adds the possibility of auto incrementing the sub-address base on the previous sub-address. This procedure is shown in Figure 5.



I2C @	Register
R0	ASIC parameter address (LSB)
R1	ASIC parameter address (MSB)
R2	Data

Figure 4 - Slow Control simple or direct parameter sub-addressing procedure

I2C @	Register
R0	ASIC parameter address (LSB)
R1	ASIC parameter address (MSB)
R3	Data with auto incremental @

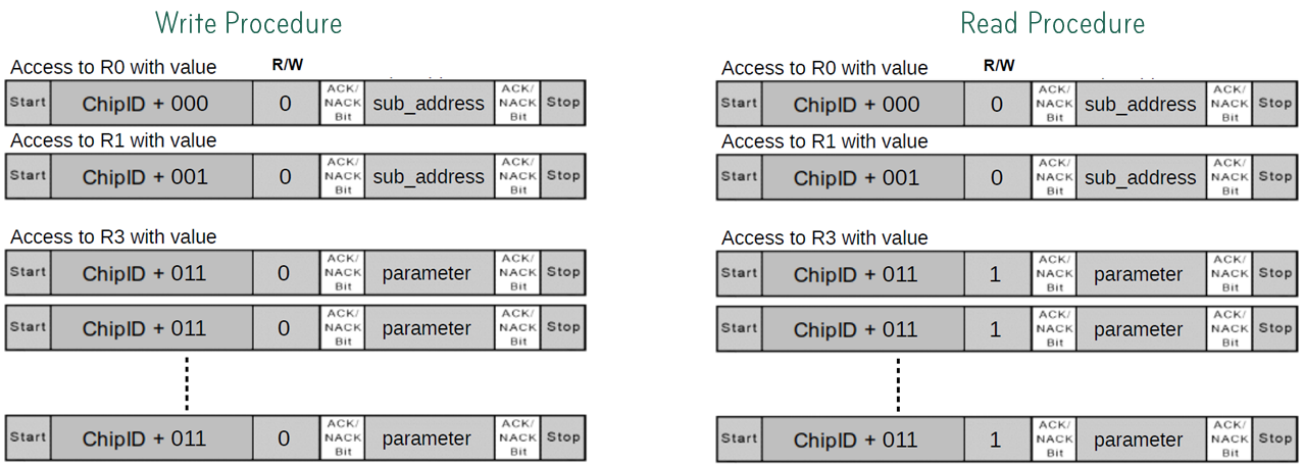


Figure 5 - Slow Control auto-increment parameter sub-addressing procedure

Slow Control parameters available for this ASIC are listed in the Table 4. “NC” term denotes non used Slow Control bits. Data in “Address” and “Subadd” columns denote the sub_address in R1 & R0 writing sequences respectively (Figure 3). Data payload in R2 (direct parameter addressing - Figure 4) or R3 (auto-increment addressing - Figure 5) will be based on data in “Parameters or Default Value” column. This ASIC configuration has been arranged in the following configuration: Address 0-63 : for ASIC channels, 64 : for ASIC bias, 65 : for ASIC clusters, 66 : for ASIC digital & 67 : for analog probe.

Address	Subadd	Bit#	Default Value	Name	Description
0-63	0	[7-4]	1111	NC	Not Connected
		3	1	useCtest	Connect test injection capacitor (input DAC measurement) 0 – Capa disconnected 1 – Capa connected (default)
		2	1	inDAC	Switch ON or OFF input DAC. 0 – Input DAC is OFF 1 – Input DAC is ON (default)
		1	0	DAC_select	Select either high impedance (require external capacitance and matching resistor) or low

					impedance (no external component required). 0 – low impedance (default) 1 – high impedance
		0	0	Cmd_test	Enable test injection 0 – Disable (default) 1 – Enable
	1	[7-0]	10000000	inDAC	Set input DAC value
	2	[7-6]	10	patComp	Set preamplifier compensation capacitance
		[5-0]	100000	patGain	Set time preamplifier gain
	3	[7-4]	0100	lgGain	Set low gain charge preamplifier gain
		[3-0]	0100	hgGain	Set high gain charge preamplifier gain
	4	[7-4]	0001	tauLG	Set high gain shaper peaking time
		[3-0]	0001	tauHG	Set low gain shaper peaking time
	5	[7-6]	00	NC	Not Connected
		[5-0]	000000	calibDacT1	Set channelwise adjustment threshold DAC 1 (low threshold)
	6	[7-6]	00	NC	Not Connected
		[5-0]	000000	calibDacT2	Set channelwise adjustment threshold DAC 2 (high threshold)
	7	[7-6]	01	NC	Not Connected
		5	1	EN_paT	Enable time preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default)
		4	1	maskTLn	Mask low threshold discriminator output 0 – discri is masked 1 – discri is operating (default)
		3	1	maskTHn	Mask high threshold discriminator output 0 – discri is masked 1 – discri is operating (default)

		2	1	maskTQn	Mask charge threshold discriminator output 0 – discri is masked 1 – discri is operating (default)
		1	1	EN_paLG	Enable low gain charge preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default)
		0	1	EN_paHG	Enable high gain charge preamplifier 0 – preamplifier disabled 1 – preamplifier enabled (default)
	8	7	0	NC	Not Connected
		6	0	Sel_ext_trigQ	Enable external trigger selection for charge trigger 0 – internal trigger (default) 1 – external trigger
		5	0	Sel_ext_trigTH	Enable external trigger selection for time trigger (High level threshold) 0 – internal trigger (default) 1 – external trigger
		4	0	Sel_Ext_trigTL	Enable external trigger selection for time trigger (High level threshold) 0 – internal trigger (default) 1 – external trigger
		3	1	EN_shLG	Enable low gain charge shaper 0 – shaper disabled 1 – shaper enabled (default)
		2	1	EN_shHG	Enable high gain charge shaper 0 – shaper disabled 1 – shaper enabled (default)

		1	1	EN_pdetLG	Enable low gain peak detector 0 – peak detector disabled 1 – peak detector enabled (default)
		0	1	EN_pdet_HG	Enable high gain peak detector 0 – peak detector disabled 1 – peak detector enabled (default)
	65	[7-4]	0000	NC	Not Connected
		3	0	Probe_QH	Analog Monitoring for Shaper 0 – disabled (default) 1 – enabled
		2	0	Probe_QL	Analog Monitoring for Shaper 0 – disabled (default) 1 – enabled
		1	0	Probe_paHG	Analog Monitoring for Shaper HG pre-amp 0 – disabled (default) 1 – enabled
		0	0	Probe_paLG	Analog Monitoring for Shaper HG pre-amp 0 – disabled (default) 1 – enabled
	66	7	0	EN_probeD_rstn_TDC	Digital Monitoring for TDC reset 0 – disabled (default) 1 – enabled
		6	0	EN_probeD_TrigT_H	Digital Monitoring for High Th Time Trigger 0 – disabled (default) 1 – enabled
		5	0	EN_probeD_TrigT_H_RS	Digital Monitoring for latched High Th Time Trigger 0 – disabled (default) 1 – enabled
		4	0	EN_probeD_TH	Digital Monitoring for intermediate (channel-selected) for latched High Th Time Trigger

					0 – disabled (default) 1 – enabled
		3	0	EN_probeD_TrigT_L	Digital Monitoring for Low Th Time Trigger 0 – disabled (default) 1 – enabled
		2	0	EN_probeD_TrigT_L_RS	Digital Monitoring for latched Low Th Time Trigger 0 – disabled (default) 1 – enabled
		1	0	EN_probeD_TL	Digital Monitoring for intermediate (channel-selected) for latched Low Th Time Trigger 0 – disabled (default) 1 – enabled
		0	0	EN_probeD_Hold_delayed	Digital Monitoring for peak detector Hold input 0 – disabled (default) 1 – enabled

64	0	[7-4]	0100	Ibo_inDac0	Set input DAC0 output stage bias
		[3-0]	0100	Ibi_inDac0	Set input DAC0 input stage bias
	1	[7-4]	0100	Ibo_inDac1	Set input DAC1 output stage bias
		[3-0]	0100	Ibi_inDac1	Set input DAC1 input stage bias
	2	[7-4]	0100	Ib_calibDac	Set trigger threshold calibration bias
		[3-0]	0100	Ib_paT	Set pre-amp (Time Trigger) input stage bias
	3	[7-4]	0100	Ib_paHG	Set pre-amp (High Gain Shaper) input stage bias
		[3-0]	0100	Ib_paLG	Set pre-amp (Low Gain Shaper) input stage bias
	4	[7-4]	0100	Ibi_shHG	Set High Gain Shaper input stage bias
		[3-0]	0100	Ibo_shHG	Set High Gain Shaper output stage bias
	5	[7-4]	0100	Ibi_shLG	Set Low Gain Shaper input stage bias

		[3-0]	0100	Ibo_shLG	Set Low Gain Shaper output stage bias
	6	[7-4]	0100	Ibi_pdetector	Set peak detector input stage bias
		[3-0]	0100	Ibi_pdbuffer	Set peak detector buffer stage bias
	7	[7-4]	0100	Ib_FCP_pdetector	Set peak detector differential P input stage bias
		[3-0]	0100	Ib_FCN_pdetector	Set peak detector differential N input stage bias
	8	[7-4]	0100	Ib_FCP_pdbuffer	Set peak detector differential P buffer stage bias
		[3-0]	0100	Ib_FCNpdbuffer	Set peak detector differential N buffer stage bias
	9	[7-4]	0100	Ibi_discri1	Set discriminator (Low Th. Time Trigger) input stage bias
		[3-0]	0100	Ibm1_discri1	Set discriminator (Low Th. Time Trigger) middle stage 1 bias
	10	[7-4]	0100	Ibm2_discri1	Set discriminator (Low Th. Time Trigger) middle stage 2 bias
		[3-0]	0100	Ibi_discri2	Set discriminator (High Th. Time Trigger) input stage bias
	11	[7-4]	0100	Ibm1_discri2	Set discriminator (High Th. Time Trigger) middle stage 1 bias
		[3-0]	0100	Ibm2_discri2	Set discriminator (High Th. Time Trigger) middle stage 2 bias
	12	[7-4]	0100	Ibi_discricharge	Set discriminator (Charge Trigger) input stage bias
		[3-0]	0100	Ibo_discricharge	Set discriminator (Charge Trigger) output stage bias
	13	7	1	ON_inDac0	Enable Input DAC0 0 – disabled 1 – enabled (default)
		6	1	ON_inDac1	Enable Input DAC1 0 – disabled 1 – enabled (default)
		5	1	ON_paT	Enable pre-amp (Time Trigger) 0 – disabled 1 – enabled (default)

		4	1	ON_paHG	Enable pre-amp (High Gain Shaper) 0 – disabled 1 – enabled (default)
		3	1	ON_paLG	Enable pre-amp (Low Gain Shaper) 0 – disabled 1 – enabled (default)
		2	1	ON_shHG	Enable High Gain Shaper 0 – disabled 1 – enabled (default)
		1	1	ON_shLG	Enable Low Gain Shaper 0 – disabled 1 – enabled (default)
		0	1	ON_pdetector	Enable peak detector 0 – disabled 1 – enabled (default)
	14	[7-5]	110	NC	
		4	1	ON_calibDac	Enable Trigger threshold calibration stage 0 – disabled 1 – enabled (default)
		3	1	ON_discriCharge	Enable Charge Trigger discriminator 0 – disabled 1 – enabled (default)
		2	1	ON_pdBuffer	Enable peak detector buffer 0 – disabled 1 – enabled (default)
		1	1	ON_discri1	Enable Low Th. Time Trigger Discriminator 0 – disabled 1 – enabled (default)
		0	1	ON_discri2	Enable High Th. Time Trigger Discriminator 0 – disabled 1 – enabled (default)
	15	[7-4]	0100	SlopeTrim	Set delay cell slope trimming
		[3-0]	0100	Ibi_discri_delay	Set delay cell discriminator input bias stage
	16	[7-4]	0100	Ibm_discri_delay	Set delay cell discriminator middle bias stage
		[3-0]	0100	Ibo_discri_delay	Set delay cell discriminator output bias stage

	17	[7-4]	0100	Ibi_delaydac	Set delay cell DAC input bias stage
		[3-0]	0100	Ibo_delayDac	Set delay cell DAC output bias stage
	18	[7-4]	0100	Ibi_delayDac16ChnClust	Set delay cell (Cluster) input bias stage
		[3-0]	0100	Ibo_delatDac16ChnClust	Set delay cell (Cluster) output bias stage

65	0	[7-4]	0010	Bias_1V HW default is wrong Should be 1000	Set Vbias reference voltage trimming
		[3-0]	0000	Bg HW default is wrong Should be 1000	Set BandGap reference voltage trimming
	1	[7-0]	00000000	Dac1[7-0]	Set Time Trigger threshold (Low) : Bits [7-0]
	2	[7-2]	000000	Dac2[5-0]	Set Time Trigger threshold (High) : Bits [5-0]
		[1-0]	01	Dac1[9-8]	Set Time Trigger threshold (Low) : Bits [9-8]
	3	[7-4]	0000	DacQ[3-0]	Set Charge Trigger threshold : Bits [3-0]
		[3-0]	0100	Dac2[9-6]	Set Time Trigger threshold (High) : Bits [9-6]
	4	[7-6]	00	NC	
		[5-0]	010000	DacQ[9-4]	Set Charge Trigger threshold : Bits [9-4]
	5	[7-4]	0100	Ibi_thresholdDac	Set Time threshold DAC input stage bias
		[3-0]	0100	Ibo_thresholdDac	Set Time threshold DAC output stage bias
	6	[7-4]	0100	Ibi_thresholdDacQ	Set Charge threshold DAC input stage bias
		[3-0]	0100	Ibo_thresholdDacQ	Set Charge threshold DAC output stage bias
	7	[7-4]	0000	NC	
		3	1	EN_th1	Enable Time Trigger threshold (Low) : 0 – disabled 1 – enabled (default)

		2	1	EN_th2	Enable Time Trigger threshold (High) : 0 – disabled 1 – enabled (default)
		1	1	EN_thQ	Enable ChargeTrigger threshold : 0 – disabled 1 – enabled (default)
		0	1	EN_bg	Enable BandGap reference voltage : 0 – disabled 1 – enabled (default)
	8	[7-0]	01010000	Delay_clusterL	Set delay cluster for Low Th. Time Trigger
	9	[7-0]	01010000	Delay_clusterH	Set delay cluster for High Th. Time Trigger
	10	[7-0]	11111111	Delay	Set delay for peak detector
	11	7	0	hysteresis1	Enable hysteresis for discriminator1: 0 – enable (default) 1 – disable
		6	0	hysteresis2	Enable hysteresis for discriminator2: 0 – enable (default) 1 – disable
		5	0	EnBypassResetMgmt	Bypass reset cluster: 0 –disable (default) 1 – enable
		4	0	Sel_hold	Select peak detector Hold input : 0 – internal (default) 1 – external
		3	1	EN_delay	Enable delay cell : 0 – disabled 1 – enabled (default)
		2	1	Latch	Enable trigger latch : 0 – disabled 1 – enabled (default)
		[1-0]	01	Sel_trig	Select trigger source for peak detector selection : 00 – global ASIC trigger 01 – Local Time Trigger Low Th. (default)

					1 0 – Local Time Trigger High Th. 11 – Local Charge Trigger High
	12	7	0	EN_ProbeD_SelectADCHG	Digital Monitoring for High Gain Shaper ADC selection (Cluster 0) 0 – disabled (default) 1 – enabled
		6	0	EN_ProbeD_SelectADCLG	Digital Monitoring for Low Gain Shaper ADC selection (Cluster 0) 0 – disabled (default) 1 – enabled
		5	0	EN_ProbeD_rstn_delaybox	Digital Monitoring for Digital Delay cell Reset (Cluster 0) 0 – disabled (default) 1 – enabled
		4	0	EN_ProbeD_reset	Digital Monitoring for cluster Delay cell Reset (Cluster 0) 0 – disabled (default) 1 – enabled
		3	0	EN_ProbeD_end_delayH	Digital Monitoring for cluster Delay cell output (High Th. Time Trigger) (Cluster 0) 0 – disabled (default) 1 – enabled
		2	0	EN_ProbeD_end_delayL	Digital Monitoring for cluster Delay cell output (Low Th. Time Trigger) (Cluster 0) 0 – disabled (default) 1 – enabled
		1	0	EN_ProbeD_ConvDoneADCHG	Digital Monitoring for High Gain shaper ADC conversion done (Cluster 0) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_ConvDoneADCLG	Digital Monitoring for Low Gain shaper ADC

					conversion done (Cluster 0) 0 – disabled (default) 1 – enabled
	13	[7-2]	0	NC	
		1	0	EN_ProbeD_RstnADC	Digital Monitoring for ADC reset (Cluster 0) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_RstnLatchint	Digital Monitoring for trigger latch reset (Cluster 0) 0 – disabled (default) 1 – enabled
	14	7	0	EN_ProbeD_SelectADCHG	Digital Monitoring for High Gain Shaper ADC selection (Cluster 1) 0 – disabled (default) 1 – enabled
		6	0	EN_ProbeD_SelectADCLG	Digital Monitoring for Low Gain Shaper ADC selection (Cluster 1) 0 – disabled (default) 1 – enabled
		5	0	EN_ProbeD_rstn_delaybox	Digital Monitoring for Digital Delay cell Reset (Cluster 1) 0 – disabled (default) 1 – enabled
		4	0	EN_ProbeD_reset	Digital Monitoring for cluster Delay cell Reset (Cluster 1) 0 – disabled (default) 1 – enabled
		3	0	EN_ProbeD_end_delayH	Digital Monitoring for cluster Delay cell output (High Th. Time Trigger) (Cluster 1) 0 – disabled (default) 1 – enabled
		2	0	EN_ProbeD_end_delayL	Digital Monitoring for cluster Delay cell output

					(Low Th. Time Trigger) (Cluster 1) 0 – disabled (default) 1 – enabled
		1	0	EN_ProbeD_ConvDoneADCHG	Digital Monitoring for High Gain shaper ADC conversion done (Cluster 1) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_ConvDoneADCLG	Digital Monitoring for Low Gain shaper ADC conversion done (Cluster 1) 0 – disabled (default) 1 – enabled
	15	[7-2]	0	NC	
		1	0	EN_ProbeD_RstnADC	Digital Monitoring for ADC reset (Cluster 1) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_RstnLatchint	Digital Monitoring for trigger latch reset (Cluster 1) 0 – disabled (default) 1 – enabled
	16	7	0	EN_ProbeD_SelectADCHG	Digital Monitoring for High Gain Shaper ADC selection (Cluster 2) 0 – disabled (default) 1 – enabled
		6	0	EN_ProbeD_SelectADCLG	Digital Monitoring for Low Gain Shaper ADC selection (Cluster 2) 0 – disabled (default) 1 – enabled
		5	0	EN_ProbeD_rstn_delaybox	Digital Monitoring for Digital Delay cell Reset (Cluster 2) 0 – disabled (default) 1 – enabled

		4	0	EN_ProbeD_reset	Digital Monitoring for cluster Delay cell Reset (Cluster 2) 0 – disabled (default) 1 – enabled
		3	0	EN_ProbeD_end_delayH	Digital Monitoring for cluster Delay cell output (High Th. Time Trigger) (Cluster 2) 0 – disabled (default) 1 – enabled
		2	0	EN_ProbeD_end_delayL	Digital Monitoring for cluster Delay cell output (Low Th. Time Trigger) (Cluster 2) 0 – disabled (default) 1 – enabled
		1	0	EN_ProbeD_ConvDoneADCHG	Digital Monitoring for High Gain shaper ADC conversion done (Cluster 2) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_ConvDoneADCLG	Digital Monitoring for Low Gain shaper ADC conversion done (Cluster 2) 0 – disabled (default) 1 – enabled
	17	[7-2]	0	NC	
		1	0	EN_ProbeD_RstnADC	Digital Monitoring for ADC reset (Cluster 2) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_RstnLatchint	Digital Monitoring for trigger latch reset (Cluster 2) 0 – disabled (default) 1 – enabled
	18	7	0	EN_ProbeD_SelectADCHG	Digital Monitoring for High Gain Shaper ADC selection (Cluster 3) 0 – disabled (default)

					1 – enabled
		6	0	EN_ProbeD_SelectADCLG	Digital Monitoring for Low Gain Shaper ADC selection (Cluster 3) 0 – disabled (default) 1 – enabled
		5	0	EN_ProbeD_rstn_delaybox	Digital Monitoring for Digital Delay cell Reset (Cluster 3) 0 – disabled (default) 1 – enabled
		4	0	EN_ProbeD_reset	Digital Monitoring for cluster Delay cell Reset (Cluster 3) 0 – disabled (default) 1 – enabled
		3	0	EN_ProbeD_end_delayH	Digital Monitoring for cluster Delay cell output (High Th. Time Trigger) (Cluster 3) 0 – disabled (default) 1 – enabled
		2	0	EN_ProbeD_end_delayL	Digital Monitoring for cluster Delay cell output (Low Th. Time Trigger) (Cluster 3) 0 – disabled (default) 1 – enabled
		1	0	EN_ProbeD_ConvDoneADCHG	Digital Monitoring for High Gain shaper ADC conversion done (Cluster 3) 0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_ConvDoneADCLG	Digital Monitoring for Low Gain shaper ADC conversion done (Cluster 3) 0 – disabled (default) 1 – enabled
	19	[7-2]	0	NC	
		1	0	EN_ProbeD_RstnADC	Digital Monitoring for ADC reset (Cluster 3)

					0 – disabled (default) 1 – enabled
		0	0	EN_ProbeD_RstnLatchint	Digital Monitoring for trigger latch reset (Cluster 3) 0 – disabled (default) 1 – enabled

66	0	[7-4]	1111	TX_strength	Setting for CLPS driver strength
		[3-0]	1100	TX_preEmphasis	Setting for CLPS driver pre-emphasis
	1	[7-2]	000000	NC	
		[1-0]	10	Delay_PreEmphasis	Setting for CLPS driver pre-emphasis delay
	2	7	1	EN_RX	Select : 0 –internal Forced_ValEvtn (SC) 1 –external ValEvt (through differential RX buffer)
		6	0	PP_RX	Enable Power Pulsing for differential receiver 0 – disabled (default) 1 – enabled
		5	1	Forced_ValEvtn	Internal ValEvt (trigger Fast masking) 0 – enabled 1 – disabled (default)
		[4-0]	00000	NC	
	3	7	1	EN_ck320	Enable 320MHz clock transmission to ASIC core 0 – disabled 1 – enabled (default)
		6	0	EN_digitalProbe	Enable Digital monitoring output 0 – disabled (default) 1 – enabled
		5	0	EN_Nor_TrigT_L_RS_pad	Enable NOR gate output Low Th. Time Trigger 0 – disabled (default) 1 – enabled
		4	0	EN_Nor_TrigT_Q_pad	Enable NOR gate output Non latched Charge Trigger 0 – disabled (default)

					1 – enabled
		3	0	EN_Nor_TrigT_H_RS_pad	Enable NOR gate output High Th. Time Trigger 0 – disabled (default) 1 – enabled
		2	0	EN_Nor_TrigQ_RS_pad	Enable NOR gate output latched Charge Trigger 0 – disabled (default) 1 – enabled
		[1-0]	00	selGlobalTrigger	Select Global trigger source for peak detector selection 00 – Ground (default) 01 – Low Th. Time Trigger 10 – High Th. Time Trigger 11 – Charge Trigger
	4	7	0	EN_trigT_L_mux_pad	Enable multiplexed output for Low Th. Time Trigger 0 – disabled (default) 1 – enabled
		6	0	EN_trigT_H_mux_pad	Enable multiplexed output for High Th. Time Trigger 0 – disabled (default) 1 – enabled
		5	0	EN_trigQ_mux_pad	Enable multiplexed output for Charge Trigger 0 – disabled (default) 1 – enabled
		[4-0]	01111	modeRO	Set digital part readout mode
	5	7	0	Inh_rstOnDlyH	Inhibit peak detector reset on High Gain cluster delay box 0 : Reset is active (default) 1 : Reset is inhibited
		6	0	Inh_rstOnDlyL	Inhibit peak detector reset on low gain cluster delay box 0 : Reset is active (default) 1 : Reset is inhibited
		5	0	Sync_Cluster	Cluster Sync Selection 0 : All clusters data conversion (default) 1 : Cluster specific data conversion
		[4-0]	00100	Nb_trigger	Set trigger sum threshold

	6	7	0	TDC_passthrough	If enabled data from standalone TDC is not latched
		[6-4]	000	NC	
		[3-0]	1111	EnableClkDataRO	Enable Data Readout Clock 0 : Disable 1 : Enable (default)

67	0	[7-5]	000	NC	
		4	1	ON_biasBuffer	Enable analog buffer bias 0 : Disable 1 : Enable (default)
		[3-0]	0100	Ibi_Buffer	Set analog buffer input stage bias
	1	[7-4]	0100	ibFCP_buffer	Set analog buffer differential P stage bias
		[3-0]	0100	ibFCN_buffer	Set analog buffer differential N stage bias
	2	[7-6]	00	cmPDLGn	Miller capacitance for Low Gain Shaper peak detector buffer(n) 00 – 100fF (default) 01 – 300fF 10 – 500fF 11 – 700fF
		[5-4]	00	cmPDLGp	Miller capacitance for Low Gain Shaper peak detector buffer(p) 00 – 100fF (default) 01 – 300fF 10 – 500fF 11 – 700fF
		[3-2]	00	cmPDHGn	Miller capacitance for High Gain Shaper peak detector buffer(n) 00 – 100fF (default) 01 – 300fF 10 – 500fF 11 – 700fF
		[1-0]	00	cmPDHGp	Miller capacitance for High Gain Shaper peak detector buffer(p) 00 – 100fF (default) 01 – 300fF 10 – 500fF

					11 – 700fF
	3	[7-5]	000	NC	
		4	0	EN_probeA	Enable analog monitoring 0 : Disable (default) 1 : Enable
		3	0	EN_PDLG	Enable Low Gain Shaper peak detector multiplexed output 0 : Disable (default) 1 : Enable
		2	0	EN_PDHG	Enable Hign Gain Shaper peak detector multiplexed output 0 : Disable (default) 1 : Enable
		[1-0]	00	cmProbeA	Miller capacitance for Analog Monitoring buffer(p) 00 – 100fF (default) 01 – 300fF 10 – 500fF 11 – 700fF

Table 4 – TEMPOROC2 Slow Control list

Specifically, for Address 0-63, each subadd in this section will correspond only to the selected channel. This means that, in order to have all channels wide operation, each Address will have to be selected when writing the Slow Control operation. Otherwise, all the other Address (64-67) operations will be effective for the whole ASIC.

Pinout, Power supplies & mechanics

Mechanics

Temporoc2 is packaged in 20x20mm 516 ball flip-chip BGA package.

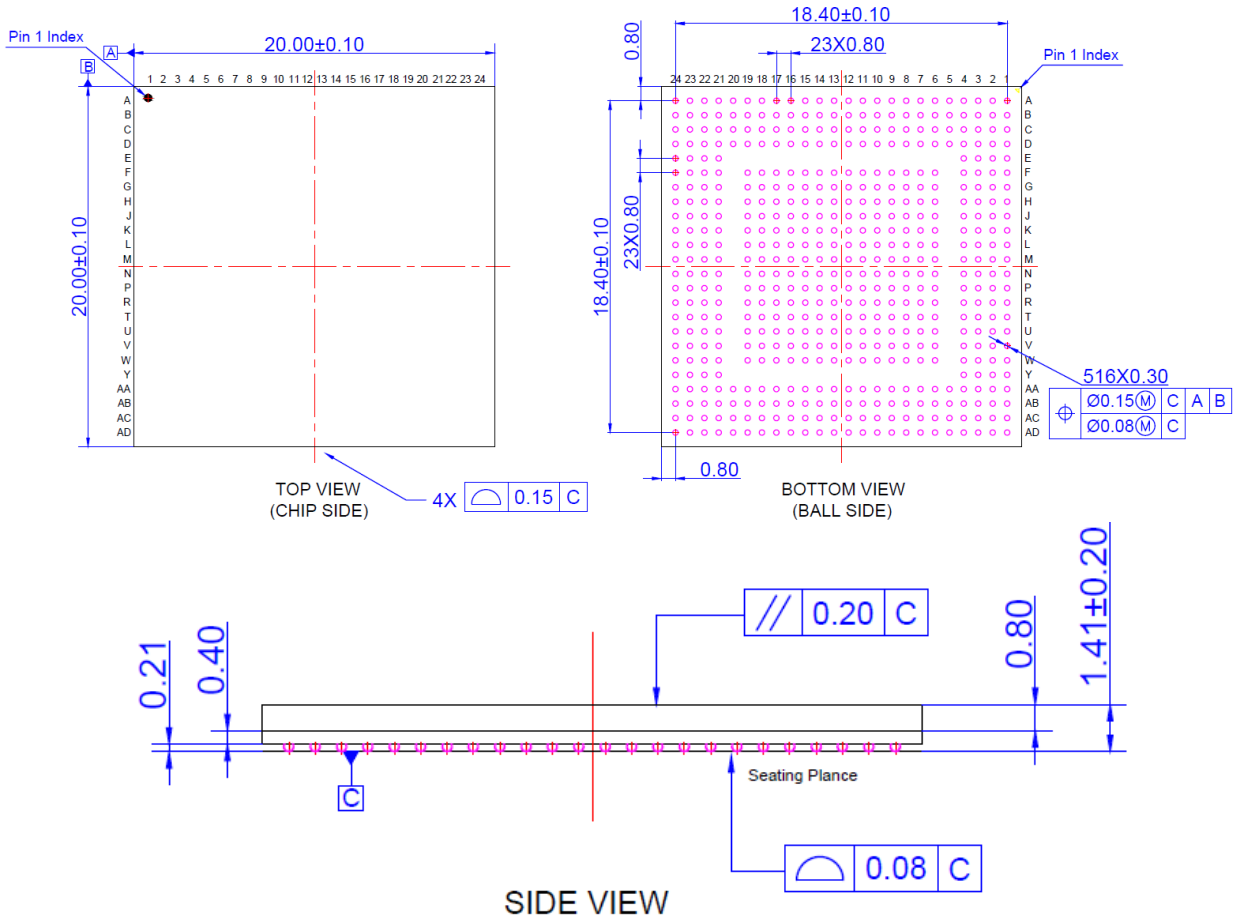


Figure 6 - Temporoc2 BGA packaging mechanical view

Ball-out

	1	2	3	4	5	6	7	8	9	10	11	12
A	in<53>	in<55>	in<57>	in<59>	in<61>	in<63>	in<62>	Power_On	sda	clk_sm_i2c	valevent_n	valevent_p
B	in<51>	in<52>	in<54>	in<56>	in<58>	in<60>	in_ctest	rstn_sc	resetn_i2c	scl	vcasc_rx	GND
C	in<49>	in<50>	ibi_rx	NC	NC	NC	NC	NC	NC	NC	NC	GND
D	in<47>	in<48>	ibo_rx	NC	NC	NC	NC	NC	NC	NC	NC	GND
E	in<45>	in<46>	vcp_aBuffer	NC								
F	in<43>	in<44>	vcn_aBuffer	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
G	in<41>	in<42>	vref_thresholdDacQ	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
H	in<39>	in<40>	vref_thresholdDac	NC		VDD	VDD	NC	GND	GND	GND	GND
J	in<37>	in<38>	VthresholdQ	NC		VDD	VDD	NC	GND	GND	GND	GND
K	in<35>	in<36>	Vthreshold2	NC		VDD	VDD	NC	GND	GND	GND	GND
L	in<33>	in<34>	Vthreshold1	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
M	ibp_paHg	in<32>	ibp_paLg	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
N	ibp_paT	in<30>	vref_1v	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
P	in<31>	in<28>	vbg	NC		VDD_PA	VDD_PA	NC	GND	GND	GND	GND
R	in<29>	in<26>	vbias_1v	NC		VDD	VDD	NC	GND	GND	GND	GND
T	in<27>	in<24>	vref_inDac	NC		VDD	VDD	NC	GND	GND	GND	GND
U	in<25>	in<22>	vcasc_paT	NC		VDD	VDD	NC	GND	GND	GND	GND
V	in<23>	in<20>	vcasc_paQ	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
W	in<21>	in<18>	vref_sh	NC		VDD_PA	VDD_PA	VDD_PA	VDD	VDD	VDD	GND
Y	in<19>	in<16>	vcp_pdetect	NC								
Z	in<17>	in<14>	vcn_pdetect	NC	NC	NC	NC	NC	NC	NC	NC	GND
AA	in<15>	in<12>	vref_delay	NC	NC	NC	NC	NC	NC	NC	NC	GND
AB	in<13>	in<10>	in<8>	in<6>	in<4>	in<2>	Vth_delay	vcm_ADC	NC	NC	NC	GND
AC	in<11>	in<9>	in<7>	in<5>	in<3>	in<1>	in<0>	reserved	ck_read	VinP_ADC	VinN_ADC	rstn_read
	1	2	3	4	5	6	7	8	9	10	11	12

Figure 7 – TEMPOROC2 Ball-out west part

12	13	14	15	16	17	18	19	20	21	22	23	24	
valevent_p	TDC_CLK320_N	TDC_CLK320_P	NORTrigT_L_RS_Out	NORTrigT_H_RS_Out	TDC_Hit_P	TDC_Hit_N	NC	NC	TDC_toa_fine<0>	TDC_toa_fine<1>	clk320M_N	clk320M_P	A
GND	NC	NC	TrigT_L_mux_Out	T_H_mux_Out	TrigQ_mux_Out	Digital Probe_Out	clk_DataROChn48_63P	clk_DataROChn48_63N	TDC_toa_fine<2>	TDC_toa_fine<3>	NC	NC	B
GND	NC	NC	NORTrigQ_Out	NORTrigQ_RS_out	NC	TDC_data_valid	DataROChn48_63P	DataROChn48_63N	TDC_toa_fine<4>	TDC_toa_coarse<0>	NC	NC	C
GND	NC	NC	NC	NC	NC	NC	OvfTimeCptChn48_63N	OvfTimeCptChn48_63P	TDC_toa_coarse<1>	TDC_toa_coarse<2>	NC	NC	D
									TDC_toa_coarse<3>	TDC_cal_fine<0>	NC	NC	E
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TDC_cal_fine<1>	TDC_cal_fine<2>	clk_DataROChn32_47P	clk_DataROChn32_47N	F
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		TDC_cal_fine<3>	TDC_cal_fine<4>	DataROChn32_47P	DataROChn32_47N	G
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TDC_cal_coarse<0>	TDC_cal_coarse<1>	OvfTimeCptChn32_47N	OvfTimeCptChn32_47P	H
GND	GND	GND	GND	GND	GND	DVDD	DVDD		TDC_cal_coarse<2>	TDC_cal_coarse<3>	NC	NC	J
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	NC	NC	K
GND	GND	GND	GND	GND	GND	DVDD	DVDD		rstn_latch	analogProbe_Out	PDHG_P	PDHG_N	L
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	chip_id<0>	errorb_sc	M
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	chip_id<3>	chip_id<2>	chip_id<1>	N
GND	GND	GND	GND	GND	GND	DVDD	DVDD		trig_ext	hold_ext	PDLG_P	PDLG_N	P
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	enable_RO	conv_systRO	R
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	clk_DataROChn16_31P	clk_DataROChn16_31N	T
GND	GND	GND	GND	GND	GND	DVDD	DVDD		NC	NC	DataROChn16_31P	DataROChn16_31N	U
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		NC	NC	OvfTimeCptChn16_31N	OvfTimeCptChn16_31P	V
GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD		NC	NC	NC	NC	W
									NC	NC	NC	NC	Y
GND	NC	NC	NC	NC	NC	NC	DataROChn0_15P	DataROChn0_15N	NC	NC	NC	NC	Z

GND	NC	NC	ADCOUT<5>	ADCOUT<4>	ADCOUT<1>	ADCOUT<0>	OvfTimeCptChn0_15N	OvfTimeCptChn0_15P	NC	NC	NC	NC	AA
GND	NC	NC	ADCOUT<7>	ADCOUT<6>	ADCOUT<3>	ADCOUT<2>	NC	NC	NC	NC	NC	NC	AB
rstn_read	rstn_probe	resetn	ADCOUT<9>	ADCOUT<8>	ADCConvDone	ADCSample	ADCselectn	NC	NC	NC	clk_DataROChn0_15P	clk_DataROChn0_15N	AC
12	13	14	15	16	17	18	19	20	21	22	23	24	

Figure 8– TEMPOROC2 ball-out East part

TEMPOROC2 pinout

Net Name	BGA Ball	Type
ibp_paT	N1	Bias
ibp_paHg	M1	
ibp_paLg	M3	
vcm_ADC	AB8	
RESERVED	AC8	
Vthreshold1	L3	
Vthreshold2	K3	
VthresholdQ	J3	
vbg	P3	
vbias_1v	R3	
vcasc_paQ	V3	
vcasc_paT	U3	
vcn_aBuffer	F3	
ibo_rx	D3	
vcn_pdetect	Z3	
vcp_aBuffer	E3	
ibi_rx	C3	
vcp_pdetect	Y3	
vref_1v	N3	
VREF_DELAY	AA3	
VREF_INDAC	T3	
VREF_SH	W3	
vref_thresholdDac	H3	
vref_thresholdDacQ	G3	
VTH_DELAY	AB7	
vcasc_rx	B11	
IN_CTEST	B7	Analog Input
VinP_ADC	AC10	
VinN_ADC	AC11	
PDHG_P	L23	Multiplexed Analog Output
PDHG_N	L24	
PDLG_P	P23	
PDLG_N	P24	
analogProbe_Out	L22	
CHIP_ID<0>	M23	I/O Digital Single Ended
CHIP_ID<1>	N24	
CHIP_ID<2>	N23	
CHIP_ID<3>	N22	
clk_sm_i2c	A10	
errorb_sc	M24	
ck_read	AC9	
rstn_read	AC12	
rstn_probe	AC13	
resetn	AC14	
Power_On	A8	
resetn_i2c	B9	
rstn_sc	B8	
scl	B10	
sda	A9	
ADCOUT<9>	AC15	
ADCOUT<8>	AC16	
ADCOUT<7>	AB15	
ADCOUT<6>	AB16	
ADCOUT<5>	AA15	
ADCOUT<4>	AA16	
ADCOUT<3>	AB17	
ADCOUT<2>	AB18	
ADCOUT<1>	AA17	
ADCOUT<0>	AA18	
ADCSample	AC18	
ADCConvDone	AC17	
ADCselectn	AC19	
TDC_toa_coarse<1>	D21	
TDC_toa_coarse<0>	C22	
TDC_toa_fine<4>	C21	
TDC_toa_fine<3>	B22	
TDC_toa_fine<1>	A22	
TDC_toa_fine<2>	B21	
TDC_toa_fine<0>	A21	
TDC_cal_fine<4>	G22	
TDC_cal_fine<2>	F22	
TDC_cal_fine<1>	F21	
TDC_cal_fine<0>	E22	
TDC_toa_coarse<3>	E21	
TDC_toa_coarse<2>	D22	
TDC_cal_fine<3>	G21	
TDC_data_valid	C18	
NC	C17	
TrigT_L_mux_Out	B15	
T_H_mux_Out	B16	

TrigQ_mux_Out	B17	
NORTrigQ_Out	C15	
NORTrigQ_RS_out	C16	
NNORTrigT_L_RS_Out	A15	
NORTrigT_H_RS_Out	A16	
DigitalProbe_Out	B18	
conv_systRO	R24	
hold_ext	P22	
enable_RO	R23	
trig_ext	P21	
rstn_latch	L21	
OvfTimeCptChn48_63P	D20	
OvfTimeCptChn32_47P	H24	
OvfTimeCptChn16_31P	V24	
OvfTimeCptChn0_15P	AA20	
DVDD	F13	Power Supply - DVDD
DVDD	F14	
DVDD	F15	
DVDD	F16	
DVDD	F17	
DVDD	F18	
DVDD	F19	
DVDD	G13	
DVDD	G14	
DVDD	G15	
DVDD	G16	
DVDD	G17	
DVDD	G18	
DVDD	G19	
DVDD	H18	
DVDD	H19	
DVDD	J18	
DVDD	J19	
DVDD	K18	
DVDD	K19	
DVDD	L18	
DVDD	L19	
DVDD	M18	
DVDD	M19	
DVDD	N18	
DVDD	N19	
DVDD	P18	
DVDD	P19	
DVDD	R18	
DVDD	R19	
DVDD	T18	
DVDD	T19	
DVDD	U18	
DVDD	U19	
DVDD	V13	
DVDD	V14	
DVDD	V15	
DVDD	V16	
DVDD	V17	
DVDD	V18	
DVDD	V19	
DVDD	W13	
DVDD	W14	
DVDD	W15	
DVDD	W16	
DVDD	W17	
DVDD	W18	
DVDD	W19	
GND	AA12	Ground
GND	AB12	
GND	B12	
GND	C12	
GND	D12	
GND	F12	
GND	G12	
GND	H9	
GND	H10	
GND	H11	
GND	H12	
GND	H13	
GND	H14	
GND	H15	
GND	H16	
GND	H17	
GND	J9	
GND	J10	
GND	J11	
GND	J12	
GND	J13	

GND	J14	
GND	J15	
GND	J16	
GND	J17	
GND	K9	
GND	K10	
GND	K11	
GND	K12	
GND	K13	
GND	K14	
GND	K15	
GND	K16	
GND	K17	
GND	L9	
GND	L10	
GND	L11	
GND	L12	
GND	L13	
GND	L14	
GND	L15	
GND	L16	
GND	L17	
GND	M9	
GND	M10	
GND	M11	
GND	M12	
GND	M13	
GND	M14	
GND	M15	
GND	M16	
GND	M17	
GND	N9	
GND	N10	
GND	N11	
GND	N12	
GND	N13	
GND	N14	
GND	N15	
GND	N16	
GND	N17	
GND	P9	
GND	P10	
GND	P11	
GND	P12	
GND	P13	
GND	P14	
GND	P15	
GND	P16	
GND	P17	
GND	R9	
GND	R10	
GND	R11	
GND	R12	
GND	R13	
GND	R14	
GND	R15	
GND	R16	
GND	R17	
GND	T9	
GND	T10	
GND	T11	
GND	T12	
GND	T13	
GND	T14	
GND	T15	
GND	T16	
GND	T17	
GND	U9	
GND	U10	
GND	U11	
GND	U12	
GND	U13	
GND	U14	
GND	U15	
GND	U16	
GND	U17	
GND	V12	
GND	W12	
GND	Z12	
IN<0>	AC7	Analog Input
IN<1>	AC6	
IN<2>	AB6	
IN<3>	AC5	
IN<4>	AB5	

IN<5>	AC4	
IN<6>	AB4	
IN<7>	AC3	
IN<8>	AB3	
IN<9>	AC2	
IN<10>	AB2	
IN<11>	AC1	
IN<12>	AA2	
IN<13>	AB1	
IN<14>	Z2	
IN<15>	AA1	
IN<16>	Y2	
IN<17>	Z1	
IN<18>	W2	
IN<19>	Y1	
IN<20>	V2	
IN<21>	W1	
IN<22>	U2	
IN<23>	V1	
IN<24>	T2	
IN<25>	U1	
IN<26>	R2	
IN<27>	T1	
IN<28>	P2	
IN<29>	R1	
IN<30>	N2	
IN<31>	P1	
IN<32>	M2	
IN<33>	L1	
IN<34>	L2	
IN<35>	K1	
IN<36>	K2	
IN<37>	J1	
IN<38>	J2	
IN<39>	H1	
IN<40>	H2	
IN<41>	G1	
IN<42>	G2	
IN<43>	F1	
IN<44>	F2	
IN<45>	E1	
IN<46>	E2	
IN<47>	D1	
IN<48>	D2	
IN<49>	C1	
IN<50>	C2	
IN<51>	B1	
IN<52>	B2	
IN<53>	A1	
IN<54>	B3	
IN<55>	A2	
IN<56>	B4	
IN<57>	A3	
IN<58>	B5	
IN<59>	A4	
IN<60>	B6	
IN<61>	A5	
IN<62>	A7	
IN<63>	A6	
VDD_PA	F6	Power Supply - VDD_PA
VDD_PA	F7	
VDD_PA	F8	
VDD_PA	G6	
VDD_PA	G7	
VDD_PA	G8	
VDD_PA	L6	
VDD_PA	L7	
VDD_PA	M6	
VDD_PA	M7	
VDD_PA	N6	
VDD_PA	N7	
VDD_PA	P6	
VDD_PA	P7	
VDD_PA	V6	
VDD_PA	V7	
VDD_PA	V8	
VDD_PA	W6	
VDD_PA	W7	
VDD_PA	W8	
DataROChn0_15N	Z20	I/O Digital Differential (1GHz)
DataROChn0_15P	Z19	
clk_DataROChn0_15N	AC24	
clk_DataROChn0_15P	AC23	
DataROChn16_31N	U24	

DataROChn16_31P	U23	
clk_DataROChn16_31N	T24	
clk_DataROChn16_31P	T23	
DataROChn32_47N	G24	
DataROChn32_47P	G23	
clk_DataROChn32_47N	F24	
clk_DataROChn32_47P	F23	
DataROChn48_63N	C20	
DataROChn48_63P	C19	
clk_DataROChn48_63N	B20	
clk_DataROChn48_63P	B19	
TDC_Hit_N	A18	
TDC_Hit_P	A17	
NC	A20	
NC	A19	
TDC_CLK320_N	A13	
TDC_CLK320_P	A14	
clk320M_N	A23	
clk320M_P	A24	
valevent_n	A11	I/O Digital Differential (50MHz)
valevent_p	A12	
NC	AC20	
NC	AB20	
NC	AC22	
NC	AB22	
NC	AB24	
NC	AA22	
NC	AA24	
NC	Z22	
NC	Z24	
NC	Y22	
NC	Y24	
NC	W22	
NC	W24	
NC	V22	
NC	U22	
NC	T22	
NC	R22	
NC	K22	
NC	K24	
TDC_cal_coarse<3>	J22	
NC	J24	
TDC_cal_coarse<1>	H22	
NC	E24	
NC	D24	
NC	C24	
NC	B24	
OvfTimeCptChn48_63N	A24	
NC	AB19	
OvfTimeCptChn0_15N	AA19	
NC	AC21	
NC	AB21	
NC	AB23	
NC	AA21	
NC	AA23	
NC	Z21	
NC	Z23	
NC	Y21	
NC	Y23	
NC	W21	
NC	W23	
NC	V21	
OvfTimeCptChn16_31N	V23	
NC	U21	
NC	T21	
NC	R21	
NC	K21	
NC	K23	
TDC_cal_coarse<2>	J21	
NC	J23	
TDC_cal_coarse<0>	H21	
OvfTimeCptChn32_47N	H23	
NC	E23	
NC	D23	
NC	C23	
NC	B23	
VDD	F9	Power Supply - VDD
VDD	F10	
VDD	F11	
VDD	G9	
VDD	G10	
VDD	G11	
VDD	H6	
VDD	H7	

VDD	J6		VDD	U6	
VDD	J7		VDD	U7	
VDD	K6		VDD	V9	
VDD	K7		VDD	V10	
VDD	R6		VDD	V11	
VDD	R7		VDD	W9	
VDD	T6		VDD	W10	
VDD	T7		VDD	W11	

Table 5 – TEMPOROC2 ASIC pin list

TEMPOROC2 ASIC floorplan & packaging

Preliminary mechanics give a naked die size of 4.88mm*11.18mm including scribe line giving a die area of 54 mm2. The ASIC has 515 bump pads which will be bonded to BGA substrate.

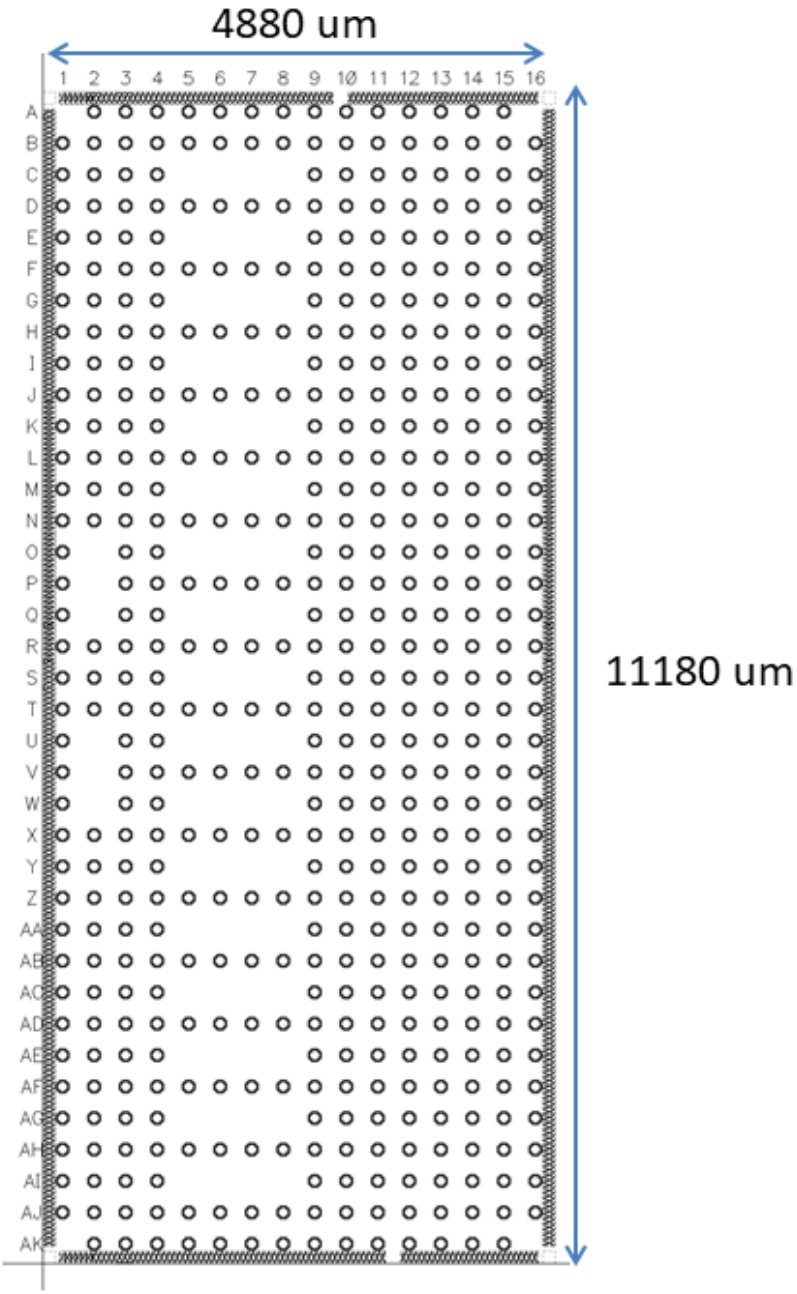


Figure 9 - Preliminary padring and form factor

Power supply

The core of the ASIC is power by 1.2V and power supplies are separated in several zone for reducing EMC influence from various section of the ASIC. It is recommended to at least separate the digital power supply from the analog power supply and to use decoupling capacitors for stabilizing & filtering the power supply.

Pin Name	Pin Type	Description	Connected to
VDD_PA	Power Supply	Analog power supply	1.2V
VDD	Power Supply	Input stage power supply	1.2V
DVDD	Power Supply	Digital power supply	1.2V
GND	Ground	Ground	0

Input connection

The input pins are solely reserved for the detector inputs (SiPM). Short distance of traces for routing the input signal is highly recommended. Suggestion of the input connection is shown in Figure 10.

Pin Name	Ball Map	Description	Connected to
In<0:63>	Various location (refer to Table 5)	Connection to detector	Detector anodes or cathodes

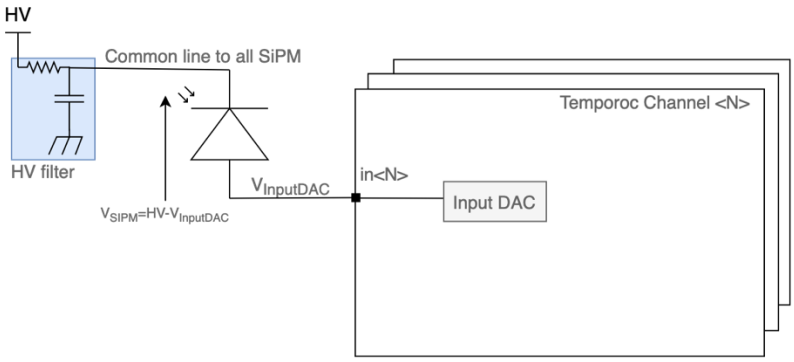


Figure 10 - SiPM connection suggestion

Biasing & debugging connections

Biasing pins are mostly optional I/Os which are available for debugging and modifying analog section biasing if required. It could be left open or connected to decoupling capacitors in most cases. However, if a biasing modification is required, it is also possible to connect the pin to resistor-based voltage divider (refer **Erreur ! Source du renvoi introuvable.**). The expected DC value of each pin can be found in Table 2. Additionally, the proposed connection for debugging pins (PDHG_P, PDHG_N, PDLG_P, PDLG_N,analogProbe_Out & in_ctest) is shown in **Erreur ! Source du renvoi introuvable.** and **Erreur ! Source du renvoi introuvable.**.

Pin Name	Ball Map	Description	Connected to
analogProbe_Out	L22	Analog Probe monitoring output	Analog buffer & oscilloscope
PDHG_P	L23	High Gain Shaper Peak detector output (p)	ADC/ Analog buffer /Oscilloscope
PDHG_N	L24	High Gain Shaper Peak detector output (n)	ADC/ Analog buffer /Oscilloscope
PDLG_P	P23	Low Gain Shaper Peak detector output (p)	ADC/ Analog buffer /Oscilloscope
PDLG_N	P24	Low Gain Shaper Peak detector output (n)	ADC/ Analog buffer /Oscilloscope
VinP_ADC	AC10	Test ADC input (p)	Analog Input
VinN_ADC	AC11	Test ADC input (n)	Analog Input
ibp_paHg	M1	Input stage HG shaper pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
ibp_paT	N1	Input stage Time Trigger pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
Ibi_rx	C3	Input stage differential driver bias	Not connected, decoupling capacitor and/or voltage divider
Ibo_rx	D3	Output stage differential driver bias	Not connected, decoupling capacitor and/or voltage divider
vcp_aBuffer	E3	Analog buffer amp P cascode	Decoupling capacitor and/or voltage divider
vcn_aBuffer	F3	Analog buffer amp N cascode	Decoupling capacitor and/or voltage divider
vref_thresholdDacQ	G3	Charge Trigger threshold voltage reference	Decoupling capacitor and/or voltage divider
vref_thresholdDac	H3	Time Trigger threshold voltage reference	Decoupling capacitor and/or voltage divider
VthresholdQ	J3	Charge Trigger threshold	Decoupling capacitor

Vthreshold2	K3	Time Trigger threshold (high)	Decoupling capacitor
Vthreshold1	L3	Time Trigger threshold (low)	Decoupling capacitor
ibp_paLg	M3	Input stage LG shaper pre-amp bias	Not connected, decoupling capacitor and/or voltage divider
vref_1v	N3	1V low impedance ref output	Decoupling capacitor and/or voltage divider
vbg	P3	Bandgap output	Decoupling capacitor and/or voltage divider
vbias_1v	R3	1V low impedance bias output	Decoupling capacitor and/or voltage divider
vref_inDac	T3	Input DAC reference voltage	Decoupling capacitor and/or voltage divider
vcasc_paT	U3	Pre-amp cascode voltage	Decoupling capacitor and/or voltage divider
vcasc_paQ	V3	Shaper pre-amp cascode voltage	Decoupling capacitor and/or voltage divider
vref_sh	W3	Shaper reference voltage	Decoupling capacitor and/or voltage divider
vcp_pdetect	Y3	Peak detector P cascode	Decoupling capacitor and/or voltage divider
vcn_pdetect	Z3	Peak detector N cascode	Decoupling capacitor and/or voltage divider
vref_delay	AA3	Delay cell reference voltage	Decoupling capacitor and/or voltage divider
vcasc_rx	B11	LVDS receiver cascode	Decoupling capacitor and/or voltage divider
in_ctest	B7	Charge injection input	Waveform generator or pulser
Vth_delay	AB7	Delay cell threshold output	Decoupling capacitor

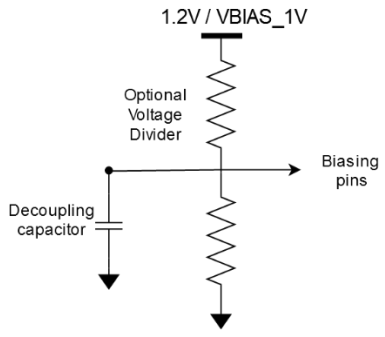


Figure 11- Proposed connection for biasing points.

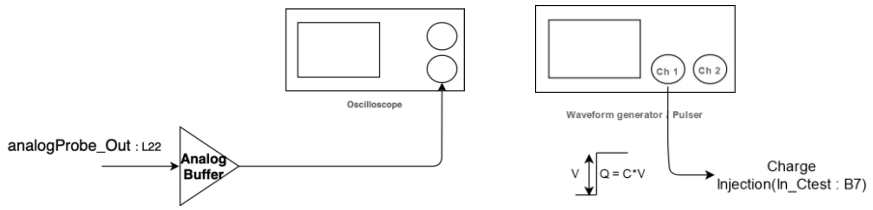


Figure 12 - Proposed connection for analogProbe_Out (Left figure) and In_Ctest (Right figure)

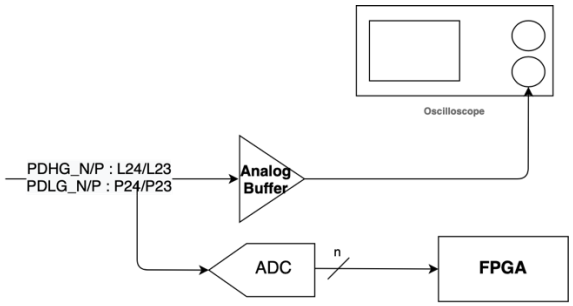


Figure 13- Proposed connection for PDHG_N/P and PDLG_N/P

Digital connections

The digital I/Os are divided into 4 types : open collector, single-ended, bidirectional and differential (CLPS[2]). The proposed connection for bidirectional and differential pins are shown in **Erreur ! Source du renvoi introuvable.**. The pins are active high unless it is stated to be active low. Additionally, suggestions of connecting various digital I/Os are also shown in **Erreur ! Source du renvoi introuvable.** and **Erreur ! Source du renvoi introuvable.**.

Pin Name	Ball Map	Description	Connected to
CHIP_ID<0:3>	M23,N24, N23, N22	Chip ID for I2C (TEMPOROC2 CHIP_ID<0:3> = "0001") : Single Ended	FPGA
clk_sm_i2c	A10	Clock for I2C slave core : Single Ended	FPGA
errorb_sc	AC13	Slow Control reset error : Open Collector	FPGA
ck_read	AC9	Clock for read register : Single Ended	FPGA
rstn_read	AC12	Low level reset for read register : Single Ended	FPGA
resetn	AC14	Low level reset for digital part : Single Ended	FPGA
rstn_probe	AC13	Low level reset for probe (analog debugging & signal monitoring) : Single Ended	FPGA
Power_On	A8	Power ON signal for sequentially powering on/off the ASIC analog part : Single Ended	FPGA
Resetn_I2C	B9	Low level reset for I2C slave core : Single Ended	FPGA
SCL	B10	SCL line for I2C : Bidir	FGPA with 47k Ohm pull up resistor to 1.2V
SCA	A9	SDA line for I2C : Bidir	FGPA with 47k Ohm pull up resistor to 1.2V
TrigT_L_mux_Out	B15	Multiplexed Time trigger output (Low threshold) : Single Ended	FPGA/Oscilloscope
TrigT_T_H_mux_Out	B16	Multiplexed Time trigger output (High threshold) : Single Ended	FPGA/Oscilloscope

[2] CLPS stand for CERN Low Power Signaling. It is not a fairly common digital I/Os standard. The common voltage is set at 0.6V with signal swing of 300mV.

TrigQ_mux_Out	B17	Multiplexed Charge trigger output : Single Ended	FPGA/Oscilloscope
NORTrigQ_Out	C15	OR output for Charge trigger : Open Collector	FPGA/Oscilloscope
NORTrigQ_RS_out	C16	OR output for latched Charge trigger : Open Collector	FPGA/Oscilloscope
NORTrigT_L_RS_Out	A15	OR output for latched Time trigger (Low threshold) : Open Collector	FPGA/Oscilloscope
NORTrigT_H_RS_Out	A16	OR output for latched Time trigger (High threshold) : Open Collector	FPGA/Oscilloscope
DigitalProbe_Out	B18	Multiplexed digital probe(monitoring) output : Single Ended	FPGA/Oscilloscope
conv_systRO	R24	Digital section conversion start : Single Ended	FPGA
hold_ext	P22	External hold signal for peak detector : Single Ended	FPGA/Waveform generator
enable_RO	R23	Digital section conversion enable : Single Ended	FPGA
trig_ext	P21	External trigger: Single Ended	FPGA/Waveform generator
rstn_latch	L21	Low level reset for trigger latch : Single Ended	FPGA
Ovf_time_cpt<0:3>	AA20,V24, H24,D20	Coarse time counter overflow : Single Ended	FPGA
DataROChn0_15N/P	Z20/Z19	Channel 0-15 data output : CLPS	FPGA
clk_DataROChn0_15N/P	AC24/AC23	Channel 0-15 data clock output : CLPS	FPGA
DataROChn16_31N/P	U24/U23	Channel 15-31 data output : CLPS	FPGA
clk_DataROChn16_31N/P	T24/T23	Channel 15-31 data clock output : CLPS	FPGA
DataROChn32_47N/P	G24/G23	Channel 32-47 data output : CLPS	FPGA
clk_DataROChn32_47N/P	F24/F23	Channel 32-47 data clock output : CLPS	FPGA
DataROChn48_63N/P	C20/C19	Channel 48-63 data output : CLPS	FPGA
clk_DataROChn48_63N/P	B20/B19	Channel 48-63 data clock output : CLPS	FPGA
clk320M_N/P	A23/A24	320MHz clock input : CLPS	FPGA
valevent_n/p	A11/12	Differential fast discriminator masking inputs : CLPS	FPGA

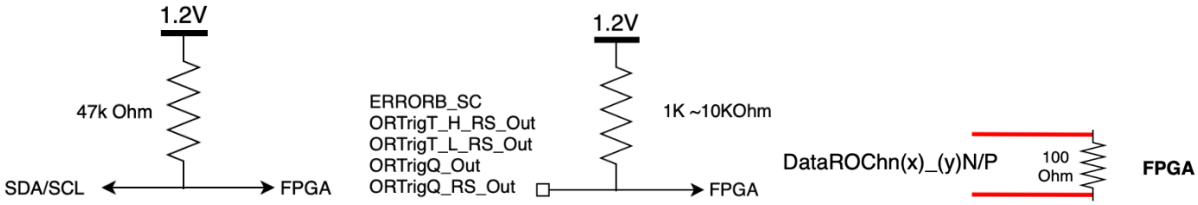


Figure 14 – Left : Proposed connection for SDA/SCL. Middle: Proposed connection for Open Collector connection. Right : Differential outputs connection.

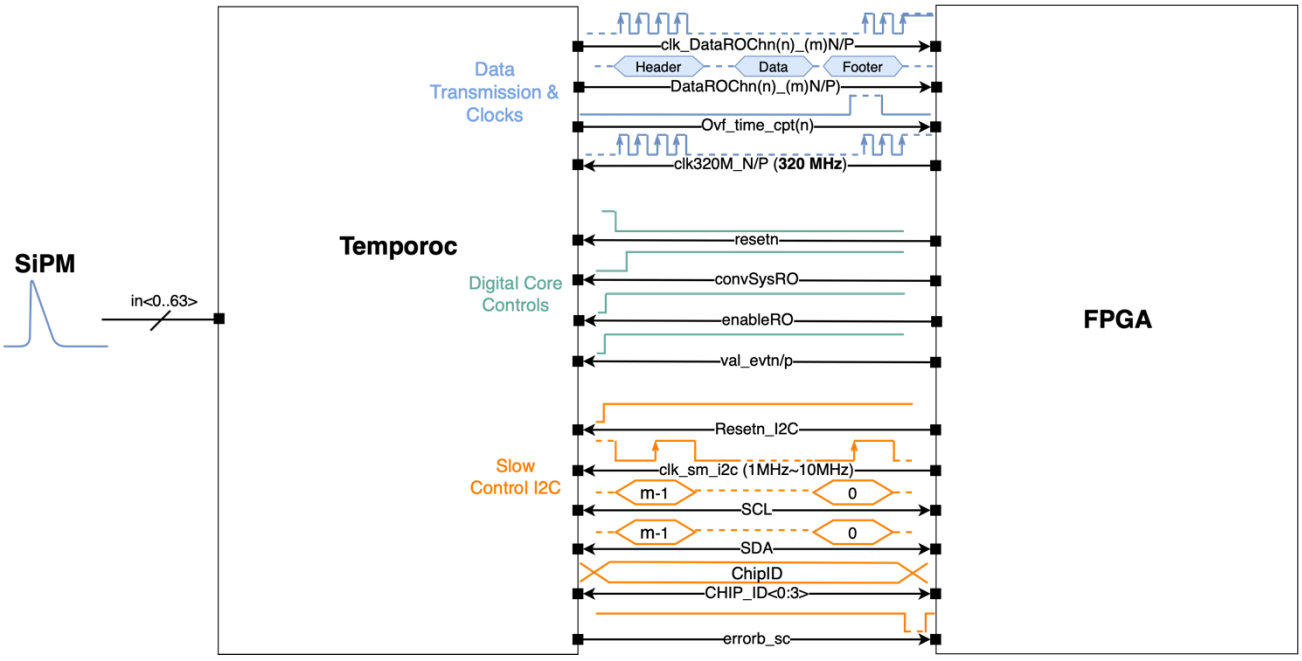


Figure 15 - Data Transmission, digital core controls and I2C for Slow Control connections suggestion

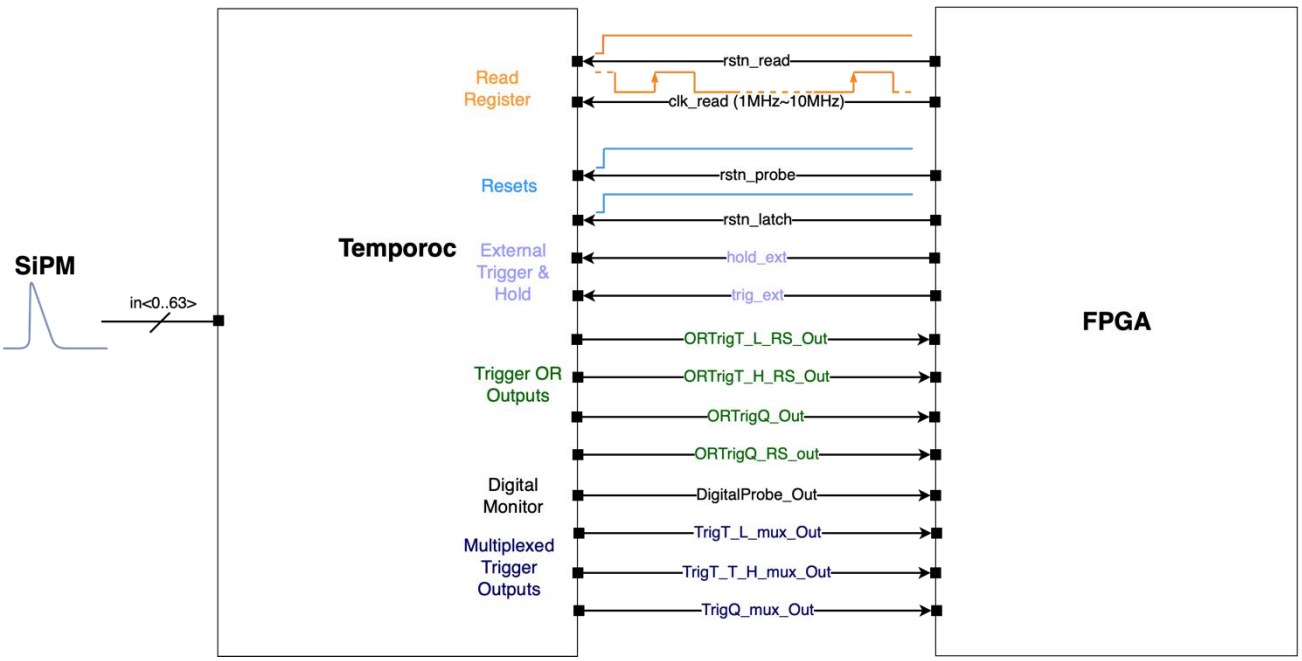


Figure 16– Read Register, resets, trigger outputs and Digital monitor connections suggestion

TEMPOROC2 analog operation

The analog part of TEMPOROC2 is composed of the input DAC, pre-amplifier for input signal discrimination & triggering, and finally two shapers (High Gain and Low Gain). Schematic diagram of the analog section is shown in **Erreur ! Source du renvoi introuvable.**.

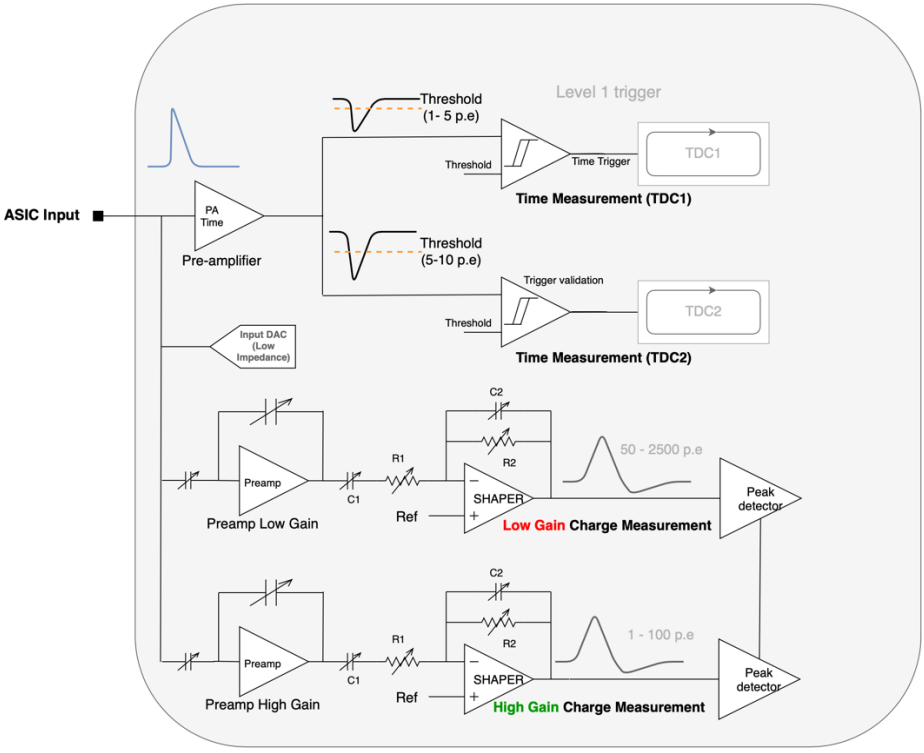


Figure 17 – TEMPOROC2 Analog Section

The input DAC can be used to setup the SiPM overvoltage, cannel per channel. This feature can be used to correct the detector not uniformity. An example the SiPM connection is illustrated in the Figure 10.
The input DAC value can be set through the following Slow Control bits:

- InDAC (Address : 0-63; Subadd : 2; Bits :7-0). Voltage span : 4 mV ~525mV. Step ~2mV.

This ASIC accepts only positive polarity inputs and the output of the pre-amp is fed into two discriminators. This pre-amp has a variable gain adjustment, accessible through Slow Control bits :

- patGain (Address : 0-63; Subadd : 2; Bits :5-0). Close-loop gain span: 8 (central bandwidth frequency = 331MHz) ~ 9.3 (central bandwidth frequency = 39MHz).

The first discriminator will generate Low threshold (Threshold1) Time Trigger output (TrigT_L). The second discriminator will be set with High Threshold (Threshold2) in order to produce a secondary Time Trigger output (TrigT_H). Threshold value for both triggers can be set from :256mV to 534mV with a step of 0.27mV. The Slow Control bits for both thresholds are as the following :

- (Threshold1, Address : 65; Subadd : 2; Bits :1-0 & Subadd : 1; Bits :7-0). Voltage span : 256mV ~ 534mV. Step = 0.27mV.
- (Threshold2, Address : 65; Subadd : 3; Bits :3-0 & Subadd : 2; Bits :7-2). Voltage span : 256mV ~ 534mV. Step = 0.27mV.

The pre-amp DC level value is set about 490mV. The schematic diagram of the pre-amp is shown in **Erreur ! Source du renvoi introuvable.**.

Both of the trigger outputs are sent into two separate Vernier TDCs. This TDC will operate only once a trigger signal is received and will provide the Fine Time for time tagging the incoming input signal.

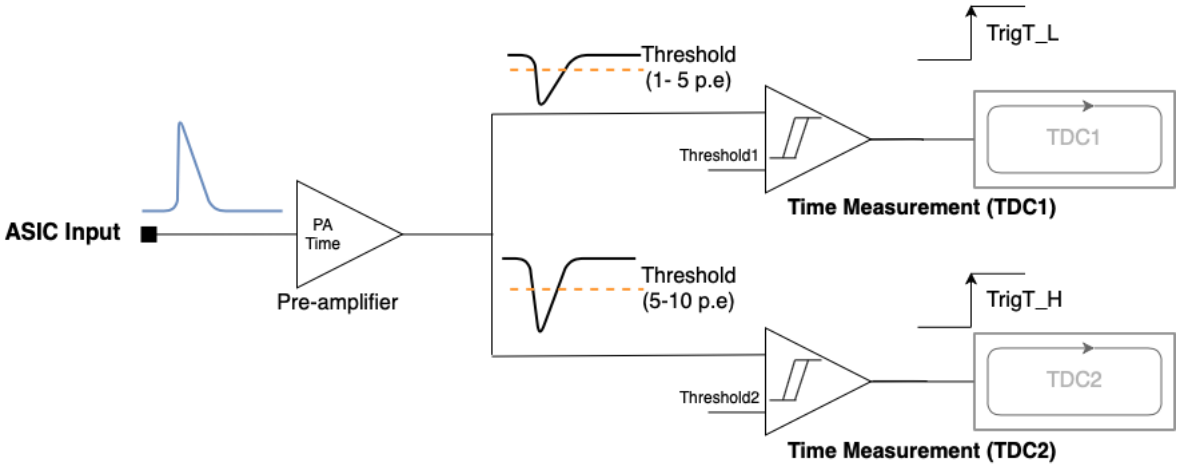


Figure 18- Pre-amp and Time Trigger block diagram

This ASIC also embeds two shapers (High Gain & Low Gain) which are connected directly to the ASIC input. Both of the shapers have a pre-amp stage & variable shaping time. The shapers pre-amp can be adjusted channel per channel through Slow Control bits hgGain for High Gain shaper and lgGain for Low Gain shaper. The Slow Control bits for adjusting the shaper pre-amp gain are the following :

- hgGain (Address : 0-63; Subadd : 3; Bits :3-0). Gain span : 5 ~ 78. Step = 4.5
- lgGain (Address : 0-63; Subadd : 3; Bits :7-4). Gain span : 0.5 ~ 7.8. Step = 0.45.

The shaping time for both shapers, can be adjusted using the following Slow Control bits: tauHG (Address : 0-63; Subadd : 4; Bits :7-4) for High Gain shaper and tauLG (Address : 0-63; Subadd : 4; Bits :3-0) for Low Gain shaper. The Slow Control bits for adjusting the shaper shaping time :

- tauHG (Address : 0-63; Subadd : 4; Bits :7-4). Shaping time span : 20ns ~300ns. Step = 20ns
- tauLG (Address : 0-63; Subadd : 4; Bits :3-0) . Shaping time span : 20ns ~300ns. Step = 20ns

Each of the shaper output will be sent to a peak detector cell which will be connected to ADCs for amplitude (charge) measurements. Additionally, Low Gain shaper signal could be used to generate Charge Trigger (TrigQ) which will be the highest threshold trigger in term of the input signal. The threshold can be set through the following Slow Control bits :

- ThresholdQ (Address : 65; Subadd : 4; Bits :5-0 & Subadd : 3; Bits :7-4). Voltage span : 76mV ~ 1193mV. Step = 1mV

The DC level of Low Gain shaper is set about 90mV. An illustration of the shapers is depicted in **Erreur ! Source du renvoi introuvable.**.

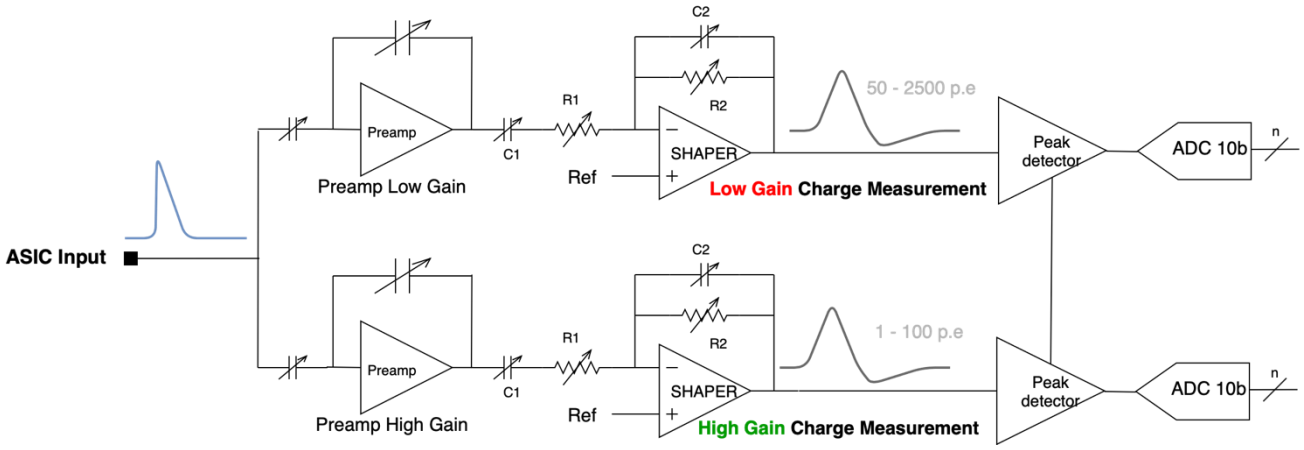


Figure 19- Shaper block diagram

Peak detectors are used to sample the amplitude of the shaper signal by conserving the peak of this signal. The operation of the peak detector is illustrated in the **Erreur ! Source du renvoi introuvable.**. Shaper output will be fed into peak detector cell and Time or Charge trigger (localized or global) will be used to enable this peak detection cell. Local trigger denotes the trigger generated within the hit channel and global ASIC trigger denotes the OR output of any trigger in the ASIC. This selection can be done with the following Slow Control bits :

- Sel_trig (Address : 65; Subadd : 11; Bits :1-0). The following triggers can be selected :
  - “00” Global ASIC trigger (Refer to Slow Control “selGlobalTrigger” Address : 66; Subadd : 3; Bits :1-0)
  - “01” Local Low Threshold Time Trigger (default)
  - “10” Local High Threshold Time Trigger
  - “11” Local Charge Trigger

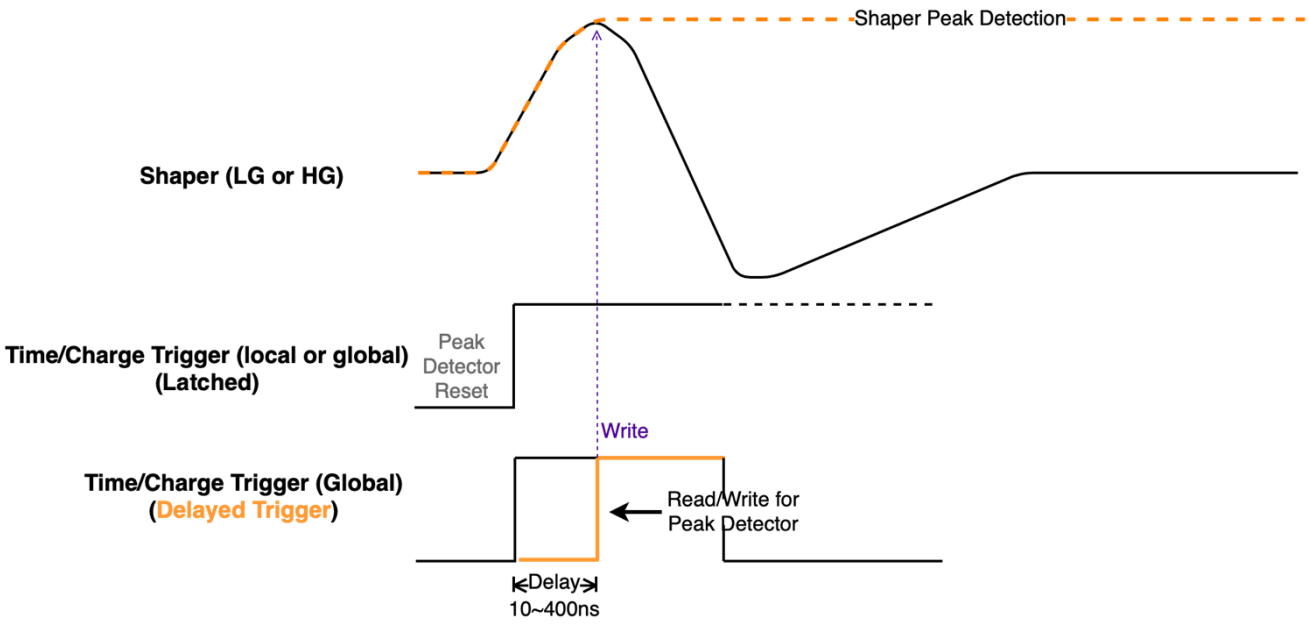


Figure 20 - Illustration of peak detection in TEMPOROC

Additionally, a delay cell (at ASIC level) is used to generate a Read/Write signal for holding the peak amplitude before sending it for data conversion through a 10-bit SAR ADC. This delay cell will take as input the trigger used for enabling the peak detector (Slow Control bits : Sel_trig (Address : 65; Subadd : 11; Bits :1-0)). Then a delay can be applied to this trigger using the following Slow Control bits :

- Delay (Address : 65; Subadd : 10; Bits : 7-0). Delay span : 3ns~832ns. Step = 3.3ns

TEMPOROC2 trigger operation

TEMPOROC2 trigger offers a few options, mainly due to the clustering configuration of the ASIC. First of all, it should be noted that, the Time Triggers (Low & High threshold) are used for two purposes: time tagging through TDC and enabling data readout/transmission. This section will cover the usage of the triggers within a cluster of 16 channels in conjunction with data readout and transmission.

The triggers are intrinsically linked to the digital part as the digital will perform the data conversion (ADCs & TDCs) and transmit the data. This ASIC offers trigger summing options where the threshold of the sum can be set through Slow Control bits :

- Nb_trigger (Address : 66; Subadd : 5; Bits : 4-0). Threshold span: 0 ~ 15. Step = 1

The summing option is available for both Time Triggers (TrigT_L and TrigT_H).

Additionally, there is also delay management which is embedded within the triggering scheme. Each Time Trigger output has a dedicated delay cell which can be set through Slow Control : Delay_ClusterL for Low Threshold Time Trigger (TrigT_L) and Delay_ClusterH for High Threshold Time Trigger (TrigT_H). For both delay cells, the delay can be set from 2ns up to 29ns with a step of 0.1ns. The Slow Control bits for the delay :

- Delay_ClusterL (Address : 65; Subadd : 8; Bits : 7-0) : Delay span : 1ns ~67ns. Step = 0.26ns
- Delay_ClusterH (Address : 65; Subadd : 8; Bits : 7-0) : Delay span : 1ns ~67ns. Step = 0.26ns

The delay output will be sent to the digital part to annotated the timeout (or trigger sum window) in case the trigger sum doesn't reach the required threshold. However, this delay can be bypassed with Charge Trigger (TrigQ) if it is required. This can be done with Slow Control bit, EN_trigQ_validation (Address : 64; Subadd : 14; Bits : 5).

The digital part, includes the trigger summing part and also receives the control signals such as other cluster sync input and delay output from the analog side. In return the digital part will send out the cluster sync output, data transmission and reset signal to the analog side. The reset of the part of the analog section is managed by separately within a reset management system which takes in account the other cluster sync within the ASIC. The block diagram of the triggering scheme of this ASIC is shown in **Erreur ! Source du renvoi introuvable.**.

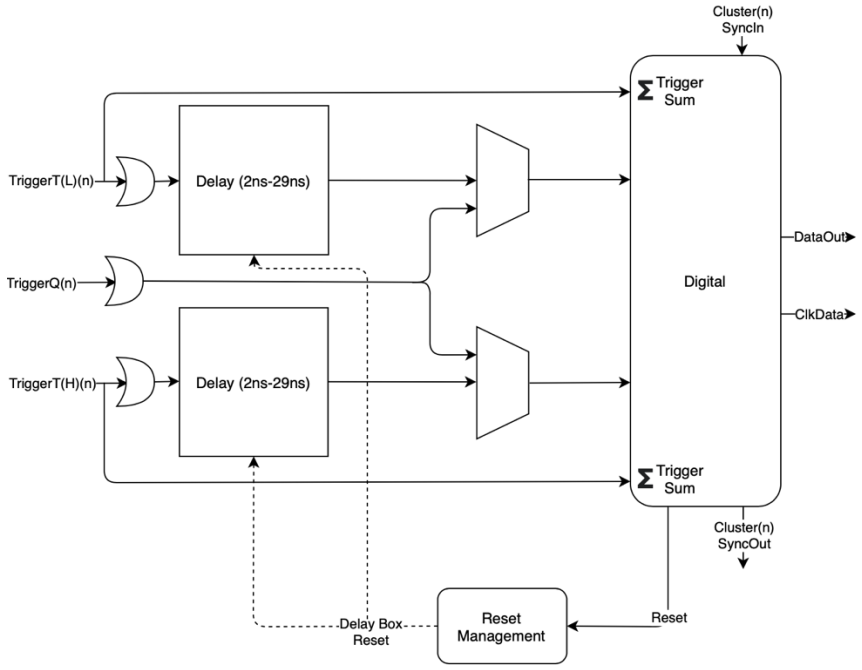


Figure 21 – TEMPOROC2 triggering scheme block diagram

Erreur ! Source du renvoi introuvable. illustrates the flow of the default ASIC configuration of the t riggering scheme. This scheme starts with the Time Triggers (Low and High thresholds) received and it will start the delay cell according the delay set. Simultaneously the triggers will be sent to the digital part for summation. In the event where there is sufficient number of triggers within the delay set or Cluster sync signal received, the digital part will proceed to data conversion and transmission. Otherwise, the ASIC will go back to standby state. It should be noted that any Time Triggers could initiate the data transmission but the it is expected that the Time Trigger with lowest threshold will

take over between two triggers. For setting the ASIC correctly, the following Slow Control bits has to be configured or left at default value :

- Nb_trigger (Address : 66; Subadd : 5; Bits : 4-0) . Default value = 4
- Delay_ClusterL (Address : 65; Subadd : 8; Bits : 7-0) . Default value = 19ns
- Delay_ClusterH (Address : 65; Subadd : 8; Bits : 7-0) . Default value = 19ns

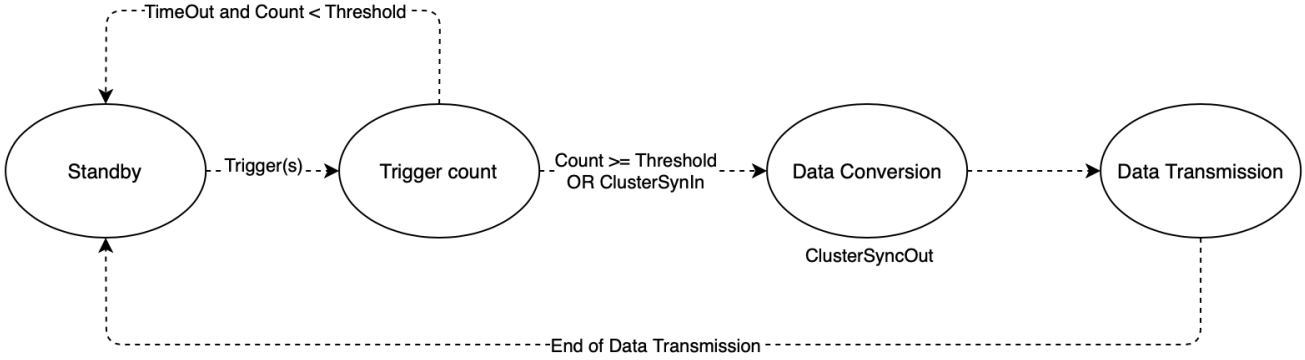


Figure 22- Default triggering & data transmission scheme

In the case of users prefer to have a simplified readout system (**Erreur ! Source du renvoi introuvable.**) which can be initiated with any incoming Time Trigger, the count threshold can be set to 0 and the delay can be set to max value. Of course, the data conversion could also be initiated trough the other cluster sync signal. The following Slow Control bits have to be set in this scheme:

- Nb_trigger (Address : 66; Subadd : 5; Bits : 4-0) . Set to min value = 0
- Delay_ClusterL (Address : 65; Subadd : 8; Bits : 7-0) . Set to max value = 29ns
- Delay_ClusterH (Address : 65; Subadd : 8; Bits : 7-0) . Set to max value = 29ns

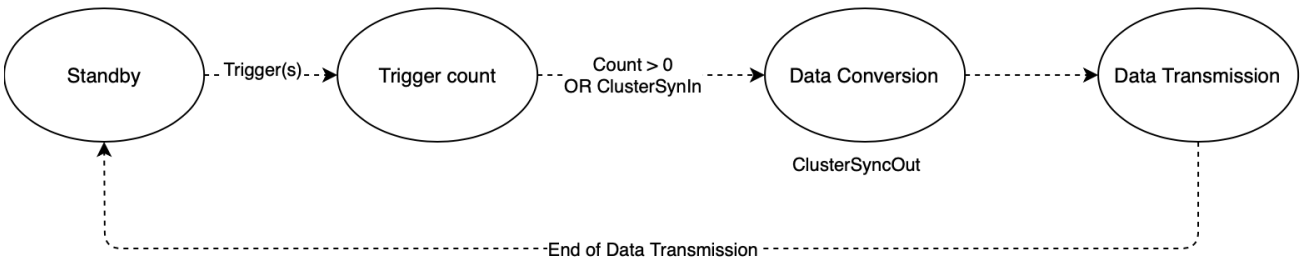


Figure 23- Simplified readout & triggering scheme

Another readout scheme available is through Charge Trigger (**Erreur ! Source du renvoi introuvable.**), where this trigger can be used to replace the delayed trigger. In this case the following Slow Control bit has to be set :

- EN_trigQ_validation (Address : 64; Subadd : 14; Bits : 5). Set to = '1'

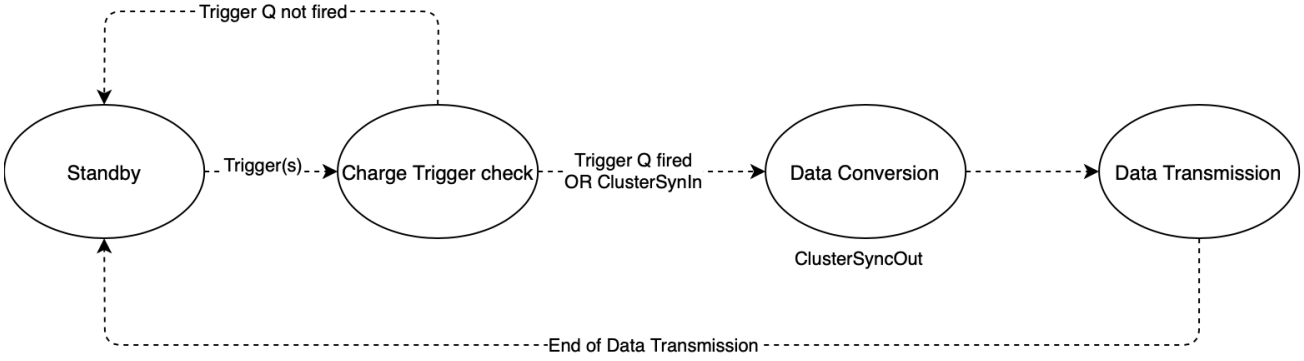


Figure 24- Simplified readout with charge validation scheme

It should be noted all the triggers should be in latched mode and not masked. Several Slow Control bits and fast masking input (ValEvt) need to be verified as the following :

- maskTLn (Address : 0-63; Subadd : 7; Bits : 4). Set to = '1'
- maskTHn (Address : 0-63; Subadd : 7; Bits : 3). Set to = '1'
- maskTQn (Address : 0-63; Subadd : 7; Bits : 3). Set to = '1'
- valevent_n/p. Ballout A11/A12. Input set to High level

TEMPOROC2 digital operation

As the digital is fully automated, one of the main features is the ability to convert and transmitting various type of data. The digital part can be operated under several readout mode. This ASIC embeds two 10-bit SAR ADCs (for charge measurement) and two TDCs (for Fine Time). Each of the ADCs is connected to High Gain Shaper and Low Gain Shaper outputs respectively. On the other hand, the TDCs are connected to each of the pre-amp triggers : High Threshold Time Trigger and Low Threshold Time Trigger. Operating the digital part also requires the digital I/Os to be connected correctly. Suggestion of the digital I/Os connections can be seen in **Erreur ! Source du renvoi introuvable.**. The following I/Os has to be set correctly on order two operate the digital part :

- clk320M_N/P (A23/A24) : 320MHz differential clock inputs, preferably a low jitter clock source
- resetn (AC14) : Low level reset for digital part, needs to be in High level.
- enable_RO (R23) : Digital section conversion enable, required to be in High level.
- conv_systRO(R24) : Digital section conversion start, required to be in High level.

The following bloc diagram illustrate in **Erreur ! Source du renvoi introuvable.** coarsely different functions of the digital core:

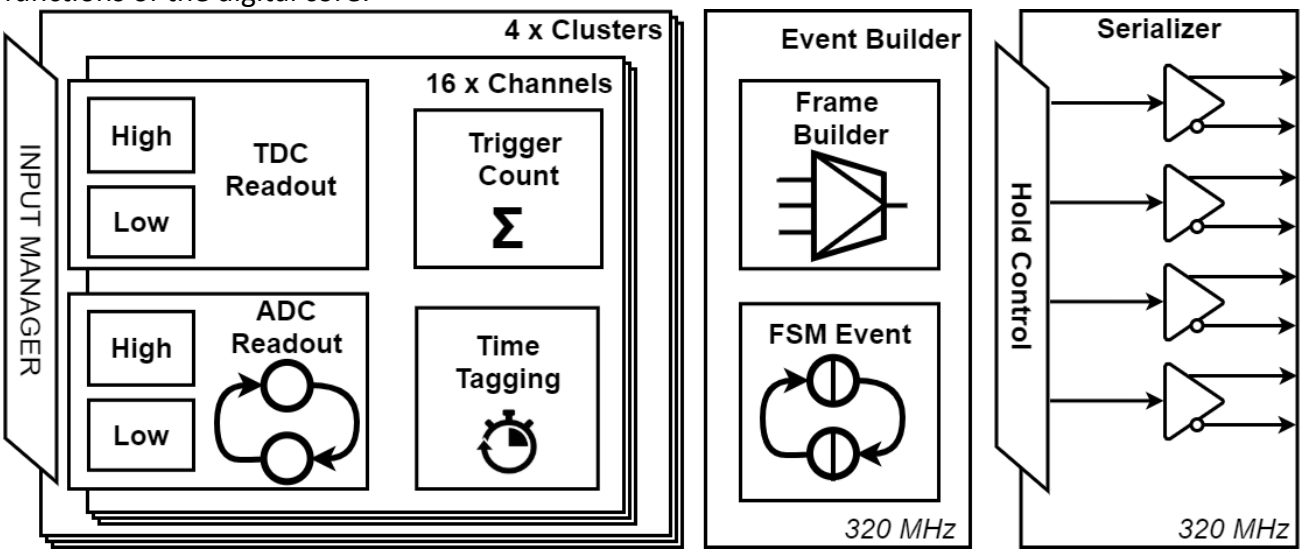


Figure 25 - Bloc diagram of the digital core of TEMPOROC2.

Depending on users preference and needs, the data conversion and output will be based on the Slow Control (ModeRO : Address : 66; Subadd : 4; Bits :4-0) selection as listed in Table 6.

Slow Control ModeRO	Readout Mode	Readout Data									Expected data length (bits)
		Test	Trigger Low	Trigger High	HADC	LADC	HTDC	LTDC	HCPT	LCTP	
"01111"	Full ADC & TDC readout (Default readout mode)				√	√	√	√	√	√	1042

“01010”	High Gain Shaper ADC & High Threshold Trigger TDC				√		√		√		530
“00101”	Low Gain Shaper ADC & Low Threshold Trigger TDC					√		√		√	530
“01100”	High & Low Gain Shapers ADC				√	√			√	√	466
“01000”	High Gain Shaper ADC				√				√		242
“00100”	Low Gain Shaper ADC					√				√	242
“00011”	High & Low Threshold Trigger TDC						√	√			722
“00010”	High Threshold Trigger TDC						√		√		370
“00001”	Low Threshold Trigger TDC							√		√	370
“01001”	High Gain Shaper ADC & Low				√			√	√	√	594

	Threshold Trigger TDC										
“00110”	Low Gain Shaper ADC & High Threshold Trigger TDC					√	√		√	√	594
“11111”	Hit	√	√	√							50
“10000”	Test	√									1042

Table 6 – TEMPOROC2 Digital Readout Mode

Full data frame of the readout is shown in **Erreur ! Source du renvoi introuvable.** which is also correspond to the Slow Control bits : ModeRO =”01111” or the full ADC & TDC readout. The full data frame consists of the following section:

- Header section : 4-bit Header & 10-bit Global Coarse Time Counter
- Channel (n) data section : 10-bit High Gain Shaper ADC, 10-bit Low Gain Shaper ADC, 18-bit High Threshold Trigger TDC, 4-bit High Threshold Trigger Coarse Time Counter,18-bit Low Threshold Trigger TDC & 4-bit Low Threshold Trigger Coarse Time Counter
- Footer section : 4-bit Footer

It should be noted that following the Slow Control selection in Table 6, the Data Frame length will be reduced as well due to the omitted data (except for the data of the Header, Footer and Coarse Time Counters). This data reduction will also shorten the overall time required to transmit out the data.

Specifically, for Hit data readout, the transmitted data will contain only trigger information as shown in **Erreur ! Source du renvoi introuvable.**.

	HEADER		Channel 0						Channel N	Channel 15						FOOTER
	Header	GLOBAL	HADC	HTDC	HCPT	LADC	LTDC	LCPT	...	HADC	HTDC	HCPT	LADC	LTDC	LCPT	Footer
Cluster	4b	10b	10b	14b	4b	10b	14b	4b	56b x 14	10b	14b	4b	10b	14b	4b	4b
	14b		56b							56b						
	914															

Figure 26- Full frame of digital data readout

	HEADER		HIGH LEVEL			LOW LEVEL			FOOTER
	Header	GLOBAL	Chn 0	...	Chn 15	Chn 0	...	Chn 15	Footer
Cluster	4b	10b	1b		1b	1b		1b	4b
	14b		16b			16b			
	50b								

Figure 27 - Hit data of digital data readout

Digital States Machines

This following FSM illustrate in **Erreur ! Source du renvoi introuvable.** the global steps to send an event:

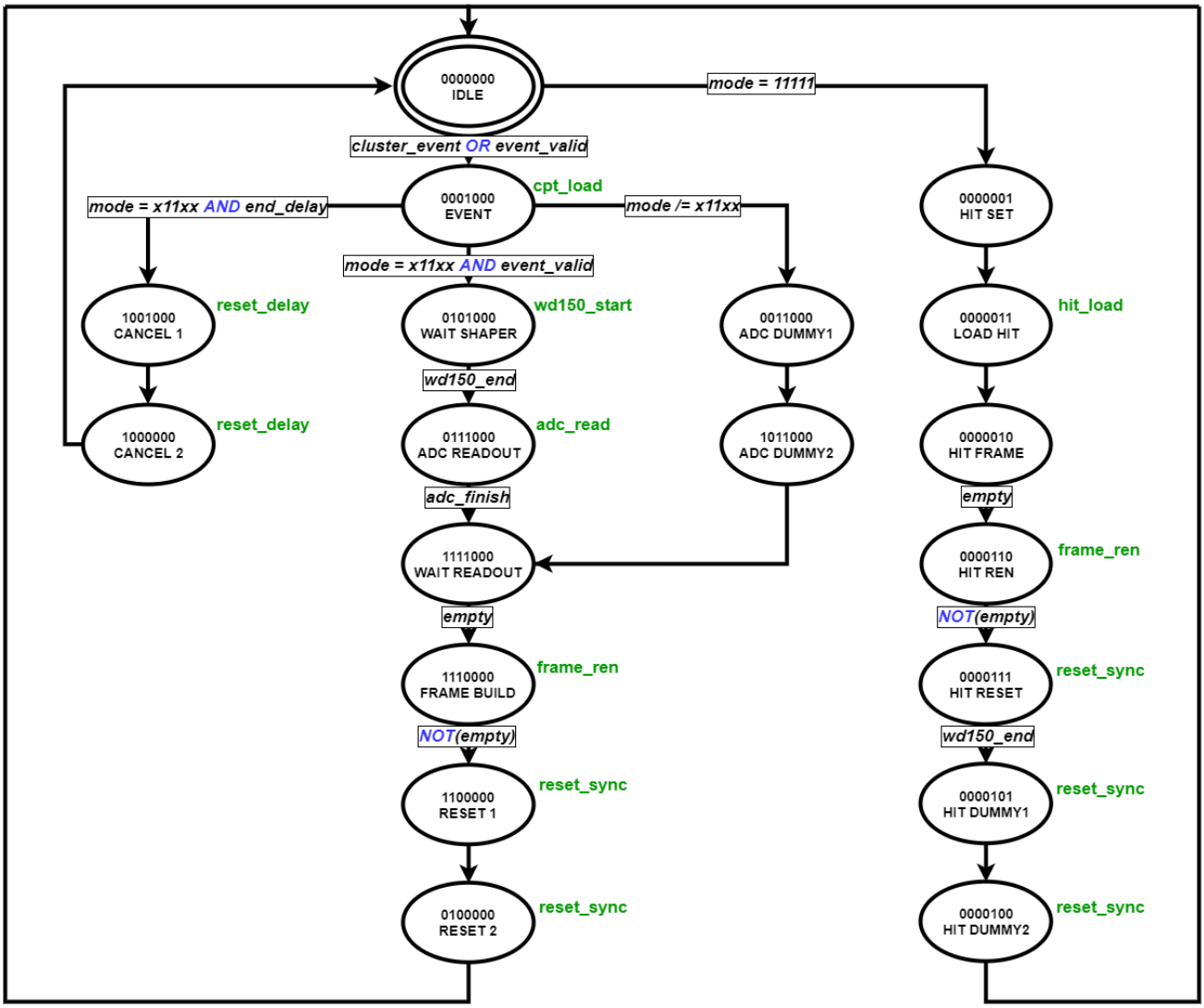


Figure 28 -Global digital FSM of TEMPOROC2.

The second FSM manage the conversion of each ADC channel if the user chooses to get Charge information of the event illustrate in **Erreur ! Source du renvoi introuvable.**.

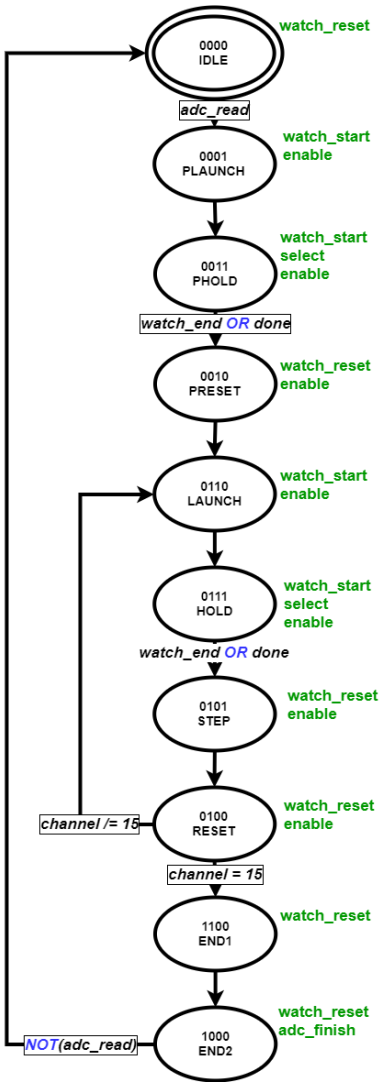


Figure 29 -FSM to convert and read each ADC channel.

For interpreting the data of the *Fine Time*, users can use the following formula :

Fine Time calculation	T = (Nslow-1) * Tslow - (Nfast-1) * Tfast + TdelaySlow – TdelayFast
Nfast	TDCData<13-7> (Gray Coded)
Nslow	TDCData<6-0> (Gray Coded)
Tfast	1.3177 ns (default – TBC pending measurement & calibration)
Tslow	1.35987 ns (default – TBC pending measurement & calibration)
TdelaySlow	0.807 ns (default – TBC pending measurement & calibration)
TdelayFast	0.788 ns (default – TBC pending measurement & calibration)

Coarse Time can be extracted from the header and also the channel data. Combining both of two data sets will give a 14-bit wide coarse counter data :

CoarseCounterData<13-4>	10-b Global data from Header
CoarseCounterData<3-0>	14-b HCPT/LCPT data from Channel data

Calculating the *Absolute Time* of the arrival signals will be as follows:
Absolute Time = (CoarseCounterData +1) *3.125ns – *Fine Time*

Interpreting the ADC data can be done as the following :

Amplitude calculation	V = Baseline + ADCData * LSB
Baseline	98mV (TBC pending measurement & calibration)
LSB	1mV (TBC pending measurement & calibration)

The timing diagram of the digital data transmission is shown in the following diagram.

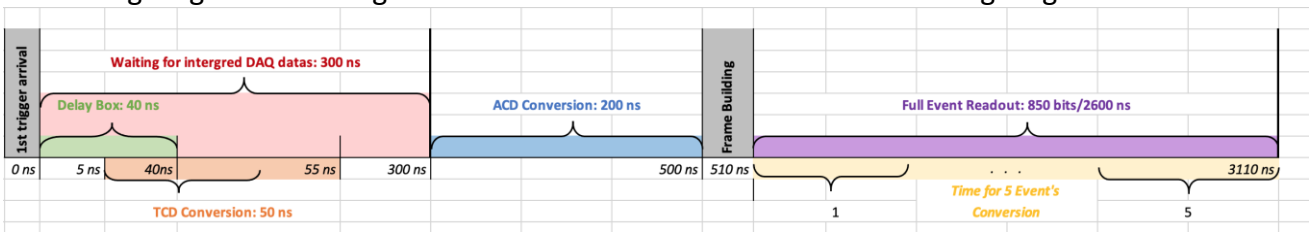


Figure 30 - Digital data conversion timing diagram

The whole timing diagram of the ASIC is illustrated in the **Erreur ! Source du renvoi introuvable.**. In this timing diagram, the ASIC is considered to have received sufficient number of events that will crossed the trigger counter threshold within the configured trigger counting windows. The data conversion and transmission are considered to be on default mode where all ADCs and TDCs will convert the data and all data will be sent out.

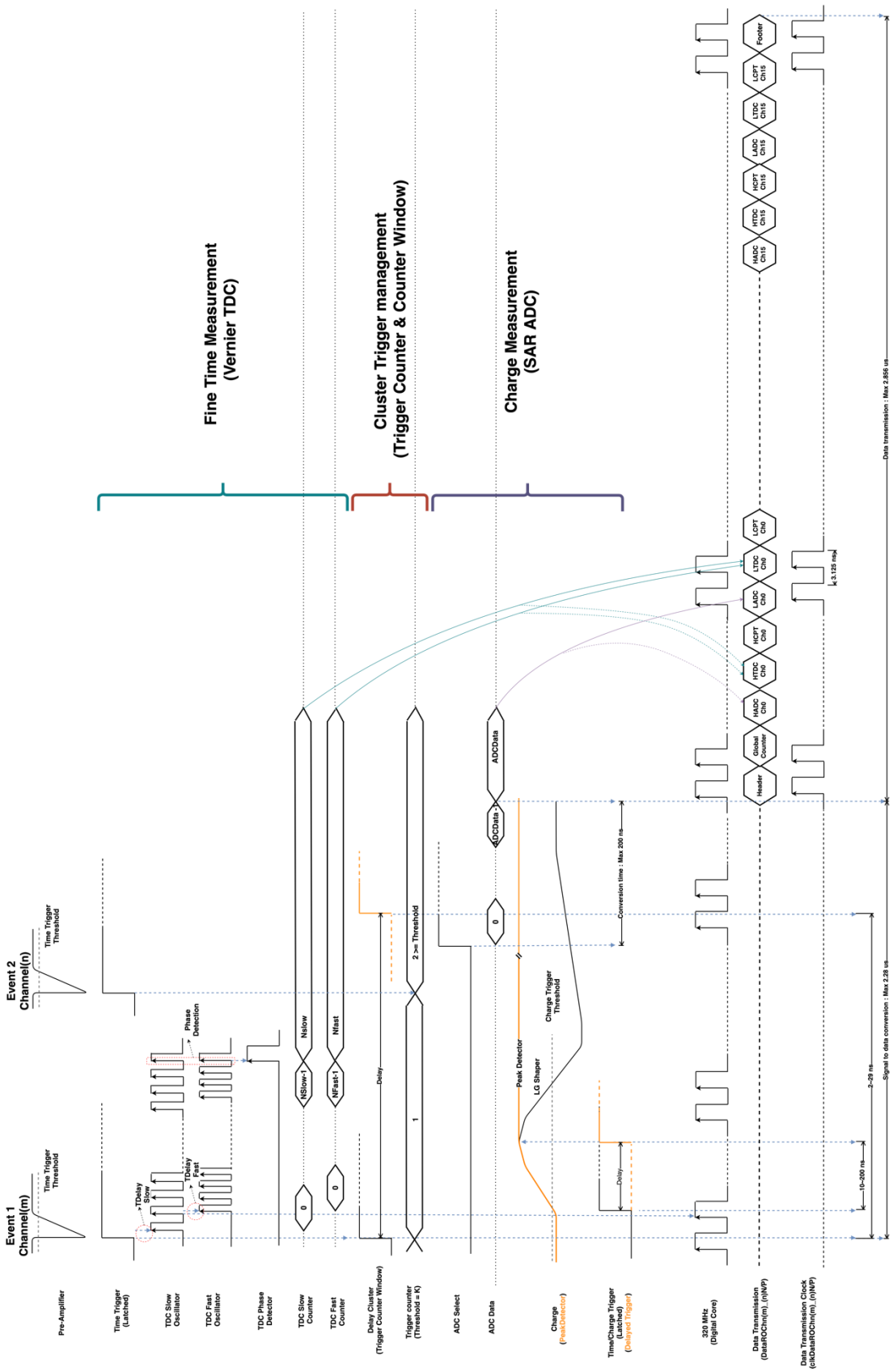


Figure 31 - Overall timing diagram from input signal to data conversion and transmission

ADC operation

TEMPOROC2 ASIC embeds two 10-bit SAR ADCs which are connected directly to the shaper peak detectors (**Erreur ! Source du renvoi introuvable.**). It should be noted, this ADC takes as input a differential signal. Therefore, for each shaper, the peak detector will output differential signal for the data conversion. The simplified diagram of this ADC is shown in **Erreur ! Source du renvoi introuvable.**.

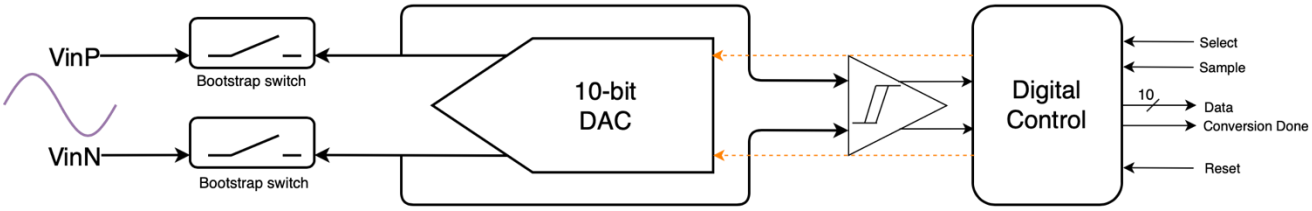


Figure 32 - 10-bit SAR ADC block diagram

The architecture of this ADC is fairly simple, the input signal is sampled with switch and a 10-bit DAC is used to adjust the signal before arriving at a discriminator. A differential discriminator is used to compare the signal and its outputs are sent to digital control module. This module will in turn control the DAC until this input signal amplitude is known. Externally, this ADC is controlled by the digital part of TEMPOROC, where the digital part would send out the ADC select signal, sample command and also reset command. In return the digital part would receive the 10-bit converted data and conversion done flag. This ADC is rated at 10MS/s and should be able to convert 1V of input signal span. Each cluster in this ASIC is equipped with two ADCs, one for each High Gain and Low Gain shapers.

TDC operation

The embedded TDC for Fine Time measurement is a Vernier TDC with ring oscillators. The simplified architecture of this TDC is shown in **Erreur ! Source du renvoi introuvable.**. The principle of this TDC is a slow oscillator is first started by incoming signal (in this ASIC: Time Trigger) and increments an associated counter. A second and faster oscillator is started by stop signal (in this ASIC: 320 MHz clock) which will also increment an associated counter. A phase detector circuit is then used to check the coincidence and to flag when both oscillators are in phase. Once both detectors are in phase, the counters will be stopped and a flag is sent to the digital part in order to recover the counters data. These data could be exploited in order to retrieve the Fine Time or the difference between Time Trigger and the 320 MHz clock edge.

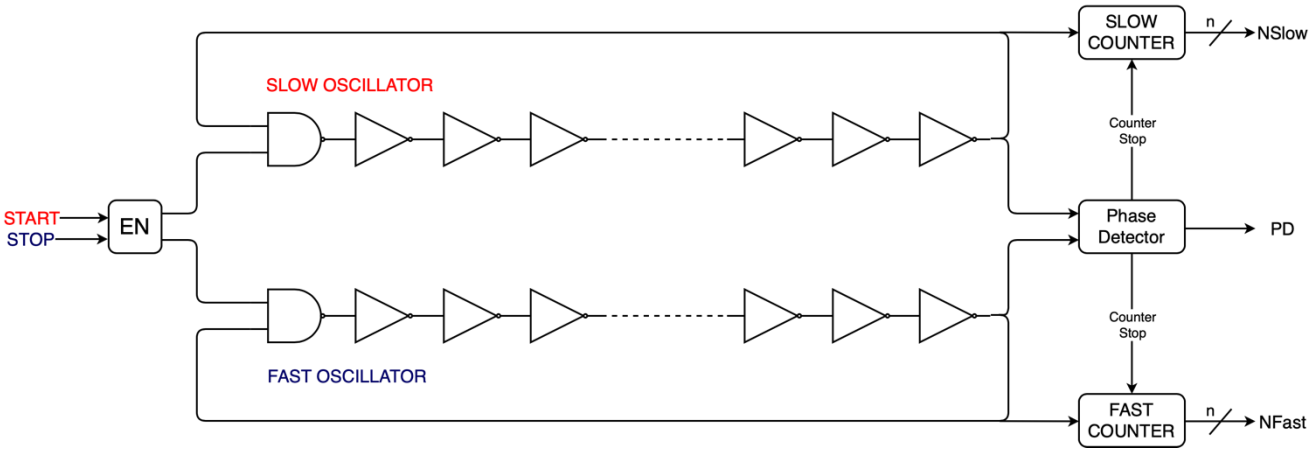


Figure 33 - TDC block diagram

In default ASIC configuration, the slow oscillator frequency is set at 735MHz and fast oscillator frequency is set at 760MHz. For both oscillators, the associated counters are 7-bit gray coded counter. This TDC has very minimal idle power consumption where the oscillators and counters will only be started once a trigger is received and stop the operation once a phase detection is available. Once the digital part has recovered the TDC data, a reset signal will be sent in order to put the TDC in standby mode again. The timing diagram of the TDC is shown in **Erreur ! Source du renvoi introuvable.**.

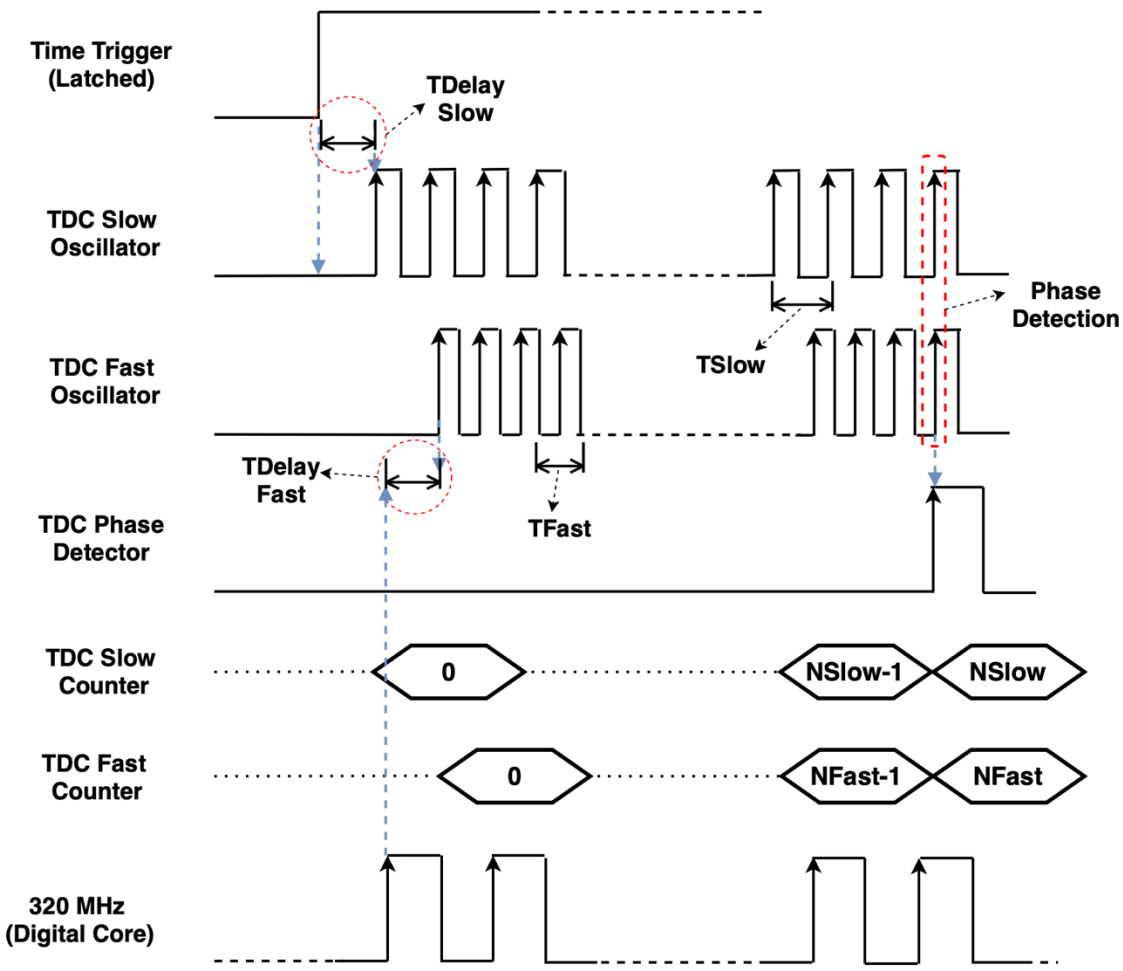


Figure 34- TDC timing diagram

This timing diagram shows the whole cycle of the TDC, starting from the arrival of Time Trigger, the start of both oscillators until the phase detection of both oscillators. The binning or LSB of this TDC is given by the difference of slow oscillator period (Tslow) and fast oscillator period (Tfast):

TDC bin = Tslow – Tfast = 42 ps (Default ASIC configuration)

Although the binning can be adjusted by modifying the oscillators frequency through Slow Control, it is not recommended as it could change drastically the performance of this TDC. Finding the Fine Time, users will have to take into account other parameters as well and use the formula given in TEMPOROC2 digital operation section:

T = (Nslow-1) * Tslow - (Nfast-1) * Tfast + TdelaySlow – TdelayFast

Each Time Trigger is equipped with a TDC, therefore there are two TDCs embedded in each analog channel of this ASIC.

TEMPOROC2 analog and triggers readout operation

For analog output (differential shaper peak detectors) and triggers (Time and Charge) readout, there is a set of registers allocated for this purpose. This register is accessible through the following interface :

- rstn_read (AC12) : Low level reset for read register, to be asserted once at the beginning at the readout
- ck_read (AC9) : Clock for read register, recommended period > 200 ns

The suggested timing diagram is illustrated in **Erreur ! Source du renvoi introuvable.**.

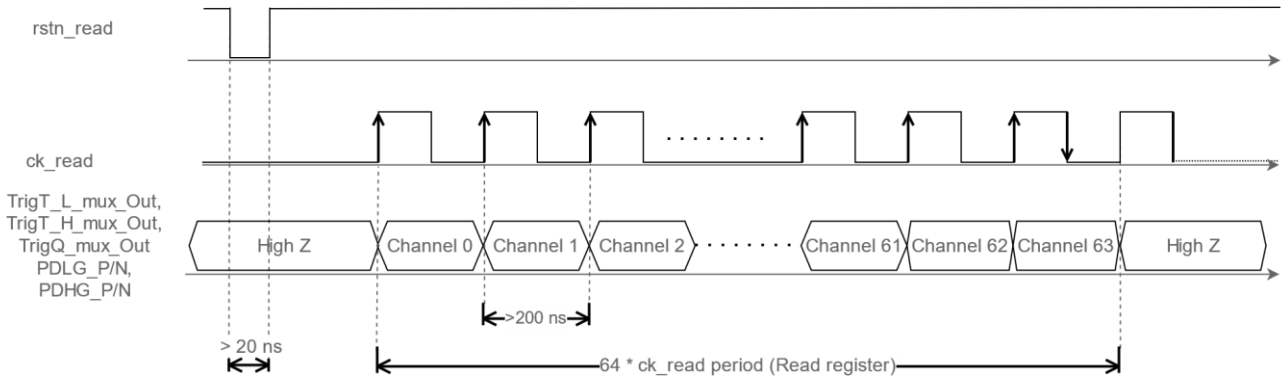


Figure 35 – TEMPOROC2 read register timing diagram

Output Name	Ball Map	Comment	Output type	Sub address
TrigT_L_mux_Out	B15	Multiplexed Time trigger output (Low threshold)	Trigger	0-63
TrigT_H_mux_Out	B16	Multiplexed Time trigger output (High threshold)	Trigger	0-63
TrigQ_mux_Out	B17	Multiplexed Charge trigger output	Trigger	0-63
PDLG_P/N	L23/24	Low Gain Shaper Peak detector output (p/n)	Analog	0-63
PDHG_P/N	P23/24	Low Gain Shaper Peak detector output (p/n)	Analog	0-63

Table 7 – TEMPOROC2 Triggers and Shaper outputs accessible from read register

Table 7 listed the available outputs accessible for the read register. The analog output can be connected to an ADC, oscilloscopes or similar devices. On the other hand, the trigger outputs can be connected for instance to a FPGA.

Datasheet version history

Version	Date	Information
1.0	26/12/2023	Initial release