Triroc is 64-channel SiPM readout chip, which is aimed for medical imaging application. The chip offers a multitude of options, thus making it suitable for other applications as well. Some of the main features are: dual polarity inputs, individual channel gain adjustment, Time Stamp and charge measurements. In order to address the need in compact high channel SiPM readout system, Triroc is designed to be operated with minimal external components.

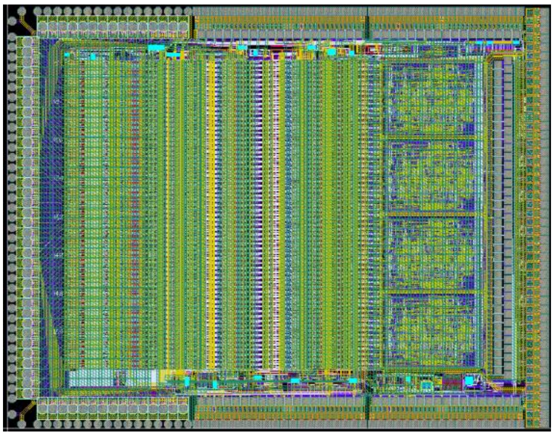

Figure 1 - ASIC layout

Parameter	Value
Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging & Dimension	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, channel by channel output enable, trigger latch, Power Pulsing

www.weeroc.com/products/triroc

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1 General description

Triroc1A is a 64-channel SiPM readout ASIC targeted for medical imaging application. In this mixed signal ASIC, the analog signal is fully digitized and the charge and timing information can be obtained directly from the digital readout.

This ASIC can be separated into 3 main sections namely: Analog, Digital and Common/Service blocks.

The Analog section is organized in to 64 channels and sensitive to negative and positive input polarity. In each channel of the Analog part, one can find an 8-bit input DAC that can be used for adjusting SiPM gain. Within the analog channel, the input signal are split into two different path: Time and Charge measurements. In Time measurement path, the input signal is fed into a pre-amplifier and a fast-trigger is generated from its output. The trigger is then sent to the Digital part for time-stamping the input signal. Additionally, the pre-amplifier output is sent to a High Gain (HG) shaper for measuring input charge lower than 100 photoelectrons (at 10^6 SiPM gain). For charge measurement section of the analog part, the input signal is sent directly to Low Gain (LG) Shaper. This shaper will allow charge measurements well over 2000 p.e. . A charge trigger is also available from this section, which is used by the digital part for validating useful and interesting events at a specified energy level.

The main purpose of the Digital part is to manage the conversion of charge and timing information from the Analog section. The converted data is then transmitted through dedicated data links.

Common/Service block regroups all the components which are used all over the ASIC such the bandgap voltage reference, 10-bit DACs for the discriminator thresholds, temperature sensor and delay cells for ADC Track/Hold.

All the enumerated ASIC pins in this document are based on BGA ball out numbering in Section 8.

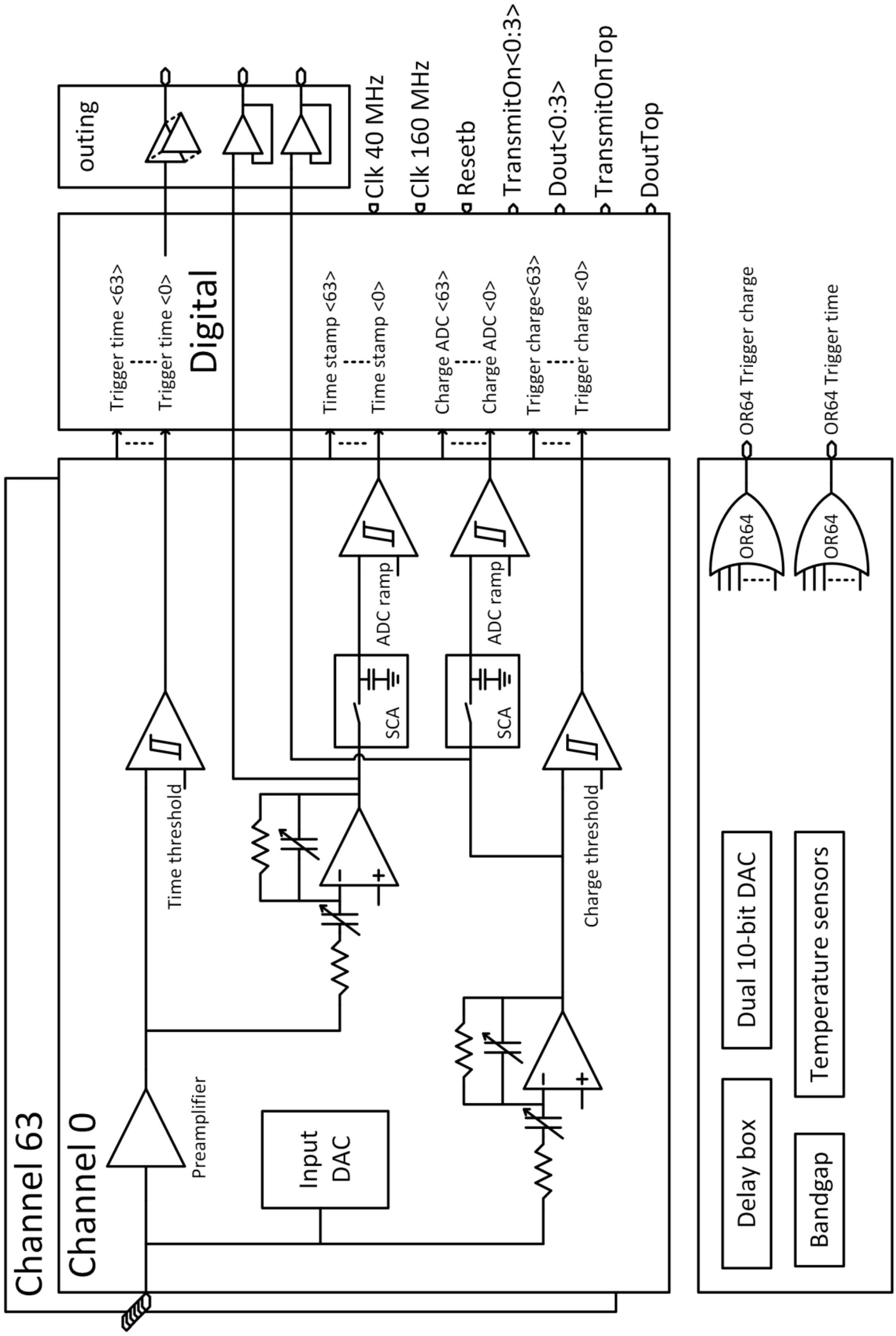


Figure 2 - General ASIC block scheme

1.1 Operation modes

1.1.1 Analog Charge measurement

Analog charge measurement is available through analog signal multiplexers. User can sequentially scan the slow shapers output for each channel. A set of internal register is available in order to shift through all the slow shaper output multiplexer. There are two signal multiplexers available in this ASIC, and each shaper (Low & High Gain shapers) are assigned its dedicated multiplexer output.

In order to use the multiplexer outputs in conjunction with an external ADC, the multiplexer outputs are required to be held for sampling: either from analog memory sampling (SCA with Track/Hold stage) or Peak Detector circuits. With analog memory sampling, users can either use internally generated Hold signal or the external Hold input of the ASIC. The internal Hold signal is generated from a delayed Time or Charge trigger. Therefore user has to set the desired delay (usually similar to shaper peaking time) prior to measuring the input charge. Otherwise, by selecting Peak Detector circuit, the peak of the shapers will be held automatically.

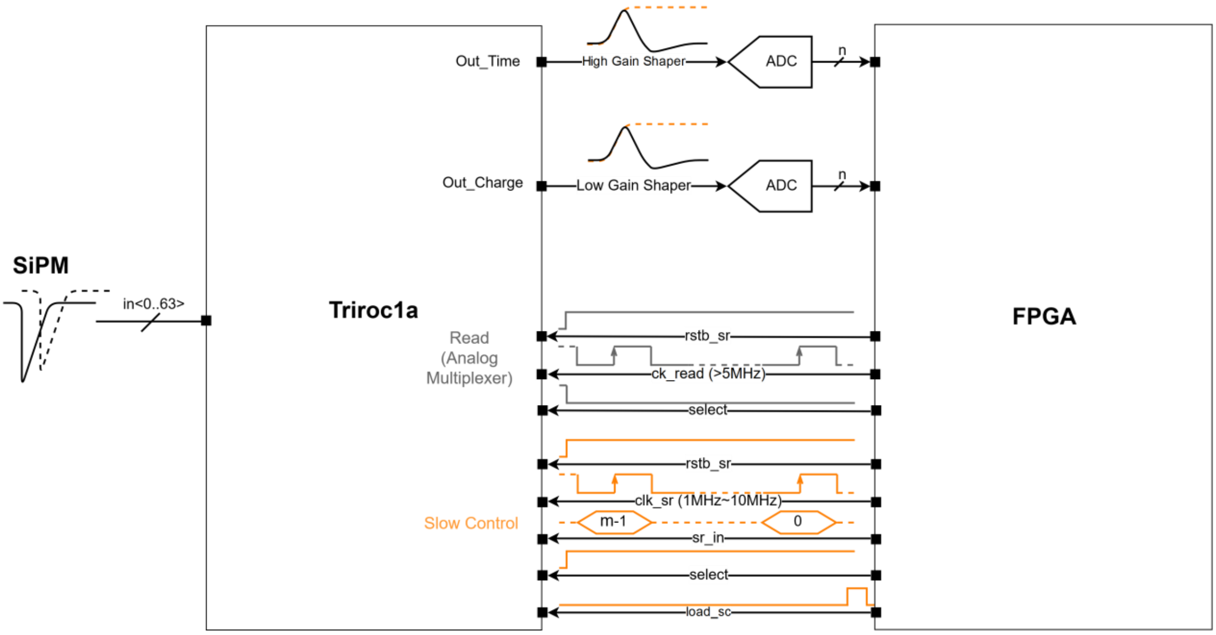


Figure 3 - Analog Charge measurement mode

1.1.2 Full digital charge measurement

In this mode, charge measurements are performed directly with the ADCs embedded in the ASIC. Even though the conversion rate is relatively modest, these ADCs still offer an excellent linearity for 10-bit data conversion. Similarly, like the charge measurement in analog mode, the Hold signal has to be provided (internally or externally), if the Peak Detector circuit is not used for sampling the slow shaper outputs. Once the slow shaper signals are held correctly, the digital conversion can be initiated automatically once the ASIC detects a trigger. Otherwise the conversion can be also initiated manually via dedicated digital core control inputs. The data will be then transferred through dedicated LVDS outputs bank. The conversion rate is in the order of 50 kEvents/s.

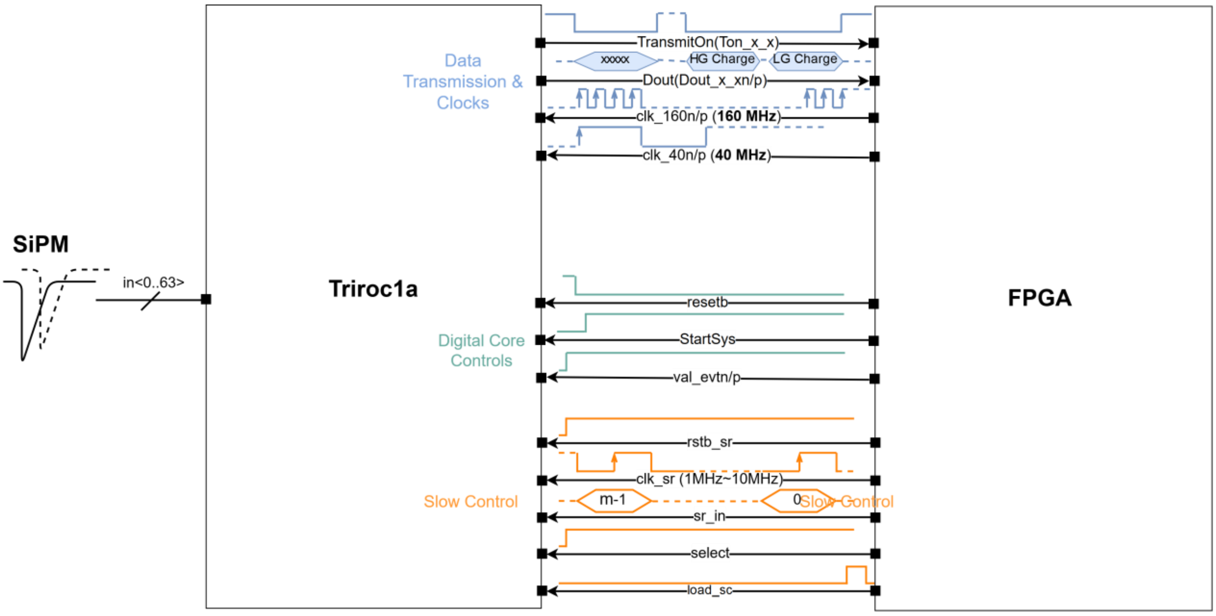


Figure 4 - Digital charge measurement mode

1.1.3 Full digital charge and time measurement

In this mode, the time and charge measurements are also performed using the ADCs embedded in the ASIC. One the ADC is assigned for converting the signal from Time-to-Amplitude converter (TAC) available in this ASIC. The other ADC has to be assigned either for Low or High Gain shapers. The digital conversion can be initiated automatically once the ASIC detects a trigger or manually via digital core control inputs. The data will be then transferred through dedicated LVDS outputs bank. Hit data, coarse and fine time and charge data are available. The conversion rate is also about 50 kEvents/s.

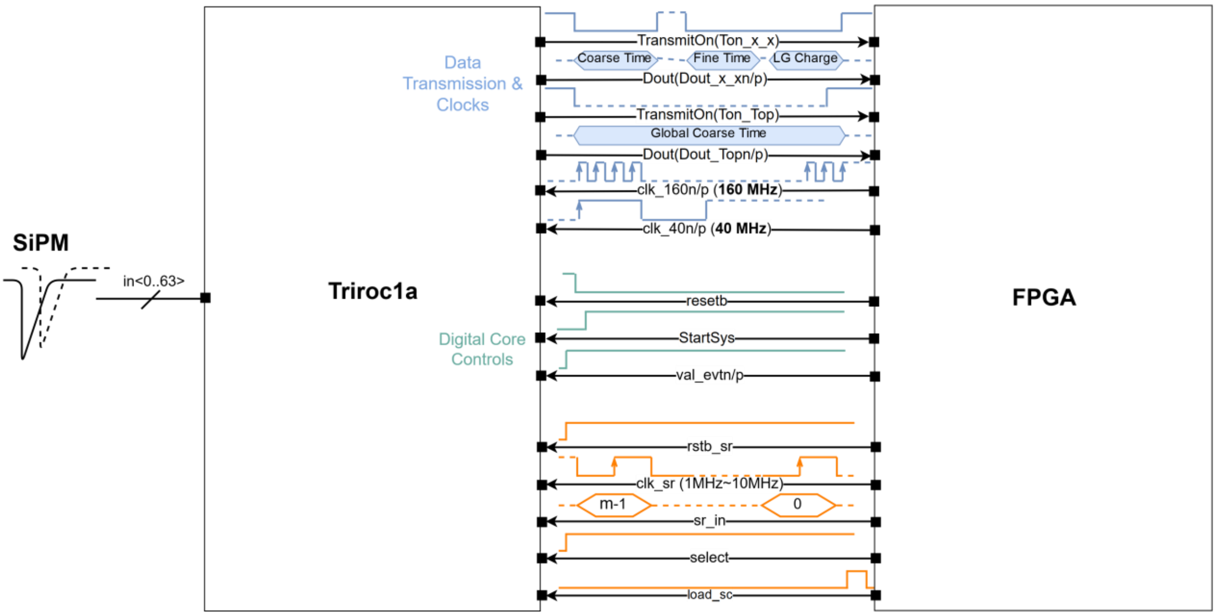


Figure 5 - Digital charge and time measurement mode

2 Maximum ratings

The operating condition of Triroc1A should not exceed the parameters listed in Table 1.

Parameter	Note	Minimum	Maximum	Unit
Storage temperature range		-40	125	°C
Operating temperature range		-20	110	°C
Power pin	All VDD power pins (3.3V – vddx)	0	3.5	V
Ground pin	All ground (gndx) pins	0	0	V
Analogue input		-0.5	VDD+0.3	V
Digital input LVCMOS		-0.5	VDD+0.3	V
Digital input LVDS		-0.5	VDD+0.3	V

Table 1 - Maximum rating operation condition

Triroc1A electrostatic discharge (ESD) protection is HBM (Human Body Model) compatible on every pin.

3 ASIC front-end

The analog front-end of this ASIC is divided into 2 sections: high bandwidth pre-amplifier for timing path and shapers (Low Gain Shaper and High Gain Shaper) for charge measurement. The block scheme of this ASIC front-end is illustrated in Figure 6.

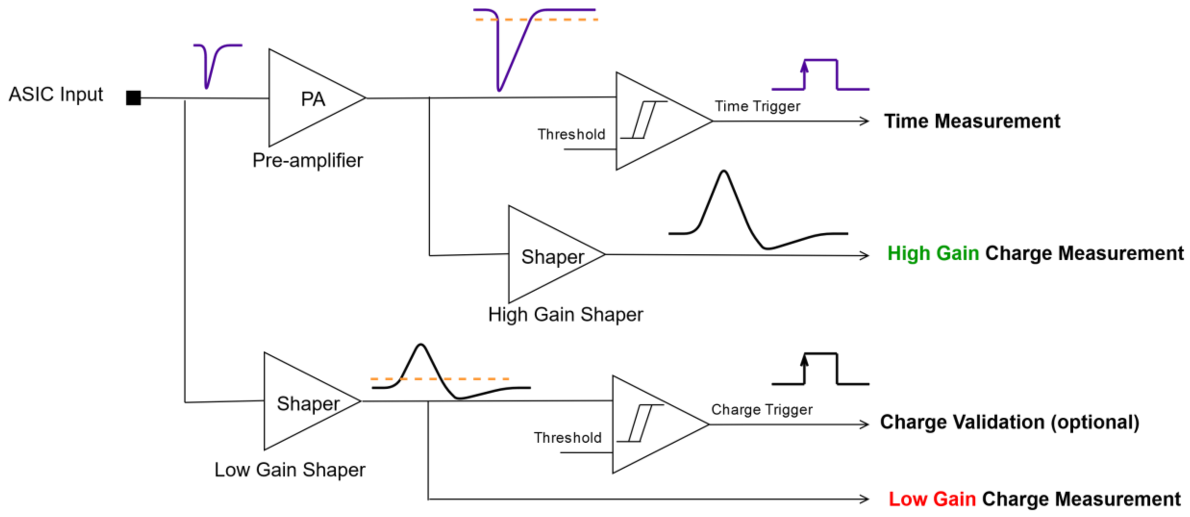


Figure 6 - Triroc front-end block diagram

3.1 Pre-amplifier

The pre-amplifier is a DC coupled common base amplifier (illustrated in Figure 11). The DC current of this pre-amplifier can be set via Slow Control parameters so that users could adjust the input impedance (50~325 Ohm) of this ASIC. The input DAC is fed through the base the pre-amplifier which allow users to tune the input voltage from 0.2 V to 2.2 V. Towards the output of the pre-amplifier, a resistor is used for current to voltage conversion. The resulting signal will be sent either to a fast discriminator for generating Time Trigger or to a High Gain shaper for secondary charge measurement.

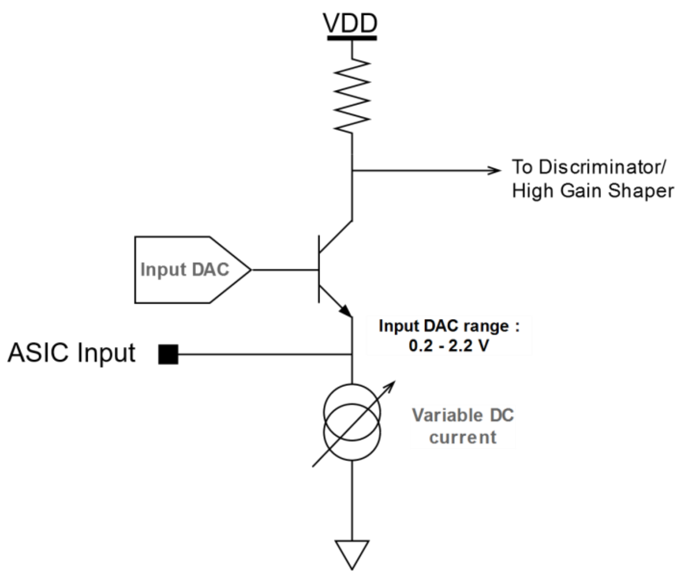


Figure 7 - Pre-amplifier structure

3.1.1 *SiPM High Voltage trimming*

At the input of the ASIC, its DC level can be adjusted by a DAC (Refer to Figure 7 – Input DAC) for each channel. This DAC can be used to trim the high voltage (HV) applied to the SiPM by either increasing (for negative HV) or decreasing (for positive HV) the effective value applied to each detector channel. This feature will allow user to adjust the detector gain non-uniformity especially when using the chip with SiPM array. The input DACs can be controlled through Slow Control registers (refer to Table 6) from bit #690 to #1255. The DAC input is binary-coded decimal on 8 bits and its electrical characteristics are the following:

- Output : 0.2-2.2 V, Range : ~2 V
- Min value (DAC code = 0) : ~0.2 V
- Max value (DAC code = 255) : ~2.2V
- LSB : ~8 mV/DAC unit

Refer to Section 6.1 for ASIC connections to detectors. <u>It is **NOT** recommend to disable the input DAC (Slow Control bits cmd/cmdb_inpdac<x> = '0') as it will clamp the pre-amp base to the ground.</u>

3.1.2 *Pre-amplifier bias and input impedance adjustment*

User can also adjust the pre-amplifier bias current (Refer to Figure 7 – Variable DC current) which will alter the ASIC input impedance as well. This bias current is controlled via Slow Control bits #87 - #90. These Slow Control bits will change the current mirror ratio which biasing the pre-amp. The effective ratio can be calculated from division of the nominal value (0.3mA*200) by the sum of activated Slow Control bits suffix. For example if Slow Control bit #87 is active (sw/swb_400 = '1'), the suffix to be used in the calculation is 400 :

Pre-amp DC current = 0.3 mA * (200/Slow Control suffix) = 0.3 mA * (200/400) = 0.15 mA

Combining all the Slow Control parameters, the current ratio will be from 0.267 to 4 which yields the DC current of the pre-amplifier from 0.08 mA to 1.2 mA. The resulting input impedance can calculated from the following equation:

Input impedance = 25 mV / Pre-amp DC current

For typical application it is recommended to set the pre-amplifier bias current to nominal value or 0.3 mA (SC bit #88 - sw/swb_200 = '1'). With the nominal bias current the input impedance is about 100 Ohm.

3.2 Shaper

In parallel to the pre-amplifier, a slow shaper, denoted as Low Gain Shaper, is used for primary charge measurement. As the input of this shaper is coming directly from the detector, the minimum signal is expected in the order of a few hundred photo electrons of charge, hence the usage of Low Gain Shaper name for identifying this component. The output of this shaper is sent to the ADC for charge measurement and also for producing Charge Trigger.

Additionally, a secondary shaper (High Gain Shaper) is also available for charge measurement. This shaper is located after the pre-amplifier stage (refer to Figure 6) in order to provide additional gain.

Both of the shapers are identical in term of design (CR-RC shaper) and Slow Control parameters. Each shaper can be configured individually. The time constant of "differentiator",t_d (R1*C1), and "integrator",t_i (R2*C2), can be set independently via the Slow Control. The bits for setting t_d and t_i of LG shaper are the following :

- t_d : sw/swb_lg_r1<2..0> (Bit SC #131-133) for R1, sw/swb_lg_c1<3..0> (Bit SC #134-137) for C1. Values: 1.25 ns - 160 ns, step : 1.25 ns.

- t_i : sw/swb_lg_r2<2..0> (Bit SC #138-140) for R2, sw/swb_lg_c2<3..0> (Bit SC #141-144) for C2. Values: 10 ns - 1.28 µs, step: 10 ns.

The bits for configuring HG shaper time constants are:

- t_d : sw/swb_hg_r1<2..0> (Bit SC #103-105) for R1, sw/swb_hg_c1<3..0> (Bit SC #106-109) for C1. Values: 1.25 ns - 160 ns, step : 1.25 ns.
- t_i : sw/swb_hg_r2<2..0> (Bit SC #110-112) for R2, sw/swb_hg_c2<3..0> (Bit SC #111-116) for C2. Values: 10 ns - 1.28 µs, step: 10 ns.

In typical usage, shaper peaking time,t_p, is equal to t_d and t_i values. Therefore t_p=t_d=t_i can be set from 10 ns – 160 ns with a step of 10 ns. By default LG and HG shapers peaking time, t_p=t_d=t_i , is set at 20 ns with a maximum gain of 10.

Parameter	C1	R1	t_d = R1*C1	C2	R2	t_i = C2*R2
Value	0.25 – 4 pF	5 - 40 kOhm	1.25 ns - 160 ns, step : 1.25 ns	0.1 – 1.6 pF	100 - 800 kOhm	10 ns - 1.28 µs, step: 10 ns

Table 2 – HG/LG shapers parameter summary.

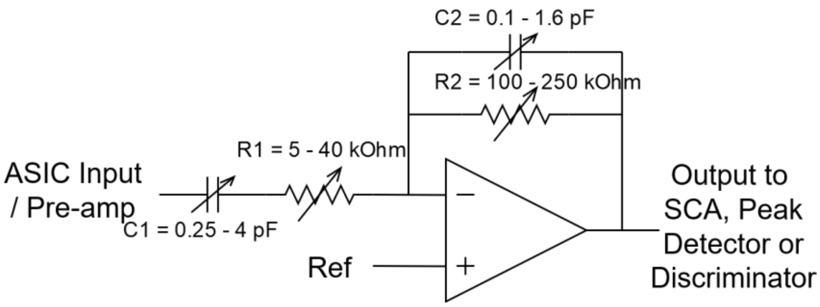


Figure 8 - Triroc shaper (High Gain & Low Gain)

3.2.1 Charge measurement

The charge measurement can be performed either using analog memories array (SCA) with Track/Hold and delay stage or directly with Peak Detector stage. The basic operations for both charge measurement system are illustrated in Figure 9 and Figure 10.

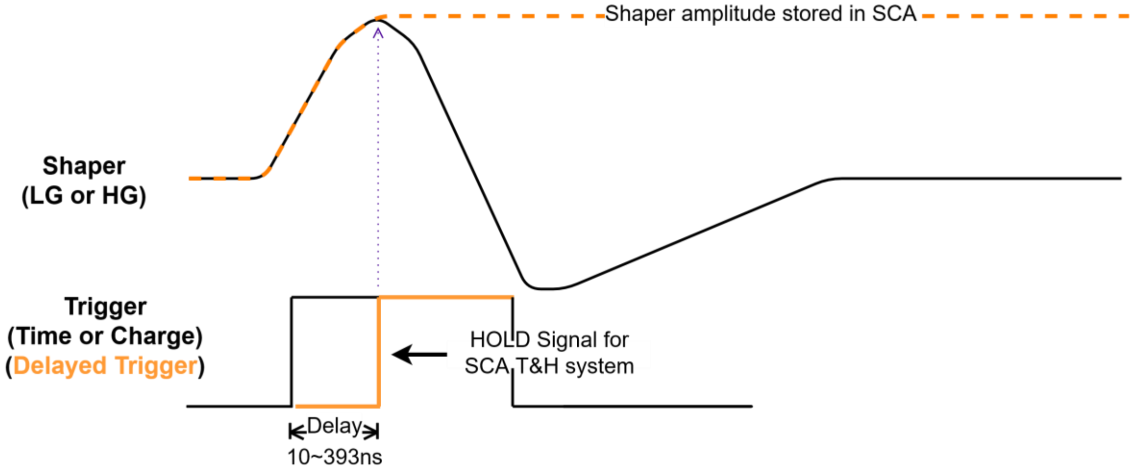


Figure 9 – SCA with Track/Hold stage operations for charge measurement

For SCA usage, a HOLD signal is required in order to store analog signal coming from the shaper. This HOLD signal can be from external source or internally generated from a trigger (Time or Charge). In the case of internally generated HOLD signal, the trigger signal is used in conjunction with a delay block. The delay can be tuned via Slow Control (bits #50 - 57), so the required signal point (e.g. shaper's peak) can be stored (or hold) into the analog memory array or SCA.

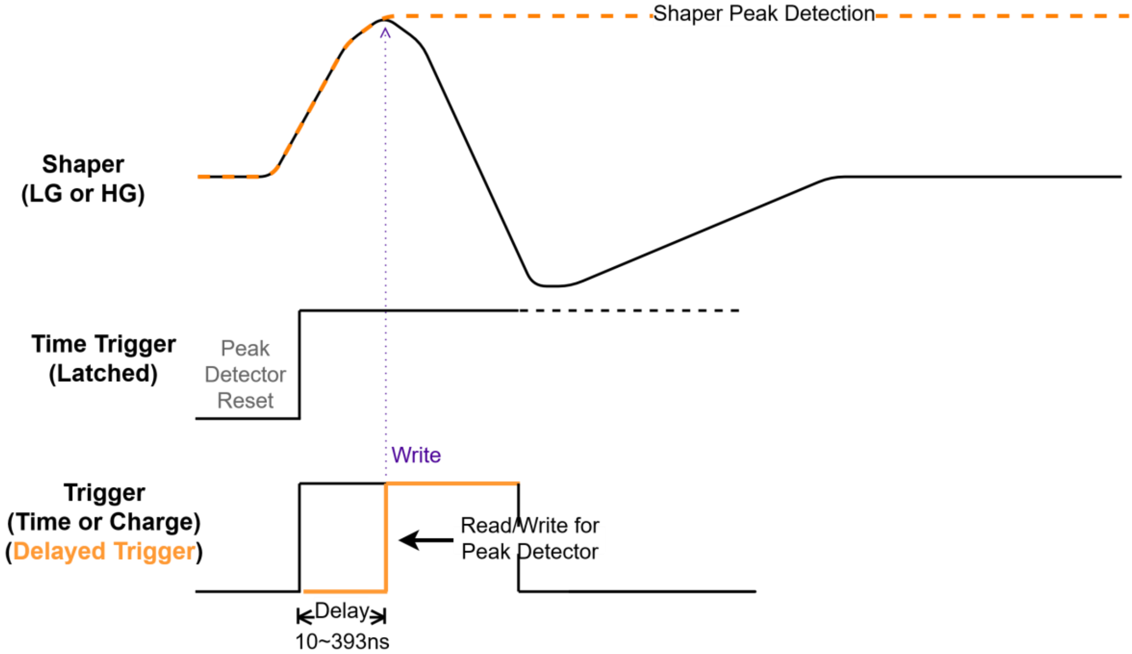


Figure 10 – Peak Detector operation

Peak Detector operations will also require internally generated delay trigger. In this case the delay has to be set long enough be longer than the peaking time of the shaper.

The internal hold generations will require latched triggers and either Time or Charge trigger can be used. The selection of the trigger is done via Slow Control bit #46 – choice_OR_delay ('1' for Charge Trigger and '0' for Time trigger). The required delay can be set through Slow Control bits #50 to #57. The characteristics of this trigger delay are the following:

- Slow Control bits : #50(MSB) - #57(LSB) – BCD coded
- Output delay : 10 – 115 ns with ~1.5ns/Delay Unit

Additionally the HOLD has to be set internally through the Slow Control bit #47 – sel_holdb ('0' for internal HOLD or '1' for external HOLD). When using external HOLD signal, the hold phase for Track/Hold stage or write phase for Peak Detector stage will be active low.

The acquired analog signal will be sent to both ADCs in this ASIC for the data conversion. Additionally, the output selection between SCA and Peak detector stage for both shapers are listed in Table 3 and Table 4. These output selections can affect the ADC input for internal data conversion (Section 4.1.1) and also Analog readout multiplexer (Section 5.4).

SC bit #124 – sel_hg<1>	SC bit #123 – sel_hg<0>	HG Shaper output
0	0	Peak Detector
0	1	SCA
1	0	Pre-amp SCA
1	1	Reserved

Table 3 – HG output selection to ADC

SC bit #153 – sel_lg	LG Shaper output
0	Peak Detector
1	SCA

Table 4 – LG output selection to ADC

3.3 Trigger scheme

This ASIC features two triggers : Time Trigger and Charge Trigger. For Time Trigger, the discriminator input is fed directly from the pre-amplifier. On the other hand, Charge Trigger is generated from LG shaper. Both trigger thresholds are set independently by 10 bits DAC. Additionally Time Trigger threshold can be trimmed further by a 6-bit DAC for each channel.

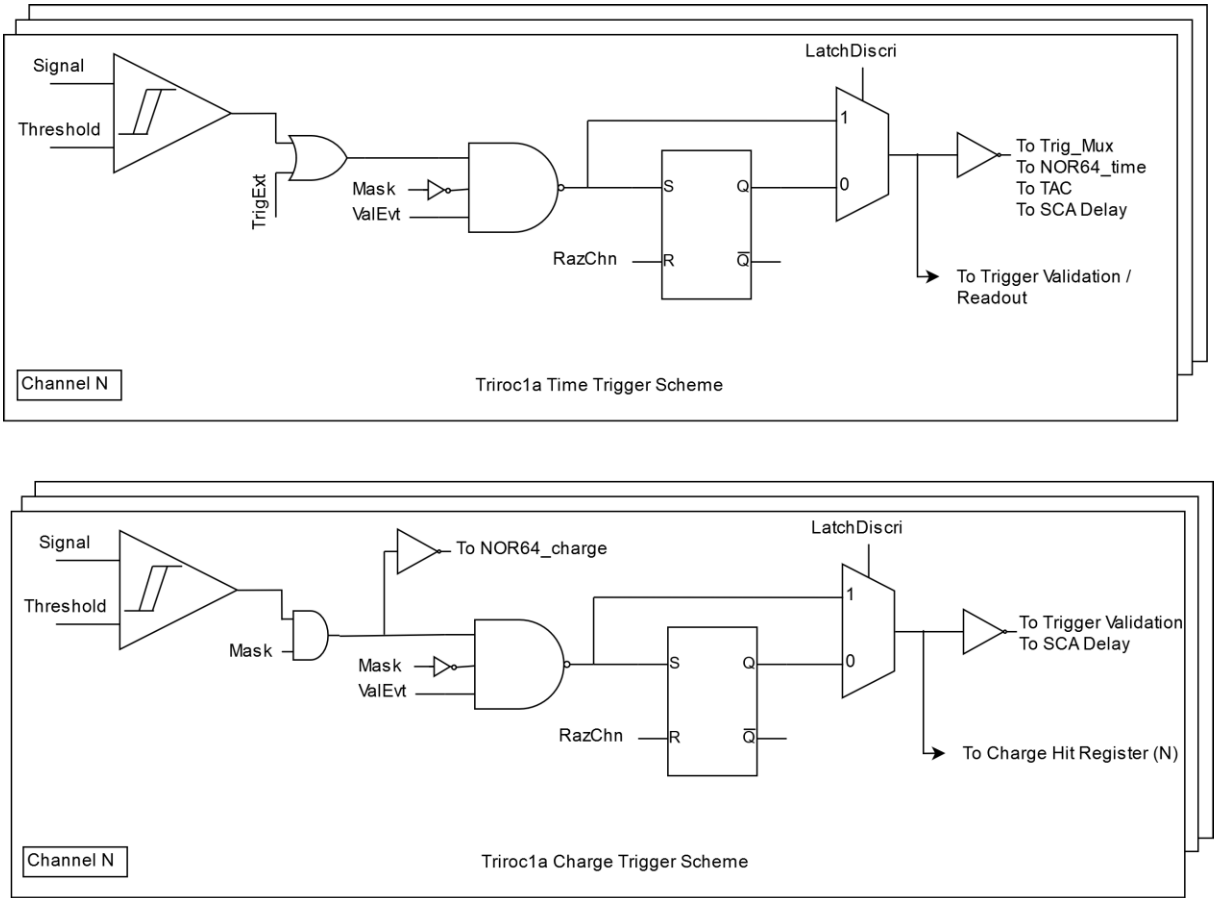


Figure 11 – Triroc triggering scheme. Top : Time Trigger scheme. Bottom : Charge Trigger scheme.

Figure 11 depicts the triggering scheme in analog channel. In each Charge and Time measurement path, a trigger can be generated for various purposes. Time Trigger, can be used at several areas. Main application of Time Trigger is to be used as Hit Channel information thus it will act as time-stamp information in the digital part. By default the Hit Channel information need to be validated by Charge Trigger, within a time frame (set around 200 ns by default). This validation can be overridden if required. Should the validation is bypassed; Hit Channel information is coming directly from Time Trigger (without Charge Trigger validation). Refer to Section 4.1.2 for readout sequences based on triggers usage.

Both Charge and Time Triggers have a secondary purpose as the driver of Track/Hold signal for internal ADCs. In default configuration, Charge Trigger will generate this Track and Hold signal (after a certain delay). Alternatively, Time Trigger can also be used to generate the Track/Hold signal. Refer to Section 3.2.1 for the usage of triggers in charge measurements.

The threshold for Time Trigger (vth_T) and Charge Trigger (vth_Q) can be set via 10-bit DACs. Additionally 6-bit trimming values of the Time Trigger threshold are available for each analog channel.

The characteristics for the Time Trigger threshold & including the trimming are the following :

- 10-bit common Time Trigger threshold :
  - Slow Control bits #70(MSB) - #79(LSB) – BCD coded
  - Output : 1.27 – 2.22 V with ~0.92mV/DAC Unit
- 6-bit channel specific Time Trigger threshold trimming :
  - Slow Control bits #297 - #681 with 6-bit per channel – BCD coded
  - Range : ~100m V with ~1.5mV/DAC Unit
- Effective Time Trigger threshold :

Time Trigger threshold = 1.27 V + ((10-bit DAC value*0.92 mV) − (6-bit DAC value * 1.5 mV))

The characteristics for the Charge Trigger threshold are the following :

- Slow Control bits #60(MSB) - #69(LSB) – BCD coded
- Output : 1.02 – 1.94 V with ~0.9mV/DAC Unit

Several inputs pins are available for controlling the triggers of this ASIC:

- ext_trig : AB21 – Input for external trigger signal for Time Trigger
- val_evt_n/p : AA23, Y23 – Event validation input. Fast masking of all 64 channels trigger outputs.

Following outputs are available for Time and Charge triggers:

- NOR64_time: F22 – 64 channels OR output of Time trigger.
- NOR64_charge: E23 – 64 channels OR output of Charge trigger.
- Trig_MUX : C23 – Time Trigger multiplexed output.
- Out <0-63>: Time Trigger output for each analog channel, not bonded in BGA version of the ASIC.

Several Slow Control parameters (Table 6) are used for controlling the trigger scheme :

- Trigger mask : Slow Control bit #169 - #232 – mask/maskb
- Internal or external "reset channel" (for latch) selection : Slow Control bit #168 – disable_RazChnInt
- Bypass internal trigger validation : Slow Control bit #167 – bypass_RazChnME
- Time & Charge trigger latch mode selection : Slow Control bit #94 – latch_discri
- Disable 64 triggers outputs buffers : Slow Control bit #13 – DIS_out_trig – This bit should be set ON/Disabled, as no wires are bonded on the die / no BGA's ball are outputting the 64 triggers.
- Enable Charge trigger OR output : Slow Control bit #12 – EN_OR64Q
- Enable Time Trigger OR output : Slow Control bit #11 – EN_OR64T
- Enable Time Trigger multiplexer output : Slow Control bit #1 – EN_TRIG_MUX

It should be noted that for Time and Charge measurement through the internal data conversion (refer Section 4), the Time and Charge trigger outputs have to be latched: Slow Control bit #94 – latch_discri = '1'. Otherwise the data conversion will not work correct even if there are data transmitted through the data out bank.

3.3.1 Trigger polarity

This ASIC is could trigger the input signal in both polarity (Figure 12 & Figure 13). However, the Slow Control bit for the input polarity and also the trigger thresholds have to be set accordingly in order to obtain the correct trigger output:

- Negative input charge:
    - Slow Control bit #93 – cmd/cmdb_polarity = '0'
    - Time Trigger threshold **<** Pre-amp baseline
    - Charge Trigger threshold **>** LG Shaper baseline

- Positive input charge:
    - Slow Control bit #93 – cmd/cmdb_polarity = '1'
    - Time Trigger threshold **>** Pre-amp baseline
    - Charge Trigger threshold **>** LG Shaper baseline

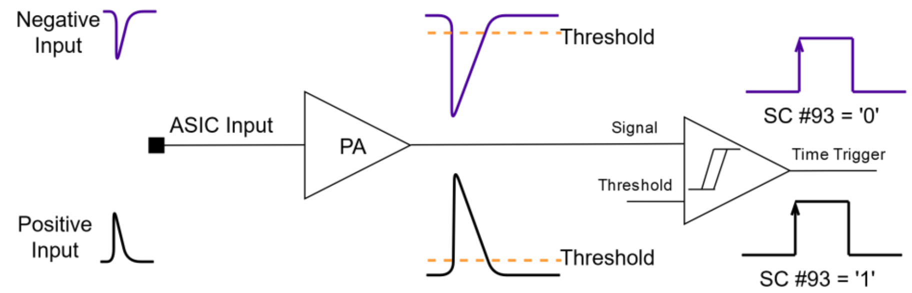


Figure 12 - Time Trigger polarity selection.

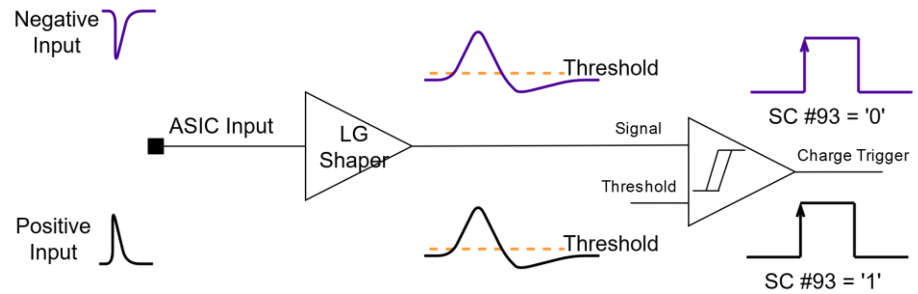


Figure 13 - Charge Trigger polarity selection.

3.3.2 Time measurement

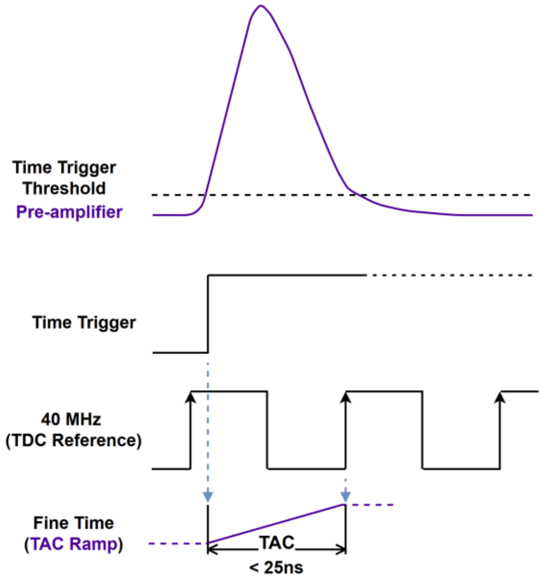


Figure 14 – Triroc fine time measurement

The fine time in this ASIC is measured from the rising edge of the Time Trigger and the next rising edge of the 40 MHz clock used as the TDC reference or time frame (Fine Time or TAC Ramp in Figure 14). The interval between these two edges is measured via a Time-to-Amplitude stage. The resulting amplitude is converted to digital data by an ADC and will indicate the interval or fine time between the arrival photon and TDC reference clock rising edge. Coupled with Coarse Time clocked by the same reference clock, user can extract the photon arrival time.

4 ASIC Back-end

4.1 Digital read-out introduction

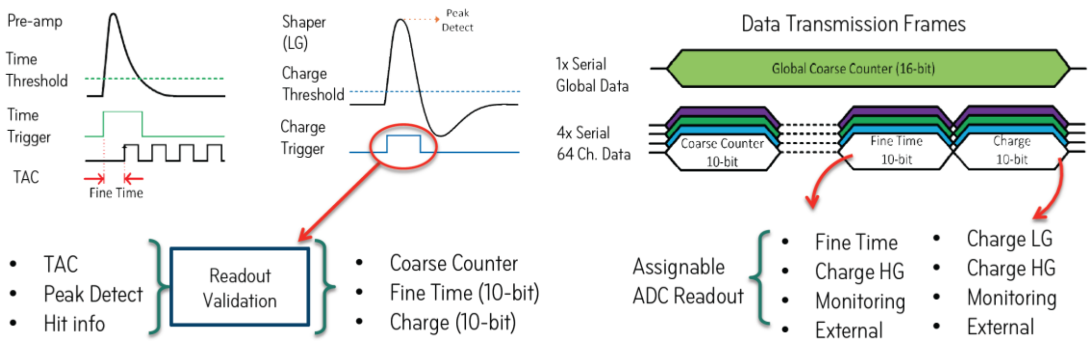


Figure 15 – TRIROC readout system

Typical readout system of TRIROC is illustrated in Figure 15. In typical usage, the Time Trigger (generated from pre-amplifier) will provide the timing information (timestamp via Time-Amplitude-Converter) which is measured between the rising edge of the 40MHz reference clock and the rising edge of Time Trigger (refer to Section 3.3.2). On the other hand, Low Gain shaper will provide charge information either through Peak Detector or Track/Hold with analog memories (SCA) circuits (refer to Section 0). All the analog time & charge information will be converted via the ADCs once the Charge Trigger (refer to Section 3.3) is acquired, which will eventually validating the readout sequence. Of course the data conversion validation, readout sequence and ADC input assignment can be overridden or changed to the user's preference.

The ADC input selection and readout sequences are discussed in Section 4.1.1 and Section 4.1.2 respectively.

4.1.1 ADC input selection

One of this ASIC features is the input selection (Table 5) of the embedded DACs is configurable for various analog block. The selection of the ADC inputs has to be configured prior to the data conversion, by setting Slow Control bits #154-155. Additionally the ADC inputs can be assigned for converting ASIC temperature and input current monitoring through sel_monitoring (E18) input.

Sel_monitoring (E8)	SC bit #155 – Sel_Data<1>	SC bit #154 – Sel_Data<0>	Time ADC Input	Charge ADC Input
0	0	0	TAC	LG Shaper*
	0	1	TAC	HG Shaper*
	1	0	HG Shaper*	LG Shaper*
	1	1	External input	External input
1	x	x	Input current	Temperature

*Refer to Table 3 and Table 4 for LG & HG shaper output

Table 5 - ADC input selection

4.1.2 Readout sequences and data conversion

In typical readout and data conversion configuration, the digital side requires the following inputs to be set correctly:

- 160 MHz clock (LVDS input at pin W23 & V23 - ck_160n/p)
- 40 MHz clock (LVDS input at pin U23 & T23 - ck_40n/p) – Same phase and synchronized to 160 MHz
- Reset input at high level (LVCMOS input at pin T22 - resetb)
- Start conversion flag at high level (LVCMOS input at pin H22 - StartSyst)

In most application, the ASIC will operate in auto-triggering mode which basically means the data conversion and readout will be initiated once a trigger is detected. There are 2 levels of operations in this mode due to the availability of two level triggering (Time and Charge triggers).

The first readout sequences (Figure 16) will require both Time and Charge triggers to be fired before the readout and data conversion is initiated. In the case of Time Trigger already fired but Charge Trigger not yet fired, a timeout can be set in order to wait for any eventual delayed Charge Trigger before the whole system is reset back to its initial condition. It should be noted that the Time Trigger verification is done individually for each channel however the Charge Trigger validation is global for whole ASIC. In order to use this functionality, several Slow Control bits are needed to be configured:

- Slow Control bit #167 - bypass_RazChnME = '0'
- Slow Control bit #168 - disable_RazChnInt = '0'
- Slow Control bit #165-166 - TimeOutSet<0..1> according to the values in Table 6

The timing diagram of the readout sequences with Charge Trigger validation is illustrated in Figure 24.

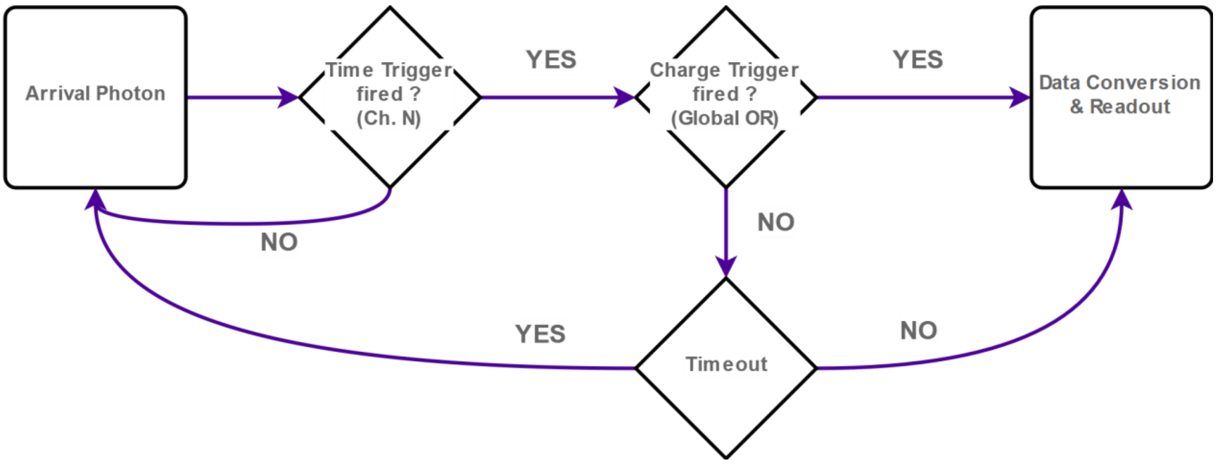


Figure 16 - Readout sequences with Charge Trigger validation

The second auto-triggering mode is based solely on Time Trigger (Figure 17). This basically means that any fired Time Trigger will initiate the readout of the 64-channel data. The following Slow Control bits are required for this Time Trigger driven readout:

- Slow Control bit #167 - bypass_RazChnME = '1'
- Slow Control bit #168 - disable_RazChnInt = '0'

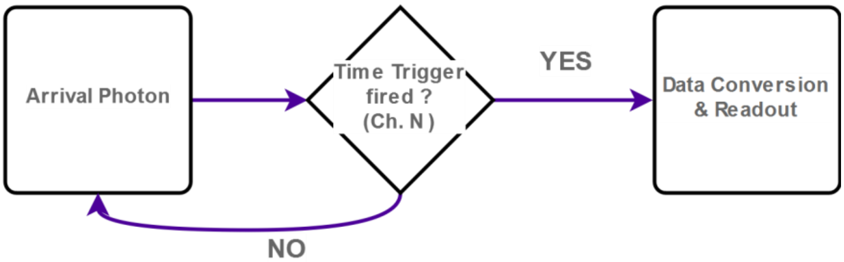


Figure 17 - Readout sequences with Time Trigger validation

The last readout mode is done manually (Force conversion) in order to initiate the readout and data conversion. This type of readout is driven by a FPGA by asserting a low level pulse (>100 ns) to ForceConvb (P22) input. The readout sequences are shown in Figure 18. This mode will bypass the readout mode illustrated in Figure 16 and Figure 17.

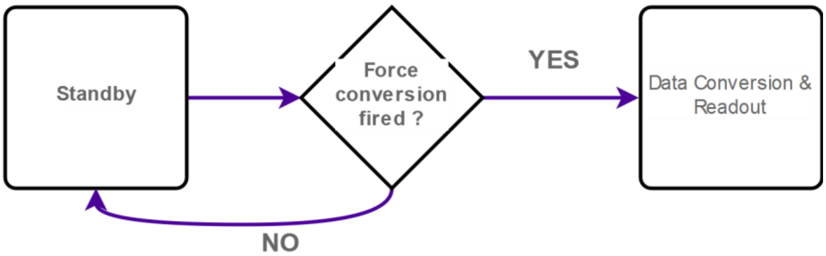


Figure 18 - Readout sequences with Force conversion command

All the readout sequences illustrated in this section will go back to initial state once the readout is done by an internal reset. However this reset can also be driven externally through RazChn (M22) input. This input is effective only when Slow Control bit #168 – disable_RazChnInt is set to '1' which means that the internal reset is disabled and the external input will take over the reset phase.

4.2 Data transmission

The data transmission from the ASIC is synchronized with the system clock running at 80 MHz (generated from 160 MHz sent to the ASIC) and each data transmission frame is associated with data transmission flag (available on TransmitOn pins). In total, there are 5 LVDS data output lanes: 4 outputs for transmitting channels data and 1 output dedicated for global coarse counter. The timing diagram channels data and global coarse counter are shown in Figure 19 and Figure 20 respectively.

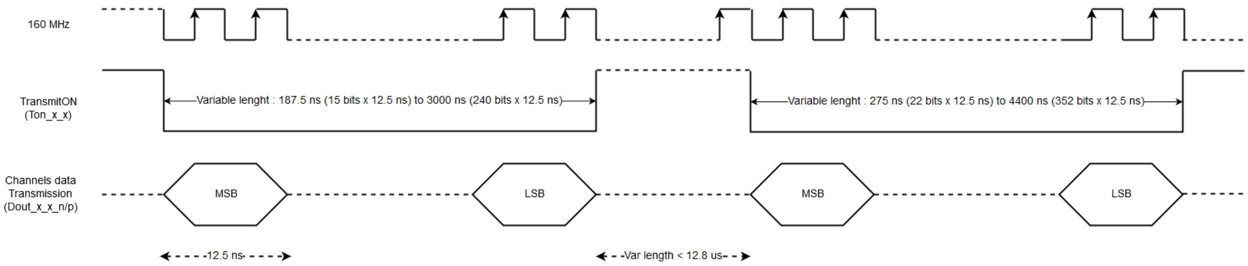


Figure 19 – Channels data transmission timing diagram

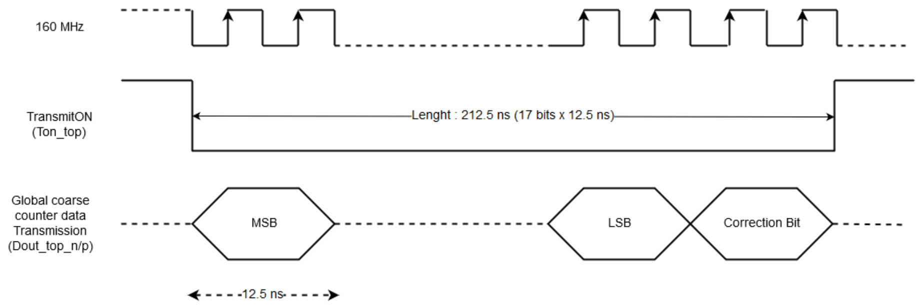


Figure 20 – Global coarse counter data transmission timing diagram

It should be noted that data transmission on several data output lanes will start simultaneously. However the length of the data frames (limited by the TransmitON signal length) could differ between the transmitting output lanes.

4.3 ReadOut Clock

The phase of the Internal ReadOut clock running at 80 MHz can be found by stopping the 160MHz while loading the slow control, as this operation will set the ReadOut Clock to low level.

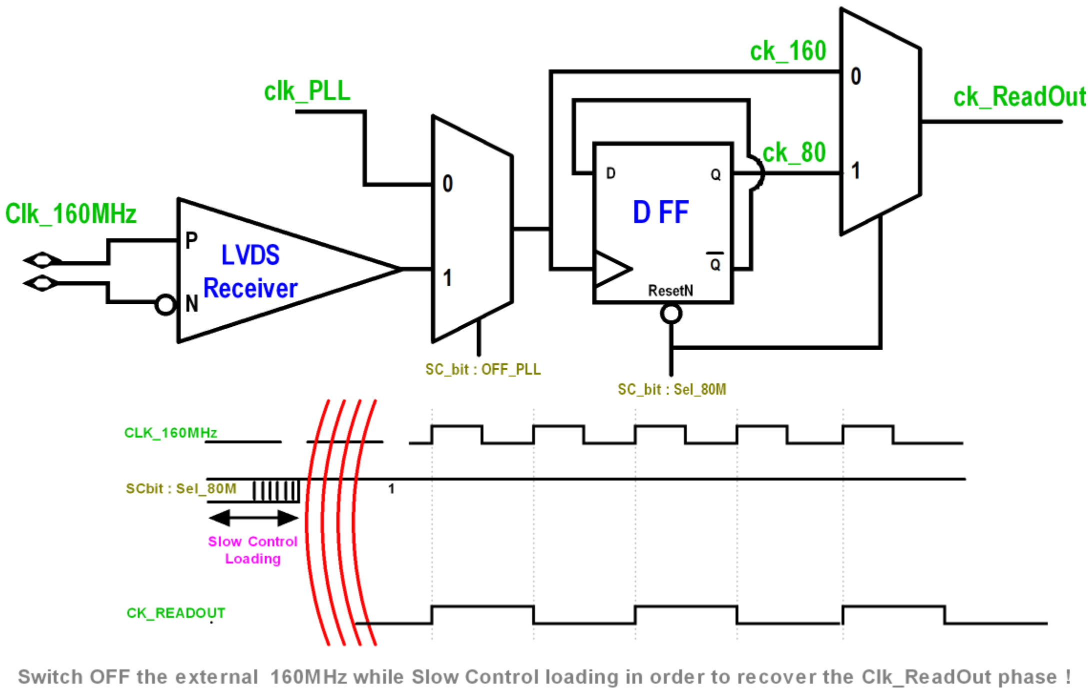


Figure 21 – ReadOut clock internal generation

4.4 Data frame and decoding for channel data

The data frame can be divided into 2 sections: channels data and global coarse time counter.

The mapping of channels data is divided further into 4 blocks: 1 block for 16 channels. For each block, we have one serial link to readout the internal memories. The readout is composed of 2 frames.

The memory mapping of the first frame is given below:

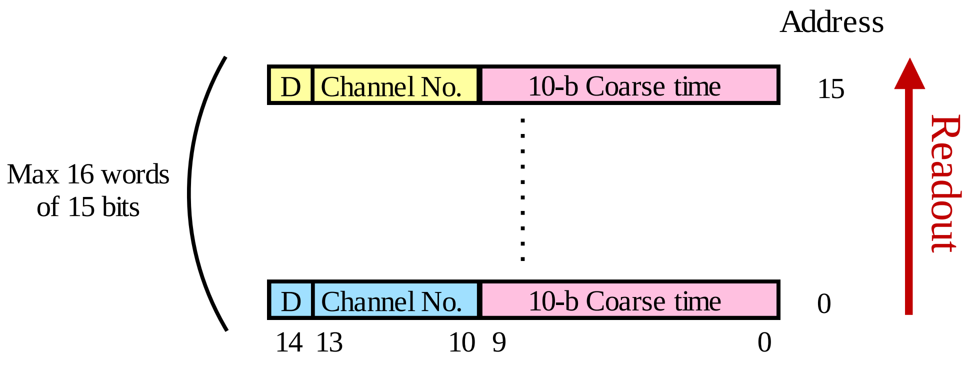


Figure 22 – TDC coarse time memory mapping (First Frame).

It is composed of maximum 16 words of 5 or 15 bits populated with:

- 1 bit for D information: word length (5 or 15 bits)
- 4 bits for channel number
- 10 bits for Coarse time counter

As the digital block integrates the zero suppress, only hit channels are readout. So, we have as many words as hit channels. The word length is given by the D information: if '0' only the 5 MSB of the word (D & Channel No.) are readout else the full word is readout. The coarse time data of a channel with the D information at '0' is the same that the last channel with the 'D' bit at '1'.

Then, the maximum readout frame is composed of 240 bits (minimum is 15 bits).

The memory mapping of the second frame is given hereafter:

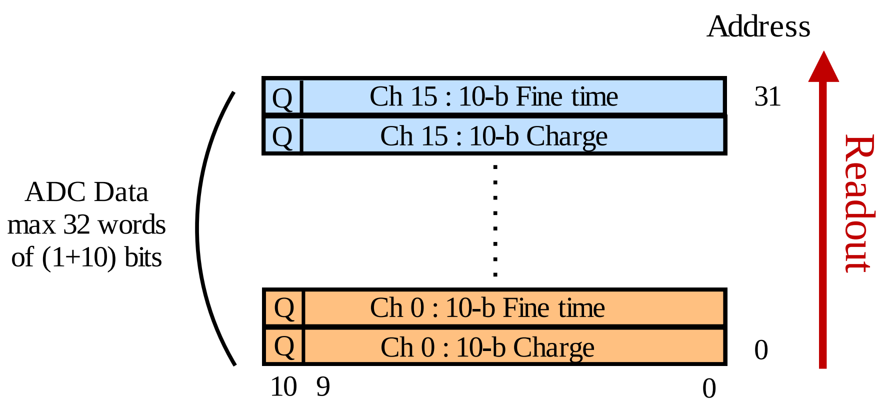


Figure 23 – Charge ADC and TDC fine time memory mapping (Second Frame).

It is composed of maximum 32 words of 11 bits feed by:

- 1 bit for Q information if the Charge Trigger has fired for this channel
- 10 bits for the ADC result (charge or fine time)

Only channels readout in the first frame will be readout during the second frame. The ADC result for one channel is composed by 2 words: 1 for the charge and 1 for fine time.

Then, the maximum readout frame is composed of 352 bits (minimum is 22 bits).

All the data are encoded in Gray format.

The readout process is done address 0 first and MSB first. The data are sent over the "data out" pins in differential output:

- Dout_48_63n/p : R23, P23
- Dout_32_47n/p : N23, M23
- Dout_16_31n/p : L23, K23
- Dout_0_15n/p : J23, H23

The data are valid when the "Transmission ON" signal is at '0' logic level. "Transmission ON" pins are:

- Ton_48_63 : R22
- Ton_32_47 : N22
- Ton_16_31 : L22
- Ton_0_15: J22

The readout is made at 80 MHz (160 MHz clock provided at ck_160_n/p inputs divided by 2 internally).

The 40 MHZ (ck_40n/p inputs) is only used for the coarse time tagging (25 ns step). The coarse time counter starts just after the release of the reset. The fine time and the coarse time information are needed to recover the real time of a hit channel: the real time is given by the next formula:

(Coarse time + 1) x (ck_40 period) – (Fine time)

With ck_40 is the TDC reference clock running at 40 MHz and Fine time is about 32 ps/ADC Unit.

An extra serial link is provided to readout a global 16+1 bit coarse time counter clocked with the overflow of the channel coarse time counter. The data is available at differential pins when the "Transmission ON" of this counter is at '0' logic level. Pins for coarse counter time counter data transmission are:

- Dout_Topn/p : G23, F23
- Ton_Top : G22

For further description of the ASIC I/O pins used in data readout, please refer to Section 6.2.3.

The global timing diagram of the data conversion and readout using auto-triggering mode with Charge Trigger validation is shown in Figure 24.

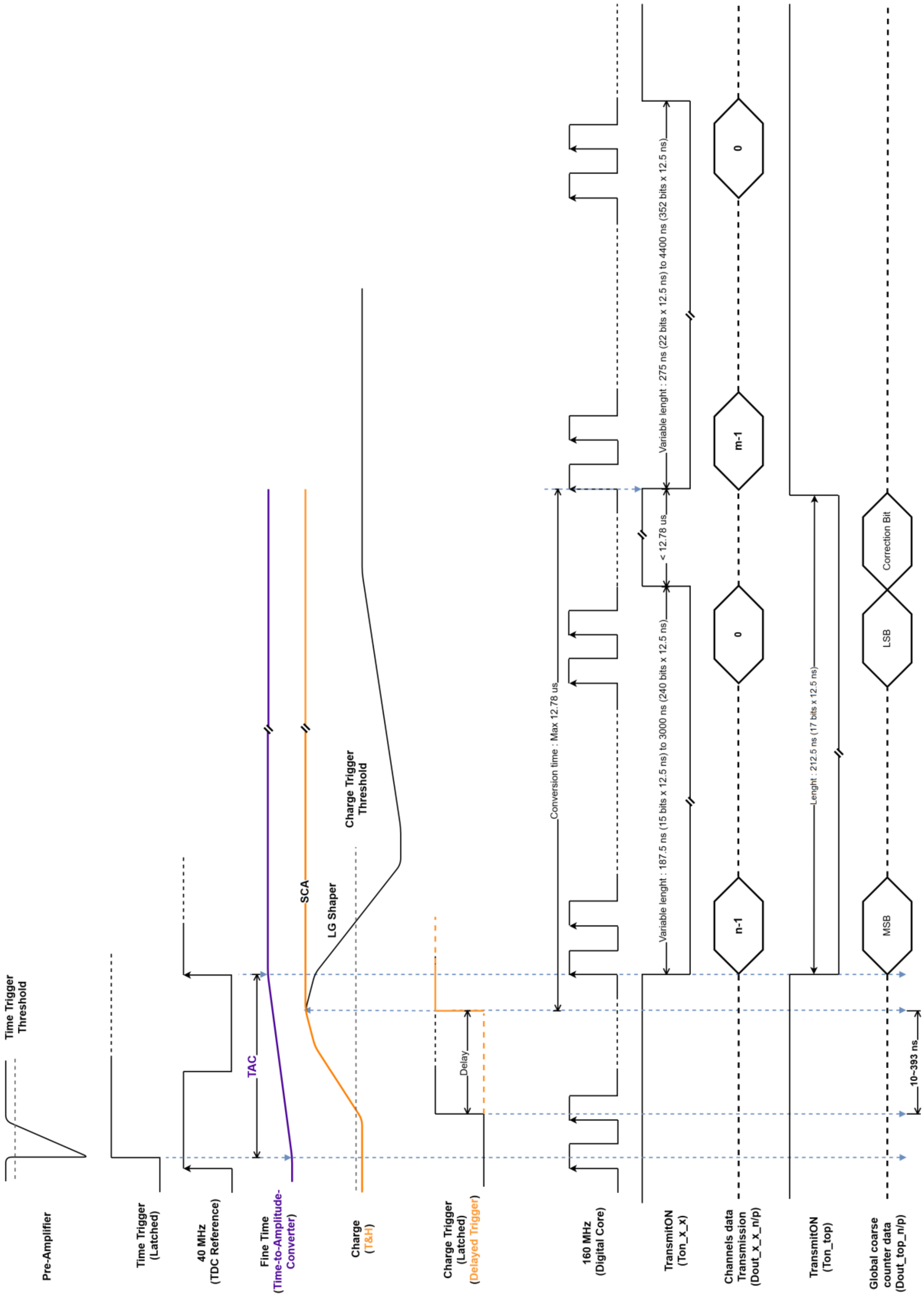


Figure 24 - Triroc Readout timing diagram

5 ASIC programmable parameters

This ASIC features several programmable registers in order to configure and monitor the output signals. The most important registers are Slow Control (SC) and Probe. Slow Control register are used for configuring the Analog section of this ASIC. On the other hand, Probe registers are used for monitoring analog or digital type signal. Both registers are accessible through a shared interface (Section 5.1).

Third set of registers, Read register, is available for monitoring shaper outputs (HG and LG) and also Time Trigger through multiplexed outputs. The fourth register, Bias register, is for selecting internal biasing points which can be used for monitoring or adjusting the value. However only one biasing point can be selected for a given time due to the multiplexed output. Both of Read and Bias registers are accessible through similar interface (Section 5.4).

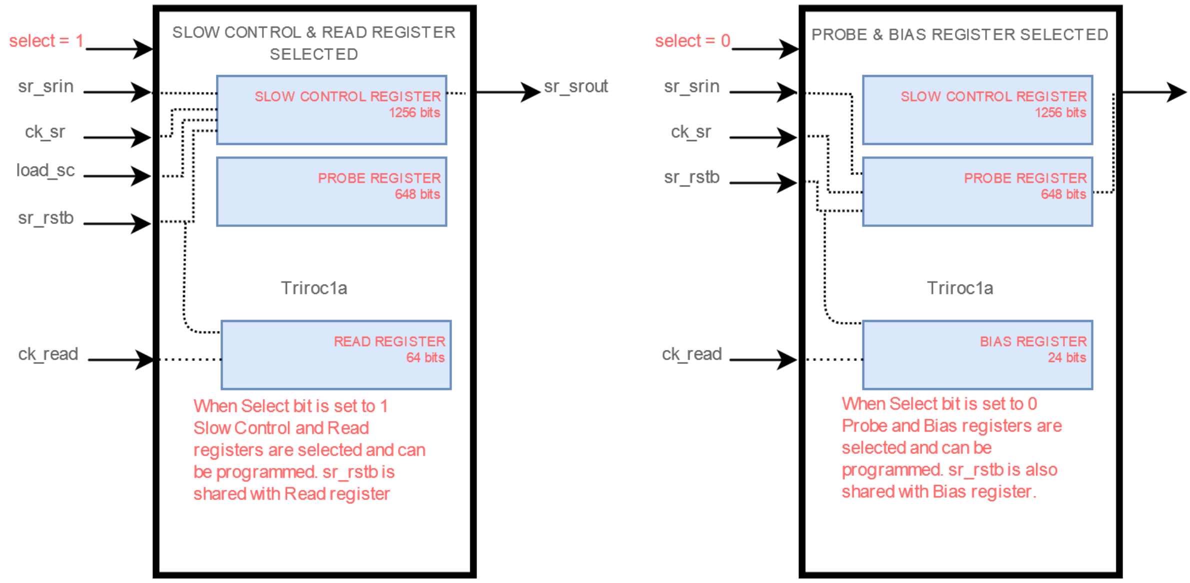


Figure 25 - Triroc 1A Slow Control, Probe, Read and Bias registers interface

5.1 Slow Control and Probe general descriptions

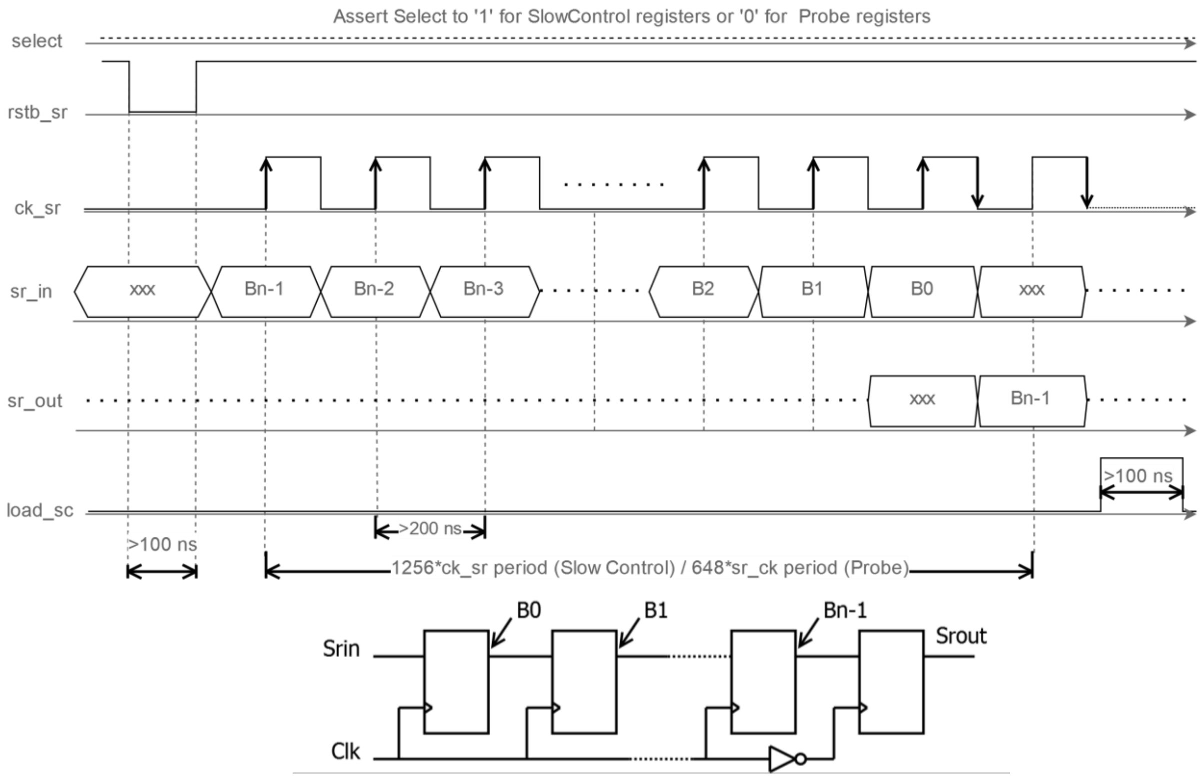


Figure 26 - Slow Control and Probe timing diagram and explanation.

The Slow Control is a shift register composed of *n* flip flops (*n* = 1256 flip flops in Triroc, first bit is B_0 = EN_TRIG_MUX and last is B_{1255} = cmd/cmdb_inpdac<63>). Data are stored in flip flops on leading edge of the clock. The data are shifted at each clock cycle as seen on Figure 26. Between sr_out and the output of the last Slow Control register's flip flop, there is another flip flop clocked on clk_sr falling edge so an additional falling edge is needed to send the data out on sr_out pin. Although most of the parameters are effective once the correct bits are shifted in, some parameters require external signal for loading the new parameters. The pin is known as load_sc in Triroc.

Just as the Slow Control, Probe is also a set of shift register. Probe and Slow Control registers are set by using the same I/O pins. A select pin is available in order to write into either Probe or Slow Control registers. The pins (BGA ball out) for configuring Probe/Slow Control registers are:

- sr_out : B23 → shift register output, on falling ck_sr falling edge (Srout in Figure 26).
- sr_in : A23 → shift register input (Srin in Figure 26).
- load_sc : B22 → Only required for loading values to input DACs. Load at low level '0'.
- rstb_sr : A22 → shift register reset('0') -> The reset, default values are loaded into the ASIC, rendering the ASIC operable. (Rstb in Figure 26).
- ck_sr : B22 →shift register clock (<10MHz). (Clk in Figure 26).
- select : A21 →select value either for Slow Control ('1') or Probe ('0') registers.

More information concerning the Probe and Slow Control pins are available in Section 6.2.

5.2 Slow Control registers

Bit	ASIC Subsection	Slow Control Name	Default value	Description
1	srin_sc, digital_triroc	EN_TRIG_MUX	1	Enable output on Trig_Mux pad. Recommended value '1' for Enable
2		SEL_80MHz	1	Enable internal clock divider for Readout. Recommended value '1' for Enable (80MHz readout)
3		DIS_Transmit	1	Disable Transmit ON signals for all I/O banks. Recommended value '0' for Enable.
4		testb_ota	1	Enable OTAs for signal monitoring in « Test Mode ». Recommended Value '1' for Enable
5		EN_ota_time	1	Enable 'Time Channels' OTA monitoring. Recommended Value '1'
6		PP_ota_time	0	Power ON/OFF 'Time Channels' OTA monitoring. Recommended Value '0' for ON
7		EN_OTA_charge	1	Enable 'Charge Channels' OTA monitoring. Recommended Value '1'
8		PP_ota_charge	0	Power ON/OFF 'Charge Channels' OTA monitoring. Recommended Value '0' for ON
9		EN_ota_probe	1	Enable 'analog signal' OTA monitoring. Recommended Value '0' for ON
10		PP_ota_probe	0	Power ON/OFF 'analog signal' OTA monitoring. Recommended Value '0' for ON
11		EN_OR64T	1	Enable output on NOR64_Time pad. Recommended value '1' for Enable
12		EN_OR64Q	1	Enable output on NOR64_Charge pad. Recommended value '1' for Enable
13		DIS_out_trig	1	Disable 64 channels trigger outputs. Recommended Value '1' for disable outputs.
14		sel_pwron_d	1	Power on Tx selection. Recommended Value '1' for Power on digital and transmissions
15		nc		NC
16		nc		
17		nc		
18		nc		
19		nc		
20		nc		
21		nc		
22		EN_transmitter	1	Enable LVDS Transmitter. Recommended Value '1'
23		PP_bias_transmitter	0	Power ON/OFF LVDS Transmitter. Recommended Value '0' for ON
24		ON/OFF 1mA	1	LVDS Transmitter current level. Recommended Value '11' for 4mA.
25		ON/OFF 2mA	1	
26		EN_receiver	1	Enable LVDS Receiver. Recommended Value '1'

27		PP_bias_receiver	0	Power ON/OFF LVDS Receiver. Recommended Value '0' for ON
28		ON/OFF 40M	1	ON/OFF 40MHz clock. Recommended value '1' for ON
29		ON/OFF 160M	1	ON/OFF 160MHz clock. Recommended value '1' for ON
30	PLL	EN_PLL	1	Enable PLL. Recommended Value '0'
31		PP_PLL	0	Power ON/OFF PLL. Recommended Value '1' for OFF
32		Ext_Vctl/Vctlb	1	No particular recommendation since PLL is OFF. Stay to default value
33		DividerN<4>	0	No particular recommendation since PLL is OFF. Stay to default value
34		DividerN<3>	0	No particular recommendation since PLL is OFF. Stay to default value
35		DividerN<2>	0	No particular recommendation since PLL is OFF. Stay to default value
36		DividerN<1>	0	No particular recommendation since PLL is OFF. Stay to default value
37		DividerN<0>	1	No particular recommendation since PLL is OFF. Stay to default value
38	ADC_ramp_Q	EN_adc_ramp_Q	1	Enable ADC Ramp – Charge Channels. Recommended Value '1'
39		PP_adc_ramp_Q	0	Power ON/OFF ADC Ramp – Charge Channels. Recommended Value '0' for ON
40		nc		NC – Spare bit
41		use/useb_compensation_Q	0	
42	Ramp_adc_T	EN_adc_ramp_T	1	Enable ADC Ramp – Time Channels. Recommended Value '1'
43		PP_adc_ramp_T	0	Power ON/OFF ADC Ramp – Time Channels. Recommended Value '0' for ON
44		nc		NC – Spare bit
45		use/useb_compensation_T	0	
46	Delay_box_triroc	choice_OR_delay	1	Select either Charge or Time trigger for internal Track/Hold generation. Recommended value '1' for Charge Trigger
47		sel_holdb	0	Select either internal Track/Hold signal or external source from Holdb pad. Recommended value '0' for internal Track/Hold signal
48		EN_delay	1	Enable Delay generation for Charge or Time Trigger. Recommended Value '1'
49		PP_delay	0	Power Delay generation for Charge or Time Trigger. Recommended Value '0' for ON
50		delay/delayb<7>	0	Delay for internal Track/Hold generation. Delay value ~ 19 ns + (BCD(delay<7:0>) * 0.8(ns)) . Recommended value will be defined later
51		delay/delayb<6>	0	
52		delay/delayb<5>	0	
53		delay/delayb<4>	1	

54		delay/delayb<3>	0	with selected value of shaper feedback. Refer Section 3.2.1.
55		delay/delayb<2>	0	
56		delay/delayb<1>	1	
57		delay/delayb<0>	0	
58	dual 10bit-DAC	EN_10bdac	1	Enable Dual 10- bit DAC. Recommended Value '1'
59		PP_10bdac	0	Power ON/OFF Dual 10- bit DAC. Recommended Value '0' for ON
60		b<9>_Q	0	DAC for setting Charge Trigger threshold: "0000000000" : 1.015V → "1111111111" : 1.943V Recommended value : Based on tests & calibration. Refer Section 3.3.
61		b<8>_Q	1	
62		b<7>_Q	0	
63		b<6>_Q	0	
64		b<5>_Q	0	
65		b<4>_Q	0	
66		b<3>_Q	0	
67		b<2>_Q	0	
68		b<1>_Q	0	
69		b<0>_Q	0	
70		b<9>_T	0	DAC for setting TimeTrigger threshold: "0000000000" : 1.274V → "1111111111" : 2.215V Recommended value : Based on tests & calibration. Refer Section 3.3.
71		b<8>_T	1	
72		b<7>_T	0	
73		b<6>_T	0	
74		b<5>_T	0	
75		b<4>_T	0	
76		b<3>_T	0	
77		b<2>_T	0	
78		b<1>_T	0	
79		b<0>_T	0	
80	bias_channel	ON/OFF_inpdac	1	Power ON/OFF Input DAC. Recommended Value '1' for ON. Value will be change only when load_sc (B22) pin = '1'.
81	*bias_regul*	EN_regul	1	Enable Internal Regulator. Recommended Value '1'
82		PP_regul	0	Power ON/OFF Internal Regulator. Recommended Value '0' for ON
83	*bias_pa*	EN_pa	1	Enable Pre-Amp. Recommended Value '1'
84		PP_pa	0	Power ON/OFF Pre-Amp. Recommended Value '0' for ON
85		OFF/ON_leak	1	Pre-amp setting in normal or calibration mode. Recommended Value '1' for Normal mode
86		ON/OFF_multivbe	0	Pre-amp input signal limiter for positive input. Recommended value ''1' for Positive input
87		sw/swb_400	0	Pre-amp DC current setting (thus ASIC input

88		sw/swb_200	1	impedance). Basic calcutions Idc = 0.3mA *200/(Sw_X). Input impedance = 25mV/Idc. Default setting : Idc = 0.3 mA*200/200 = 0.3mA. Default input impedance ~35/0.3 = 85 Ohm. Recommendation = Default value. Refer Section 3.1.2.	
89		sw/swb_100	0		
90		sw/swb_50	0		
91	*bias_discri*	EN_discri	1	Enable Discriminators. Recommended Value '1'	
92		PP_discri	0	Power ON/OFF Discriminators. Recommended Value '0' for ON	
93		cmd/cmdb_polarity	1	Set discriminator outputs according to input polarity. Recommended value '1' for positive input. Refer Section 3.3.1.	
94		latch_discri	1	Pre-amplifier and LG shaper discriminators latched output. Recommended value '1' for latch mode. Non-latch outputs are usually used for debug only. Refer Section 3.3.	
95	*bias_6bdac*	EN_6bit_dac	1	Enable 6-bit DACs for pre-amp discriminator. Recommended Value '1'	
96		PP_6bit_dac	0	Power ON/OFF 6-bit DACs for pre-amp discriminator. Recommended Value '0' for ON	
97	*bias_tdc*	EN_tdc	1	Enable TDC. Recommended Value '1'	
98		OFF_tdc	0	Power ON/OFF TDC. Recommended Value '0' for ON	
99	*bias_TWC*	EN_TWC	1	Enable Analog memory array (SCA). Recommended Value '1'	
100		PP_TWC	0	Power ON/OFF Analog memory array (SCA). Recommended Value '0' for ON	
101	*bias_charge_hg*	EN_charge_hg	1	Enable High Gain Shaper. Recommended Value '1'	
102		PP_charge_hg	0	Power ON/OFF High Gain Shaper. Recommended Value '0' for ON	
103		sw/swb_hg_r1<2>	1	R1 value : "000":40k Ohm .. "111":5k Ohm. Default value "100" : 20k Ohm	HG shaper peaking time settings : tp = R1*C1=R2*C2. Recommended value : tp =default=20 ns. Refer Section 3.2.
104		sw/swb_hg_r1<1>	0		
105		sw/swb_hg_r1<0>	0		
106		sw/swb_hg_c1<3>	0	C1 value : "0000": 0.25pF .. "1111": 4pF. Default value : "0011" : 1pF	
107		sw/swb_hg_c1<2>	0		
108		sw/swb_hg_c1<1>	1		
109		sw/swb_hg_c1<0>	1		
110		sw/swb_hg_r2<2>	1	R2 value : "000":800k Ohm .. "111":100k Ohm. Default value "111" : 100k Ohm	
111		sw/swb_hg_r2<1>	1		
112		sw/swb_hg_r2<0>	0		
113		sw/swb_hg_c2<3>	0	C2 value : "0000": 0.1pF ..	

114		sw/swb_hg_c2<2>	0	“1111”: 1.6pF. Default value : “0001” : 0.2pF	
115		sw/swb_hg_c2<1>	0		
116		sw/swb_hg_c2<0>	0		
117	*bias_sca_hg*	EN_SCA_hg	1	Enable High Gain Shaper Analog Memory SCA. Recommended Value ‘1’	
118		PP_SCA_hg	0	Power ON/OFF High Gain Shaper Analog Memory SCA. Recommended Value ‘0’ for ON	
119	*bias inv_hg*	EN_inv_hg	1	Enable High Gain Shaper Invert. Recommended Value ‘1’	
120		PP_inv_hg	0	Power ON/OFF High Gain Shaper Analog Invert. Recommended Value ‘0’ for ON	
121	*bias peak_hg*	EN_peak_hg	1	Enable High Gain Shaper Peak Detector. Recommended Value ‘1’	
122		PP_peak_hg	0	Power ON/OFF High Gain Shaper Peak Detector. Recommended Value ‘0’ for ON	
123	*top bias_channel*	sel_hg<0>	0	Selector (mux) for High Gain (HG) Shaper output to Charge ADC. "00" - HG Shaper peak detector ; “01” – HG Shaper SCA; “10” – Pre-amp SCA Recommended value “00”. Refer Section 3.2.1.	
124		sel_hg<1>	0		
125	*bias ampmeter*	EN_ampmeter	1	Enable Input Ampmeter. Recommended Value ‘0’ for disable	
126		PP_ampmeter	0	Power ON/OFF Input Ampmeter. Recommended Value ‘1’ for OFF	
127		sw_100k	0	Not used. Leave to default value	
128		sw_1000K	1	Not used. Leave to default value	
129	*bias charge lg*	EN_charge_lg	1	Enable Low Gain Shaper. Recommended Value ‘1’	
130		PP_charge_lg	0	Power ON/OFF Low Gain Shaper. Recommended Value ‘0’ for ON	
131		sw/swb_lg_r1<2>	1	R1 value : “000”:40k Ohm .. “111”:5k Ohm. Default value “100” : 20k Ohm	LG Shaper peaking time settings : tp = r1*c1=r2*c2. Recommended value : tp =default=20 ns. Refer Section 3.2.
132		sw/swb_lg_r1<1>	0		
133		sw/swb_lg_r1<0>	0		
134		sw/swb_lg_c1<3>	0	C1 value : “0000”: 0.25pF .. “1111”: 4pF. Default value : “0011” : 1pF	
135		sw/swb_lg_c1<2>	0		
136		sw/swb_lg_c1<1>	1		
137		sw/swb_lg_c1<0>	1		
138		sw/swb_lg_r2<2>	1	R2 value : “000”:800k Ohm .. “111”:100k Ohm. Default value “111” : 100k Ohm	
139		sw/swb_lg_r2<1>	1		
140		sw/swb_lg_r2<0>	1		
141		sw/swb_lg_c2<3>	0	C2 value : “0000”: 0.1pF .. “1111”: 1.6pF.	
142		sw/swb_lg_c2<2>	0		

143		sw/swb_lg_c2<1>	0	Default value : "0001" : 0.2pF
144		sw/swb_lg_c2<0>	1	
145	SCA_lg	EN_SCA_lg	1	Enable Low Gain Shaper Analog Memory. Recommended Value '1'
146		PP_SCA_lg	0	Power ON/OFF Low Gain Shaper Analog Memory. Recommended Value '0' for ON
147	inv_lg	EN_inv_lg	1	Enable Low Gain Shaper Invert. Recommended Value '1'
148		PP_inv_lg	0	Power ON/OFF Low Gain Shaper Analog Invert. Recommended Value '0' for ON
149	peak_lg	EN_peak_lg	1	Enable Low Gain Shaper Peak Detector. Recommended Value '1'
150		PP_peak_lg	0	Power ON/OFF Low Gain Shaper Peak Detector. Recommended Value '0' for ON
151	discri_charge	EN_discri_charge	1	Enable Low Gain Shaper Peak Detector. Recommended Value '1'
152		PP_discri_charge	0	Power ON/OFF Low Gain Shaper Peak Detector. Recommended Value '0' for ON
153		sel_lg	0	Selector (mux) for Low Gain (LG) Shaper output to Charge ADC. '0' - LG Shaper Peak Detector ; '1' – LG Shaper SCA; Recommended value '0'. Refer Section 3.2.1.
154		Sel_Data<0>	0	Selector (mux) for Time & Charge ADC input Time ADC "00","01" – TDC input ; "10" – HG Shaper ; "11" – Test ADC pad; Charge ADC "00","10" – LG shaper ; "01" – HG shaper ; "11" – Test ADC pad; Recommended value "00". TDC -> Time ADC. LG shaper -> Charge ADC Refer Section 4.1.1.
155		Sel_Data<1>	0	
156	temp_sensor	PP_temp_sensor	0	Enable Temperature Sensor. Recommended Value '1'
157		EN_temp_sensor	1	Power ON/OFF Temperature Sensor. Recommended Value '0' for ON
158	discri_ADC_T et Q	EN_ADC_T	1	Enable Discriminator for Time ADC. Recommended Value '1'
159		PP_ADC_T	0	Power ON/OFF Discriminator for Time ADC. Recommended Value '0' for ON
160		EN_ADC_Q	1	Enable Discriminator for Charge ADC. Recommended Value '1'
161		PP_ADC_Q	0	Power ON/OFF Discriminator for Charge ADC. Recommended Value '0' for ON
162	Common block	bypass_NOR64QRS_ValEvt	0	Event validation for noise rejection. '0' – val_evt pad and Charge Trigger NOR (NOR64Q) as event validation; '1'- val_evt only as validation. Recommended value '0' as validation comes from charge trigger.

163		Choice_OR64_BigCpt	0=> NOR64Q	Readout manager loading registers input. '0' – loading sync to Charge Trigger NOR; '1' loading sync to Hit (time) NOR. Recommended value '0' as validation comes from charge trigger.
164		add_delay_NOR64Q	0 => no delay	Add delay to Charge Trigger NOR. '0' – no delay; '1' – 200 ps delay. Recommended value '0' no delay. Delay is only required if noise rejection module doesn't work properly.
165		TimeOutSet<0>	0	Time out setting for noise rejection in additional to 100 ns by default. "00" : No addition Time out; "01": +25 ns; "10": +50 ns; "11": +75 ns Recommended value "00" – No extra time out required. Refer Section 4.1.2.
166		TimeOutSet<1>	0	
167		bypass_RazChnME	0	Bypass internal noise rejection module and use RazChnGlobalb from digital module for reseting ADC SCAs. Recommended value '0' for using internal noise rejection module. Refer Section 4.1.2.
168		disable_RazChnInt	0	Enable/disable reset signal from internal noise rejection module. Recommended value '0' for using internal noise rejection module. Refer Section 4.1.2.
169	Channel 0	mask/maskb	0	Discriminator output masking : '0 - unmask; '1' – mask. Ex : Channel 0 masking "0…01". Multiple channels can be masked simultaneously. Refer Section 3.3.
170	1			
171	2			
…				
232	Channel 63			
233	Channel 0	sw/swb_Ctest	0	Enable/Disable internal charge injection test for 64 channels. Recommended value "0…0" as not required.
234	1	sw/swb_Ctest	0	
…				
296	Channel 63	sw/swb_Ctest	0	
297	Channel 0	6bitdac<0>	0	Time threshold fine tuning. Ex with Time Threshold (VthT : 1.273V) Max Value : "0000000":1.267 V Min Value :"1111111":1.229 V DAC step : 0.6mV Recommended value will be decided with test. Refer Section 3.3.
298		6bitdac<1>	0	
299		6bitdac<2>	0	
300		6bitdac<3>	0	
301		6bitdac<4>	0	
302		6bitdac<5>	0	
303	Channel 1	6bitdac<0>	0	

304		6bitdac<1>	0	
305		6bitdac<2>	0	
306		6bitdac<3>	0	
307		6bitdac<4>	0	
308		6bitdac<5>	0	
...		....	...	...
669	Channel 62	6bitdac<0>	0	
670		6bitdac<1>	0	
671		6bitdac<2>	0	
672		6bitdac<3>	0	
673		6bitdac<4>	0	
674		6bitdac<5>	0	
675	Channel 63	6bitdac<0>	0	
676		6bitdac<1>	0	
677		6bitdac<2>	0	
678		6bitdac<3>	0	
679		6bitdac<4>	0	
680		6bitdac<5>	0	
681	Channel 0	inpdac<0>	0	ASIC input DAC for Channel 0: "00000000" = 0.2V, "11111111" =2.2V Recommended value depends on calibration. Refer Section 3.1.1.
		inpdac<1>	0	
		inpdac<2>	0	
		inpdac<3>	0	
		inpdac<4>	0	
		inpdac<5>	0	
		inpdac<6>	0	
		inpdac<7>	0	
689		cmd/cmdb_inpdac<0>	1	Input DAC Channel 0 enable. Recommended value '1' for enable.
690	Channel 1	inpdac<0>	0	ASIC input DAC for Channel 1: "00000000" = 0.2V, "11111111" =2.2V Recommended value depends on calibration. Refer Section 3.1.1.
		inpdac<1>	0	
		inpdac<2>	0	
		inpdac<3>	0	
		inpdac<4>	0	
		inpdac<5>	0	
		inpdac<6>	0	
		inpdac<7>	0	
		cmd/cmdb_inpdac<1>	1	Input DAC Channel 1 enable. Recommended value '1' for enable.
...		...	....	....

1248	Channel 63	inpdac<0>	0	ASIC input DAC for Channel 1: "00000000" = 0.2V, "11111111" =2.2V Recommended value depends on calibration. Refer Section 3.1.1.
1249		inpdac<1>	0	
1250		inpdac<2>	0	
1251		inpdac<3>	0	
1252		inpdac<4>	0	
1253		inpdac<5>	0	
1254		inpdac<6>	0	
1255		inpdac<7>	0	
1256		cmd/cmdb_inpdac<63>	1	Input DAC Channel 63 enable. Recommended value '1' for enable.

Table 6 – Slow Control register parameters

General notes about Slow Control parameters:

- In most cases, Slow Control bits implementations are not required for PP_x, recommended to be left to default value. Refer to Section 5.5 for these SC bits usage.
- Bits #30-37 are also not required to be implemented. Highly recommended to set bit#31 to '1' for less disturbance to an analog front-end.
- Bits #233-296 are not required to be implemented. Recommended to set all bits to '0'.
- The recommended values in Description column are based on the full digital time and charge measurement (Section 1.1.3) usage.
- Values in Default value column are available once the Slow Control reset is asserted: rstb_sc ='0' in Section 5.1.

5.3 Probe register parameters

Bit	Probe Type	Probe Signal	Descriptions
1	analog	channel0	out_6bit-dac
2	analog	channel1	out_6bit-dac
...	analog	...	out_6bit-dac
64	analog	channel63	out_6bit-dac
65	analog	channel 0	out_pa
66	analog	channel1	out_pa
...	analog	...	out_pa
128	analog	channel63	out_pa
129	analog	channel0	out_ramp_tdc
130	analog	channel1	out_ramp_tdc
	analog	...	out_ramp_tdc
192	analog	channel63	out_ramp_tdc
193	analog	channel0	out_hg
194	analog	channel1	out_hg
	analog	....	out_hg
256	analog	channel63	out_hg
257	analog	channel0	out_lg
258	analog	channel1	out_lg
	analog	...	out_lg
320	analog	channel63	out_lg
321	digital	channel0	out_trig_QRS
322	digital	channel1	out_trig_QRS
	digital	...	out_trig_QRS
384	digital	channel63	out_trig_QRS
385	digital	channel0	end_Q
386	digital	channel1	end_Q
	digital	...	end_Q
448	digital	channel63	end_Q
449	digital	channel0	end_T
450	digital	channel1	end_T
	digital	...	end_T
512	digital	channel63	end_T
513	digital	channel0	RazChnb
514	digital	channel1	RazChnb
	digital	...	RazChnb
576	digital	channel63	RazChnb
577	digital	top	startAdcRampb
578	digital	top	NOR64_delayed
579	digital	top	0 / GND

580	digital	top	MsbTs
581	digital	top	0 / GND
582	digital	top	StartConv
583	digital	top	StartReadOutTs
584	digital	top	StartReadOutAdc

Table 7 – Probe register parameters

5.4 Analog read-out

The timing diagram of the read registers is shown in Figure 27. In order to operate the registers, the following 3 inputs are required:

- ck_read : E19 → Clock for shifting read register (<10MHz).
- rstb_sr : A22→ Shift register reset ('0').
- select : A21 → select value either for Slow Control ('1') or Probe/Read ('0') registers. '0' for analog readout.

During the operations, "select" pin has to be set at '0' level so that the correct registers for read are selected. It should be noted that arriving at Channel 63, rstb_sr has to be pulled down to '0' in order to restart the readout again.

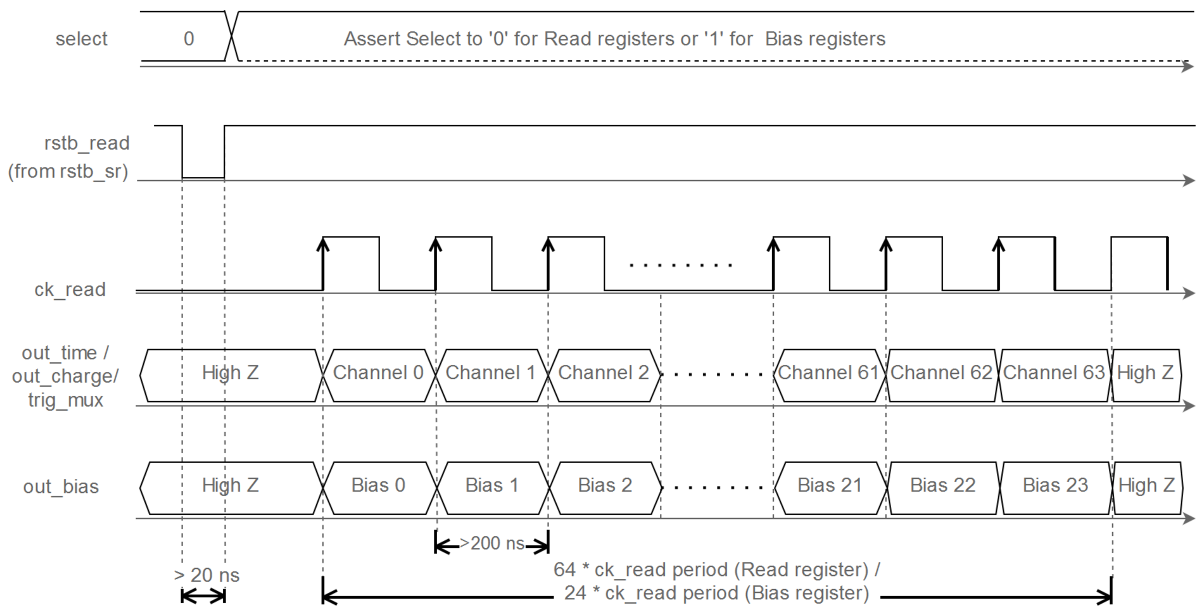


Figure 27 – Read register timing diagram

Read registers are available for reading out multiplexed output which is selected with select ='0'. There are two multiplexed outputs in this ASIC:

- out_time : E16 – Multiplexed output of Time ADC: HG Shaper analog memories (Switched Capacitor Array - SCA)/Peak Detector and Time-to-Amplitude Converter ramp.

- out_charge : E14 – Multiplexed output of Charge ADC: Temperature sensor, HG & LG shapers SCA/Peak Detector.

- trig_mux : C23 – Multiplexed Time Trigger output

It should be noted that the signal selection for each multiplexed output will depend on the ASIC slow control parameters. Refer to Section 4.1.1 for full list of available signal selection.

Otherwise if select is set at '1', registers corresponding to selected ASIC bias will be selected. The output of the bias voltage value is located at ball E15, "out_bias".

Pin name	Ball Out	Comments	Probe outputs	Sub address
out_time	E16	Multiplexed output of the HG shaper 64x SCA and TAC ramp	Analog	0-63
out_charge	E14	Multiplexed output of Temperature sensor, HG &LG 64x SCA	Analog	0-63
trig_mux	C23	Multiplexed Time Trigger output	Digital	0-63

Pin name	Ball Out	Comments	Probe outputs	Sub address
out_bias	E15	Bias – "ibm_discri_adc"	Analog	0
-	-	Bias – "ibm_discri_charge"	Analog	1
-	-	Bias – "ibi_discri_charge"	Analog	2
-	-	Bias – "ibi_charge_lg"	Analog	3
-	-	Bias – "ibi_amp"	Analog	4
-	-	Bias – "ibm_amp"	Analog	5
-	-	Bias – "ibo_amp"	Analog	6
-	-	Bias – "ibi_charge_hg"	Analog	7
-	-	Bias – "ibo_charge_hg"	Analog	8
-	-	Bias – "ibo_sca_pa"	Analog	9
-	-	Bias – "ibi_cs_tds"	Analog	10
-	-	Bias – "ibm_cs_tdc"	Analog	11
-	-	Bias – "ibo_cs_tdc"	Analog	12
-	-	Bias – "ib_fol_discri"	Analog	13
-	-	Bias – "ibm_discri"	Analog	14
-	-	Bias – "ibm_pa"	Analog	15
-	-	Bias – "ibo_pa"	Analog	16
-	-	Bias – "ib_regul"	Analog	17
-	-	Bias – "ibo_inpdac"	Analog	18
-	-	Bias – "ibm_inpdac"	Analog	19
-	-	Bias – "ibi_inpdac"	Analog	20
-	-	Bias – "ib_step_inpdac"	Analog	21
-	-	Bias – "ib_source_inpdac"	Analog	22
-	-	N/A	Analog	23

Table 8 – Read (Top) and Bias (Bottom) registers outputs addresses.

5.5 Power Pulsing

Each unused stage can be disabled to reduce power consumption. This is controlled by the Slow Control bits called "EN_bloc-name" (EN= enable). Moreover, each chip stage can be switched off dynamically thanks to the "power_on" command (pwr_on_x provided by pin AB20/AB22/AC22/C22– refer to Table 12 and Figure 33). This mode is the power pulsing function (Figure 28): for each stage, the slow control bit called "PP_bloc-name" (PP=Power Pulsing) allows bypassing this feature by forcing it ON. (Refer to the truth table – Table 9).

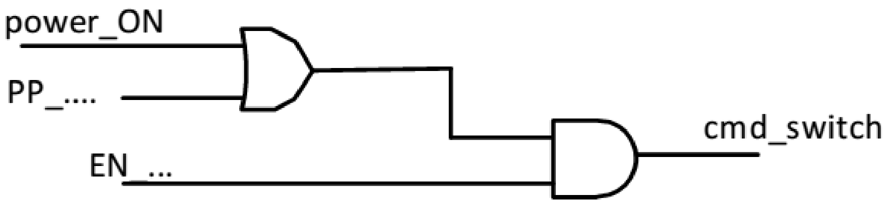


Figure 28 - Power Pulsing control logic

En_... Parameter	PP_... Parameter	Power_ON_x pin	Cmd_switch	Comments
0	X	X	0	Stage disabled – Forced OFF
1	1	X	1	Stage disabled – Forced ON
1	0	1/0	1/0	Power pulsing mode

Table 9 – Power Pulsing logic truth table

6 ASIC I/Os connections

6.1 Front-end connection

SiPM can be connected directly to the ASIC (DC coupled). No external components are required for the detector. This ASIC can accept both polarity of the SiPM signals. The illustrations of the SiPM connections to the ASIC are shown in Figure 29.

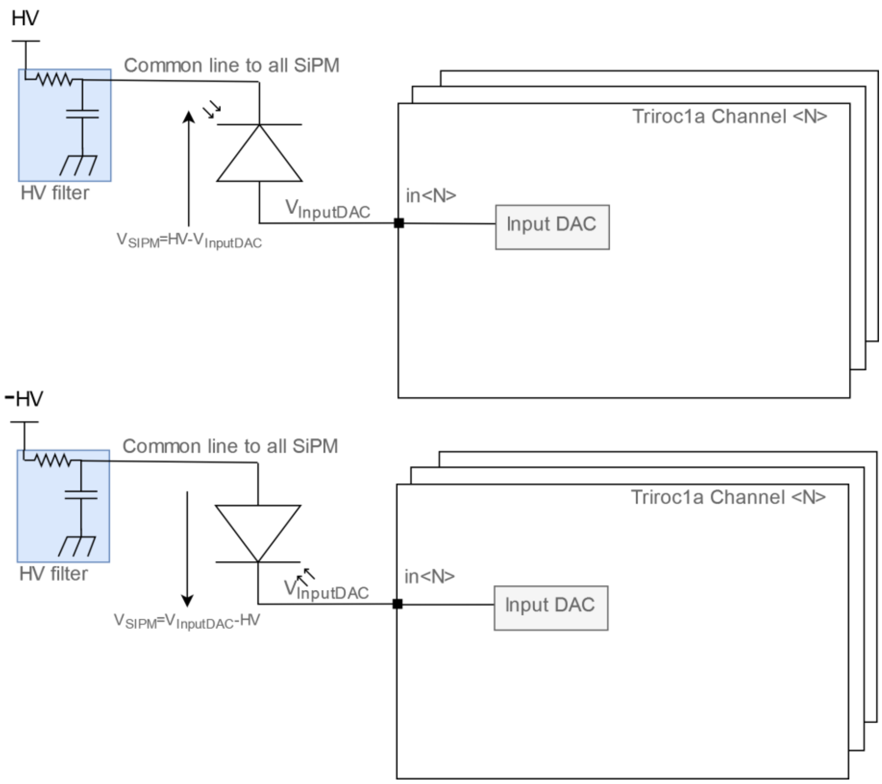


Figure 29 - Triroc1A front-end connections for positive input (Top figure) and negative input (Bottom figure).

6.2 Backend connection

The backend connection contains essentially digital I/Os. The backend connections can be divided into 3 main parts: ASIC controls, digital core I/Os and trigger/analog outputs. Connections for ASIC controls and digital core I/Os are listed in Table 11 and Table 12 respectively. Trigger and analog outputs are listed in Table 10.

Communication standards used for the back-end connections are the following:

- LVCMOS (3.3V) : Point-to-point connection. No external components required.
- LVCMOS (VH) : Point-to-point connection. No external components required. Output voltage can be raised up to 3.3V via VH power supply pins (refer to Section 6.3).
- LVDS : Differential signalling. 100 Ω termination resistor is required at the receiver side.
- Open Collector : Point-to-point connection. Pull up resistor is required (externally or internally) for each output. For certain outputs, 200 kΩ pull-up resistor is available internally. Smaller resistor (e.g. 50-100 Ω) can be added externally in parallel to the existing resistor if required.

6.2.1 Trigger and analog outputs

Trigger outputs are available through NOR64 gate (Pin : NOR64_time – F22) and a multiplexer (Pin : trig_mux – C23) for Time Trigger and only through NOR64 gate (Pin : NOR64_charge – E23) for Charge Trigger. For both NOR64 gate outputs, a 200 kΩ pull up resistors are available internally and resistor down to 1 kΩ can be added externally. On the other hand, trig_mux output for Time Trigger multiplexer is a LVCMOS buffer powered by VH. The Time Trigger multiplexer is managed by Read register (Section 5.4).

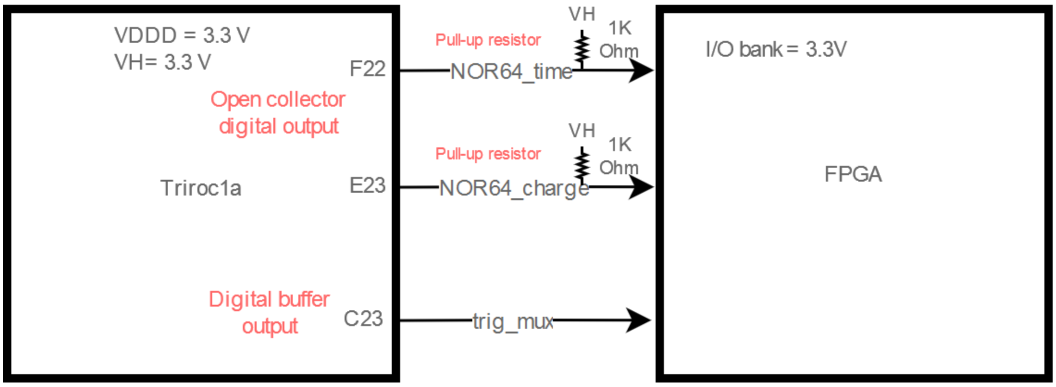


Figure 30 - Triroc1A NOR64 and Time Trigger multiplexer connections

In similar manner as trigger multiplexer output, the analog outputs (out_time - E16, out_charge – E14 and out_bias – E15) are also managed by Read/Bias register. On the other hand, the probe outputs (Analog_probe – E17 and Digital_probe – D22) are managed by Probe register (Section 5.3). The illustration of the various connections for the analog outputs is shown in Figure 31.

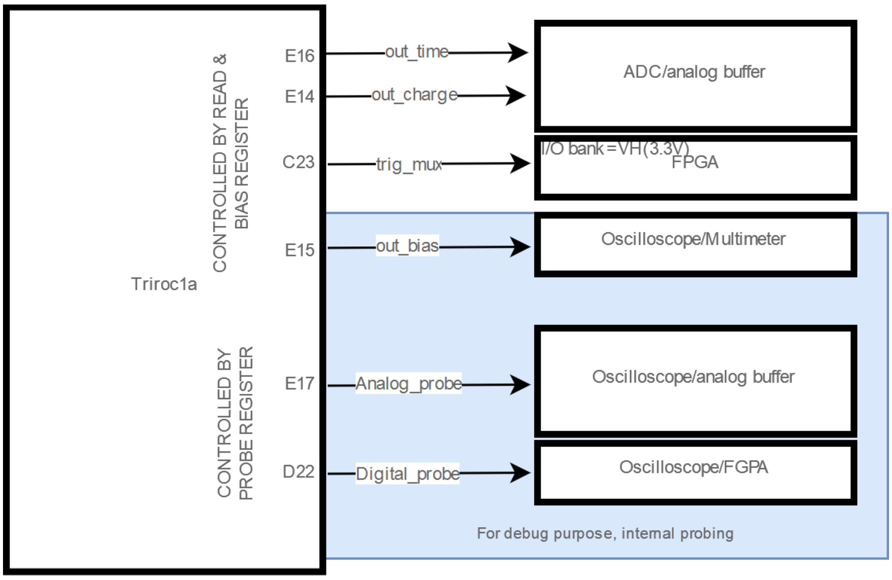


Figure 31 - Triroc 1A analog multiplexer outputs and Probe connections

The trigger connections and analog outputs are listed in Table 10.

Ball Out	Pin Name	I/O	Standard	Description
F22	NOR64_time	Output	Open Collector	Time trigger 64-channel NOR
E23	NOR64_charge	Output	Open Collector	Charge trigger 64-channel NOR
D22	D_probe	Output	LVCMOS (1.5V)	Digital signals probe
C23	Trig_MUX	Output	LVCMOS (1.5V)	Time Trigger multiplexed output
E16	Out_time	Output	Analog Output	Time ADC multiplexed output
E14	Out_charge	Output	Analog Output	Charge ADC multiplexed output
E15	Out_bias	Output	Analog Output	Bias register multiplexed output
E17	Analog_Probe	Output	Analog Output	Analog signal output monitoring

Table 10 – Trigger and analog outputs

6.2.2 ASIC controls

The connections described here are used for sending parameters and setting the ASIC. The description of each pin is provided in table below:

Ball Out	Pin Name	I/O	Standard	Description
AB20	pwron_dac	Input	LVCMOS (3.3V)	Dual 10-bit DACs power on
AC21	hold	Input	LVCMOS (3.3V)	External ADC Hold input
AB21	ext_trig	Input	LVCMOS (3.3V)	External Time Trigger input
C22	pwr_on_d	Input	LVCMOS (3.3V)	Digital part (LVDS transmitter) power on
B23	sr_out	Output	LVCMOS (3.3V)	Shift Output for Slow Control registers (select='1') or Probe registers (select='0')
A23	sr_in	Input	LVCMOS (3.3V)	Shift Input for Slow Control registers (select='1') or Probe registers (select='0')
B22	load_sc	Input	LVCMOS (3.3V)	Slow Control load signal for input DACs
A22	rstb_sr	Input	LVCMOS (3.3V)	Reset for Slow Control registers (select='1') or Probe registers (select='0')
B21	ck_sr	Input	LVCMOS (3.3V)	Clk for Slow Control registers (select='1') or Probe registers (select='0')
A21	select	Input	LVCMOS (3.3V)	Select signal for ck_read, ck_sr, rstb_sr, sr_in and sr_out
E19	ck_read	Input	LVCMOS (3.3V)	Clk for bias (select='1') or Read (select='0') registers
E18	sel_monitoring	Input	LVCMOS (3.3V)	Select leakage current/temperature monitoring

Table 11 – Backend connections and ASIC control

The illustration of the I/O connections for controlling the ASIC is shown in Figure 32. It concerns mostly the interface for accessing Slow Control/Probe and Read/Bias registers (refer Section 5).

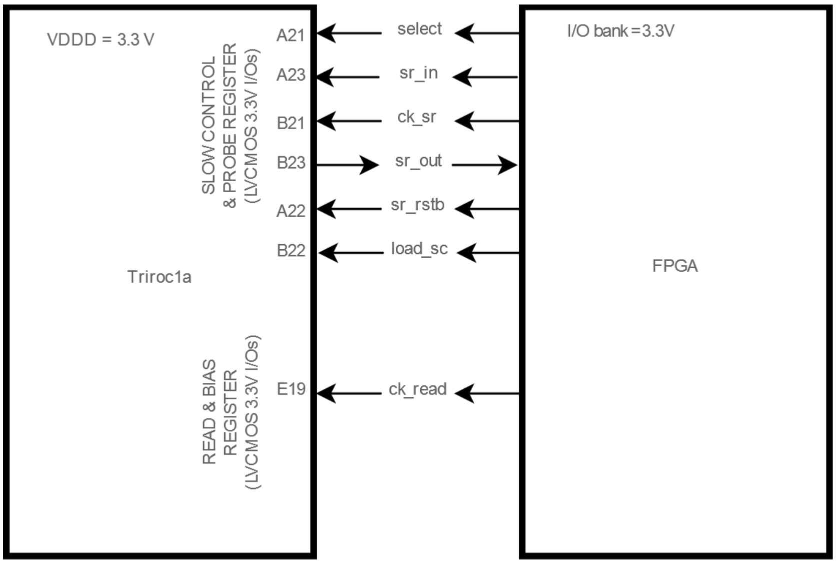


Figure 32 - Triroc1A Slow Control, Probe, Read and Bias registers interface connection

On the other hand, the interface for Power Pulsing and external controls (external Hold, external trigger etc…) are illustrated in Figure 33.

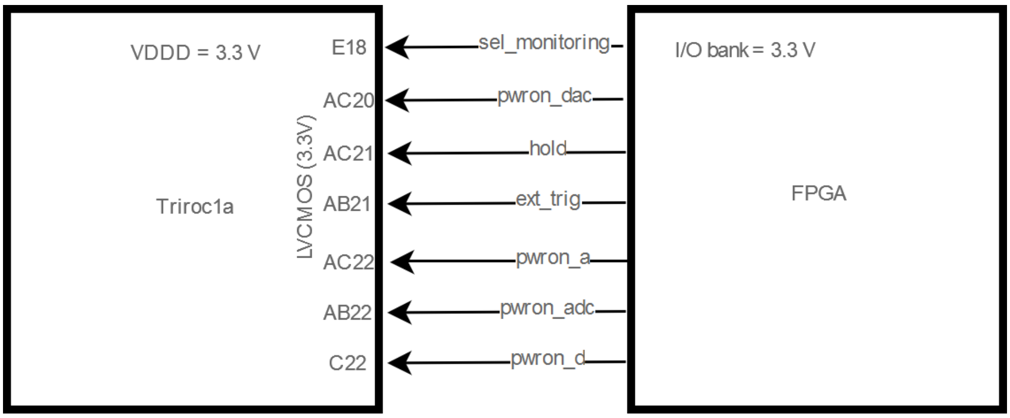


Figure 33 - Triroc1A ASIC controls connection

6.2.3 *Digital Core I/O*

The pins for digital core I/Os and communication standard are listed in Table 12.

Ball Out	Pin Name	I/O	Standard	Description
V22	OvfCptTop	Output	LVCMOS (3.3V)	Digital core top manager counter overflow
W23	ck_160n	Input	LVDS	160 MHz clock (Digital Core)
V23	ck_160p	Input	LVDS	
U23	ck_40n	Input	LVDS	40 MHz clock (Time Stamp)
T23	ck_40p	Input	LVDS	
T22	resetb	Input	LVCMOS (3.3V)	Digital core reset (active low)

R23	Dout_48_63n	Output	LVDS	Data out for channel 48 – 63
P23	Dout_48_63p	Output	LVDS	
R22	Ton_48_63	Output	Open Collector	Transmit On for channel 48 – 63
P22	ForceConvb	Input	LVCMOS (3.3V)	Digital core force conversion external input (active low)
N23	Dout_32_47n	Output	LVDS	Data out for channel 32 – 47
M23	Dout_32_47p	Output	LVDS	
N22	Ton_32_47	Output	Open Collector	Transmit On for channel 32 – 47
M22	RazChn	Input	LVCMOS (3.3V)	Digital core channel trigger reset external input
L23	Dout_16_31n	Output	LVDS	Data out for channel 16 – 31
K23	Dout_16_31p	Output	LVDS	
L22	Ton_16_31	Output	Open Collector	Transmit On for channel 16 – 31
J23	Dout_0_15n	Output	LVDS	Data out for channel 0 – 15
H23	Dout_0_15p	Output	LVDS	
J22	Ton_0_15	Output	Open Collector	Transmit On for channel 0 – 15
H22	StartSyst	Input	LVCMOS (3.3V)	Digital core start conversion external input
G23	Dout_Topn	Output	LVDS	Data out for Top Manager: Global Time Stamp
F23	Dout_Topp	Output	LVDS	
G22	Ton_Top	Output	Open Collector	Transmit On for Top Manager
AA23	val_evt_n	Input	LVDS	Time and Charge Trigger fast masking
Y23	val_evt_p	Input	LVDS	

Table 12 – Backend connections – Digital I/Os

Figure 34 show the connections between the data transmission bank (data out and transmission on links) and also the FPGA.

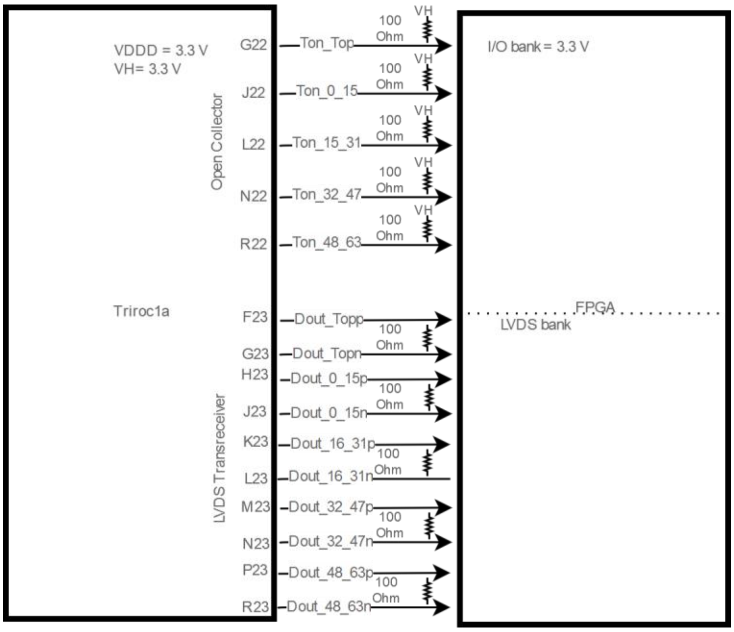


Figure 34 - Triroc1A data transmission connections

The control inputs of the digital part, the clocks and fast trigger masking (pin: val_evtn/p – AA23/Y23) connections with FPGA are shown in Figure 35.

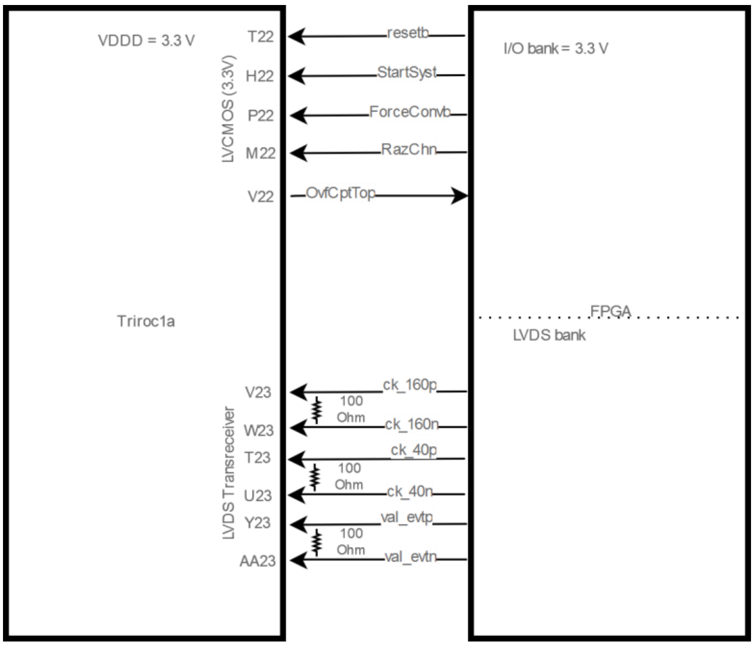


Figure 35 - Triroc1A digital core connections

6.3 Supplies, references, biases

This ASIC requires positive and ground power supplies. Positive power supplies on BGA packaging (refer to ballout in Section 8.1) are noted with a "vdd" prefix followed by the ASIC sections grouping- "i" for inputs, "m" for middle and trigger and "d" for digital and backed. All "vdd" pins must be supplied with 3.3 V and ideally all 3 sections should be powered separately. In worst case, only "vddi" should be powered separately since this pin is powering the pre-amplifier and front-end stage of this ASIC. As usual, all vdd pins should be decoupled with capacitors (e.g. 100 nF and 1 nF) for good operations. Just like the" vdd" the ground pins are also regrouped in similar manner: "gndi", "gndd" and "gndm", and should be connected to ground. In ideal case, these pins should be connected to low impedance ground plane of the PCB housing this ASIC.

A second power rail is required for backend connections of this ASIC. The power supply pins are VH and VL. VH can be connected to any voltage between 1.2 V and 3.3 V. On the other hand VL can be connected to any values lower than 1.2 V. In general practice VH is connected to 3.3 V and VL to ground.

Also in Section 8.1, bias pins are noted with "ib" prefix. Additionally the voltage references are noted with either "vref" or "vcasc" prefixes. These pins don't need external component for normal operations but available in case of adjustment are required for the bias currents or voltage references.

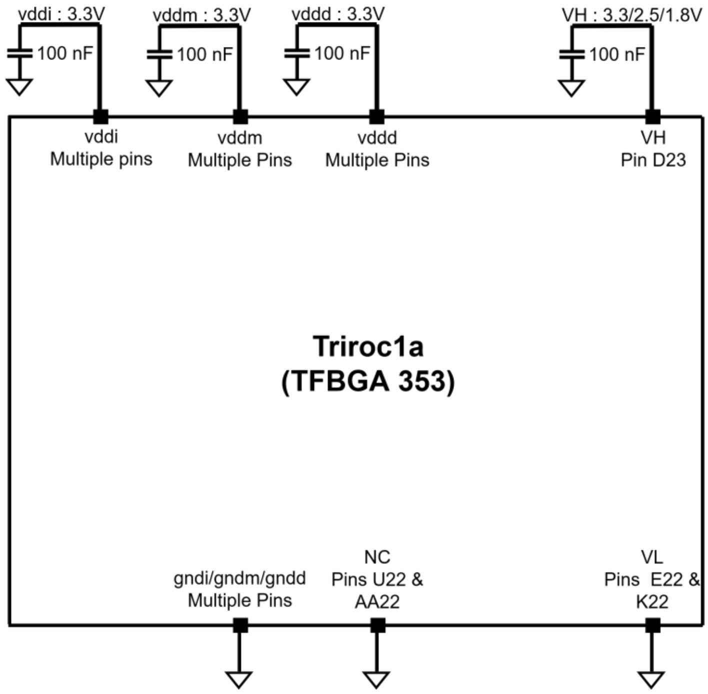


Figure 36 – Triroc1A power supply.

7 ASIC performances

The measurement results in this section have been obtained by injecting charge via capacitors unless stated otherwise.

7.1 Pre-amplifier and High Gain (HG) shaper

The pre-amplifier is a common base amplifier loaded with a resistor for current to voltage conversion. The gain of the pre-amplifier is around 13mV/p.e and 16.5mV/p.e for positive and negative inputs respectively. The waveforms of the pre-amplifier are in shown in Figure 37.

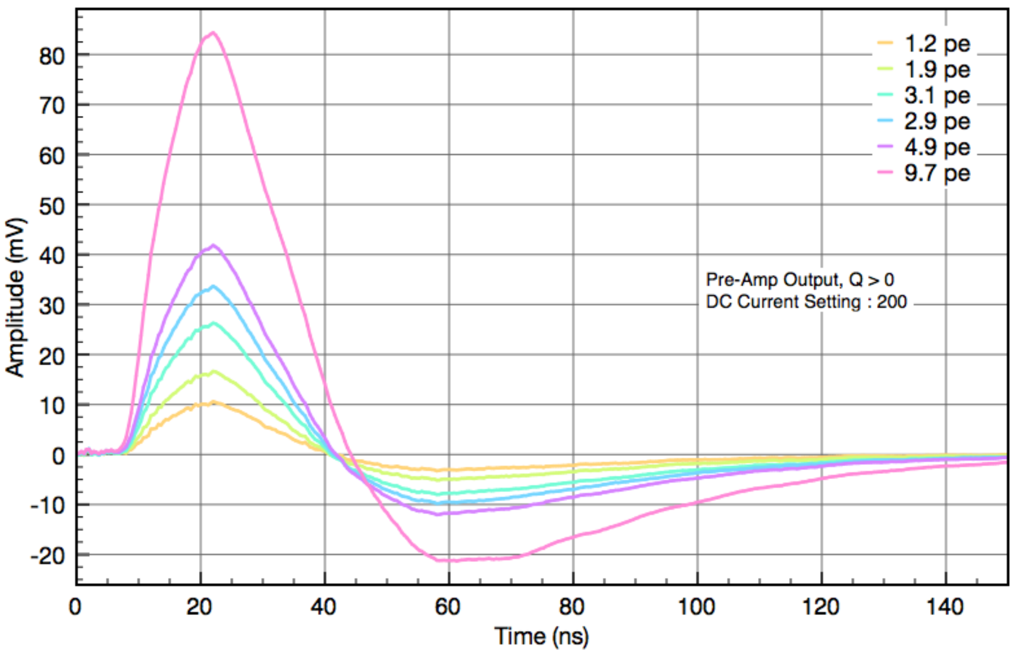


Figure 37 – Pre-amplifier outputs for positive inputs waveform observed via analog probe. Injected charge :1~10 p.e

The linearity of the pre-amplifier is illustrated in Figure 38.

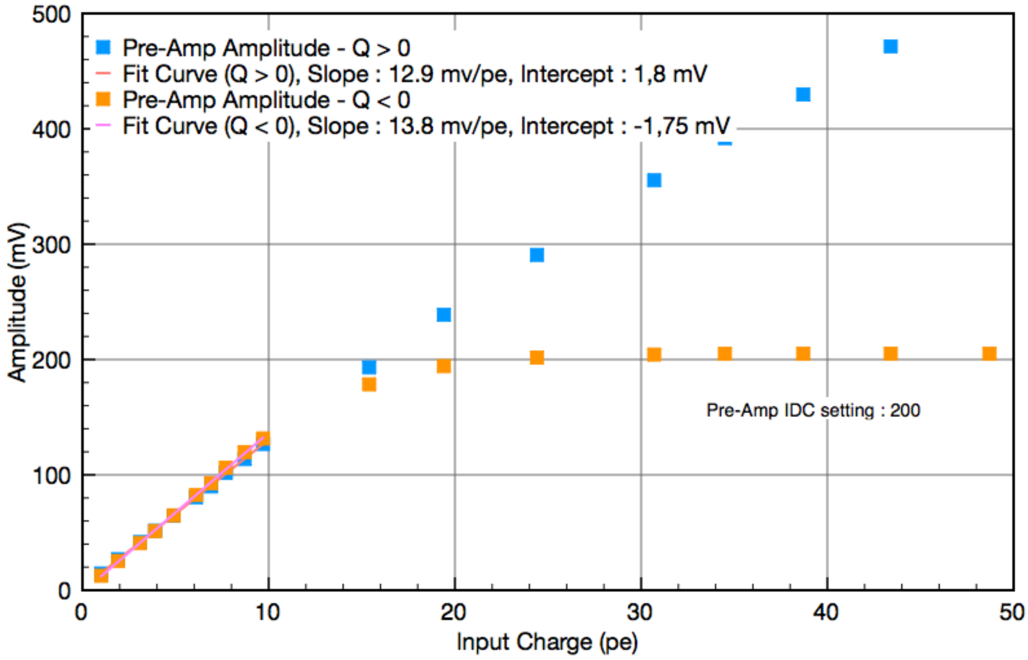


Figure 38 – Pre-amplifier linearity for positive and negative inputs measured via analog probe. 12.9 mv/p.e for positive input and 13.8mv/p.e for negative input.

The pre-amplifier outputs are sent to Trigger Time (see Triggering Scheme – Section 3.3) and the High Gain (HG) shaper for low charge measurements (Section 3.2.1).

This shaper is used for measuring input charge up to 100 photoelectrons (p.e.). HG shaper design is a typical CR-RC shaper. The measurement results of HG shaper are shown in the following figures.

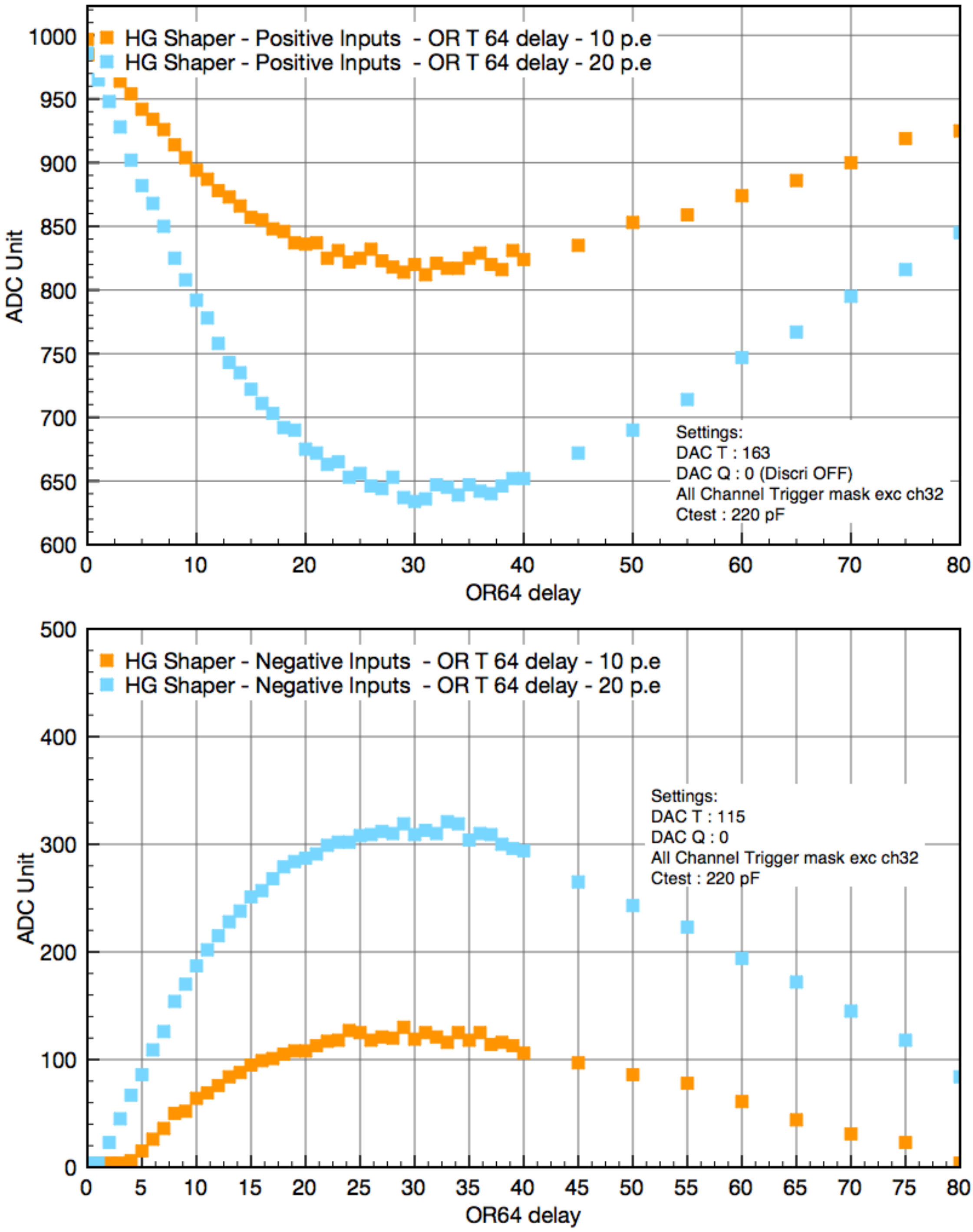


Figure 39 – HG shaper signal reconstruction via internal ADC at various trigger delay for positive input (top figure) and negative input (bottom figure). Settings : R1 : 20 kOhm, C1 : 1 pF ; R2 : 100 kOhm, C2 : 200 fF.

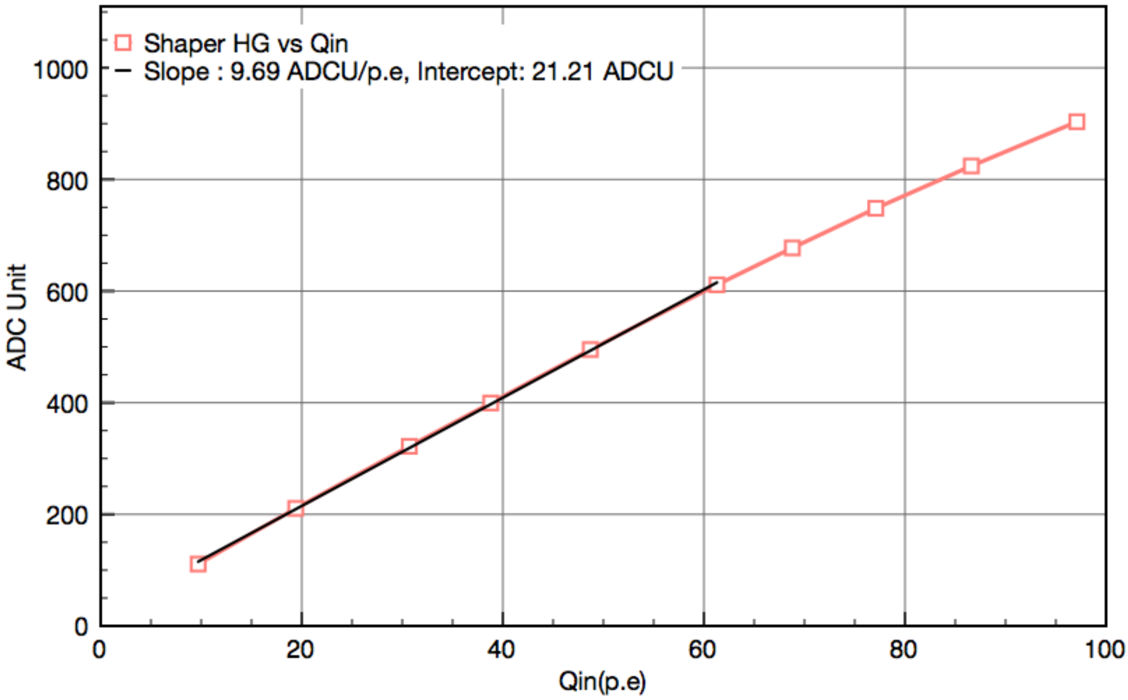


Figure 40 – HG Shaper linearity measurement up to 100p.e. Settings : R1 : 20 kOhm, C1 : 1 pF ; R2 : 100 kOhm, C2 : 200 fF.

7.2 Low Gain (LG) shaper

This shaper's input is coming directly from the detector (Section 3.2). Since the input is not amplified, the shaper will saturate later than HG shaper. Therefore LG shaper is suitable for measuring input charges higher than 100 p.e. The plot below illustrates the linearity of LG shaper.

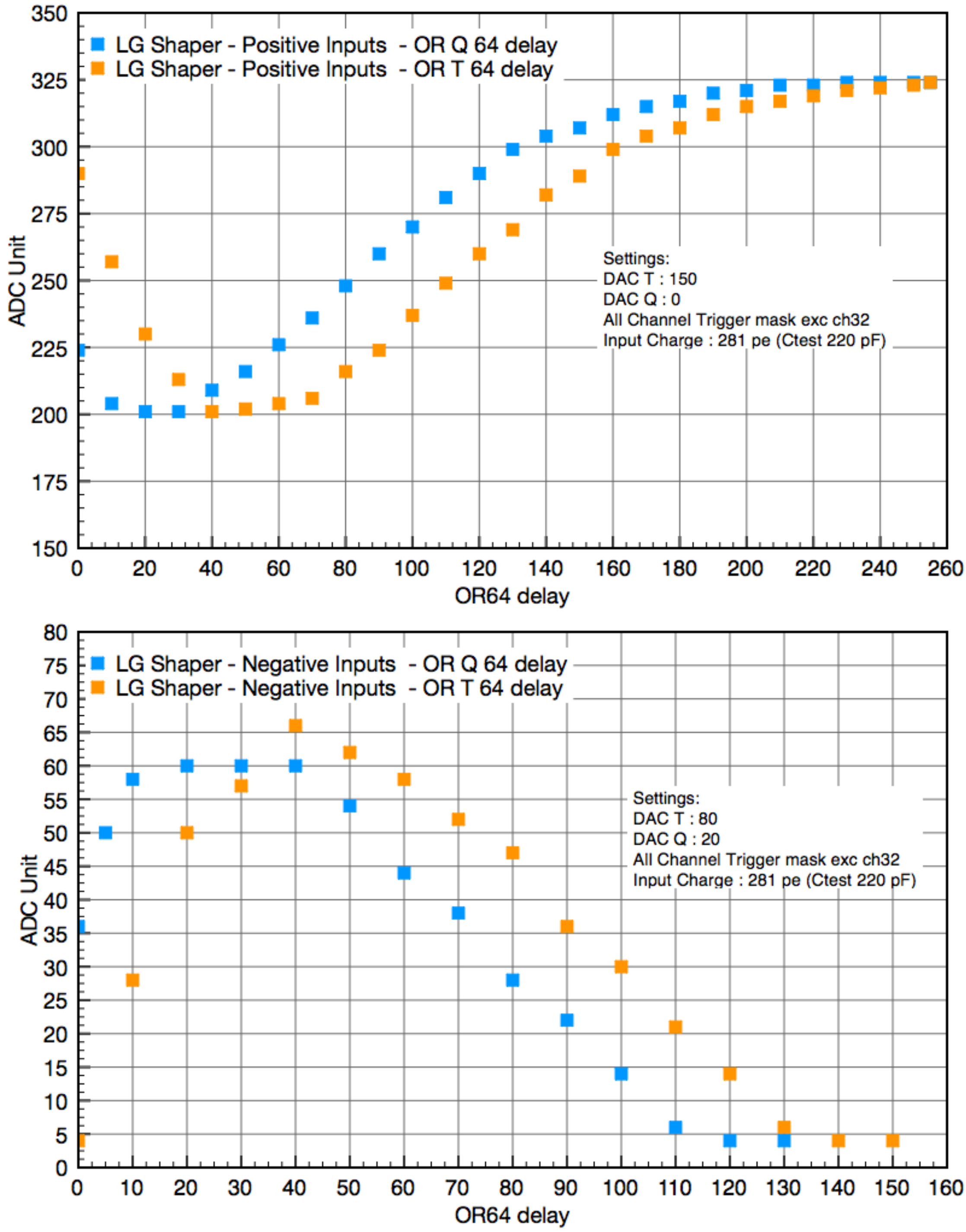


Figure 41 - LG shaper signal reconstruction via internal ADC at various trigger delay for positive input (top figure) and negative input (bottom figure). Settings : R1 : 20 kOhm, C1 : 0.25 pF ; R2 : 100 kOhm, C2 : 200 fF.

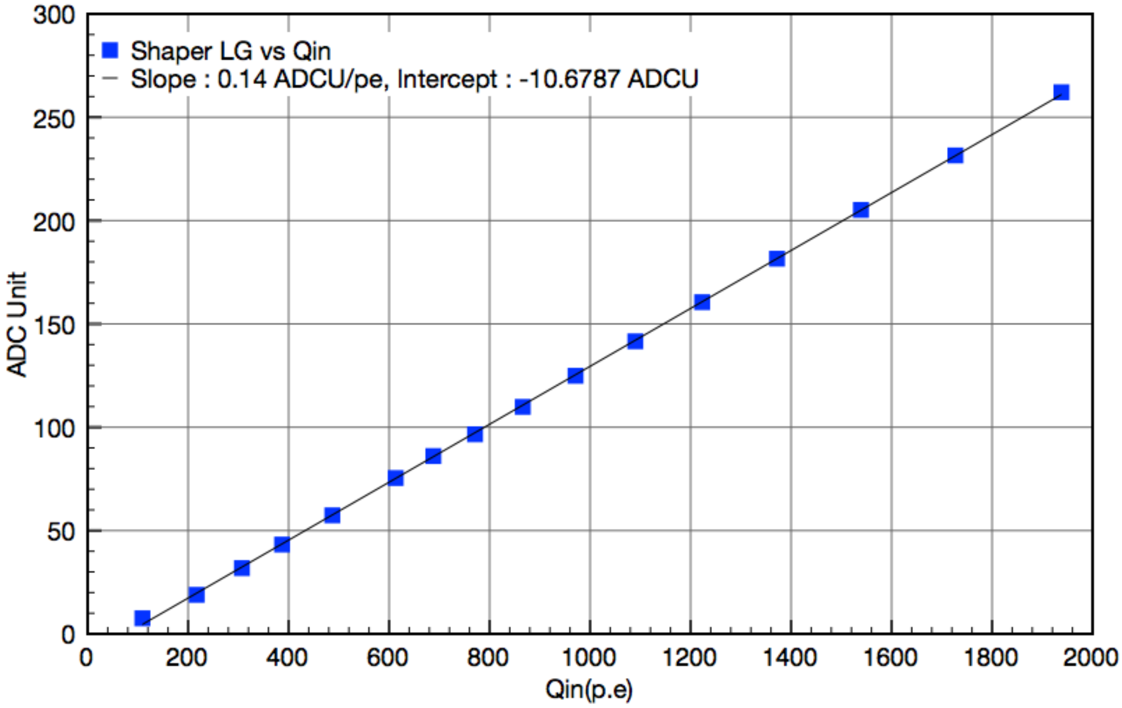


Figure 42 - HG Shaper linearity measurement up to 2000p.e.. Settings : R1 : 20 kOhm, C1 : 0.25 pF ; R2 : 100 kOhm, C2 : 200 fF.

7.3 Time Trigger efficient and jitter

Time Trigger efficiency has been measured by scanning the trigger threshold (DAC) vs input charges. The efficiency or "s-curve" plots have been produced in Figure 43.

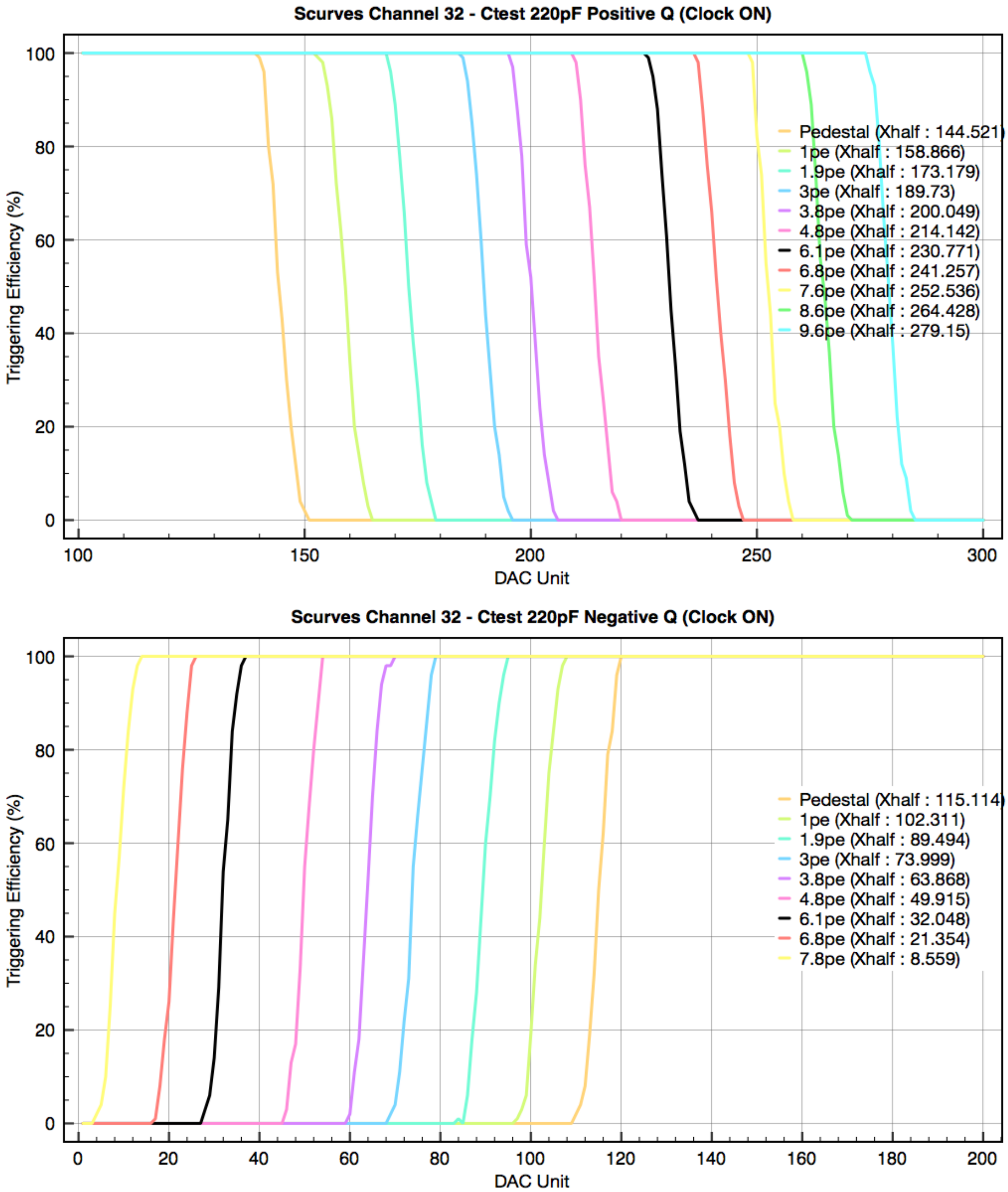


Figure 43 - Time Trigger S-curves vs input charge (up to ~10p.e) for positive input (top figure) and negative input (bottom figure).

As shown in Figure 43, the pre-amplifier has a relatively good linearity and could trigger down to 1 p.e in the best measurement setup. However in normal operation of the ASIC (e.g. 64 channels unmasked, charge validation enabled,...) minimum trigger will be between 5 to 10 p.e.

The extracted pre-amplifier gain from measurements in Figure 43 yield the values of 12.7 mV (13.92 DAC unit)/p.e and 12.74 mV (13.92 DAC unit) /p.e respectively for positive and negative input configurations.

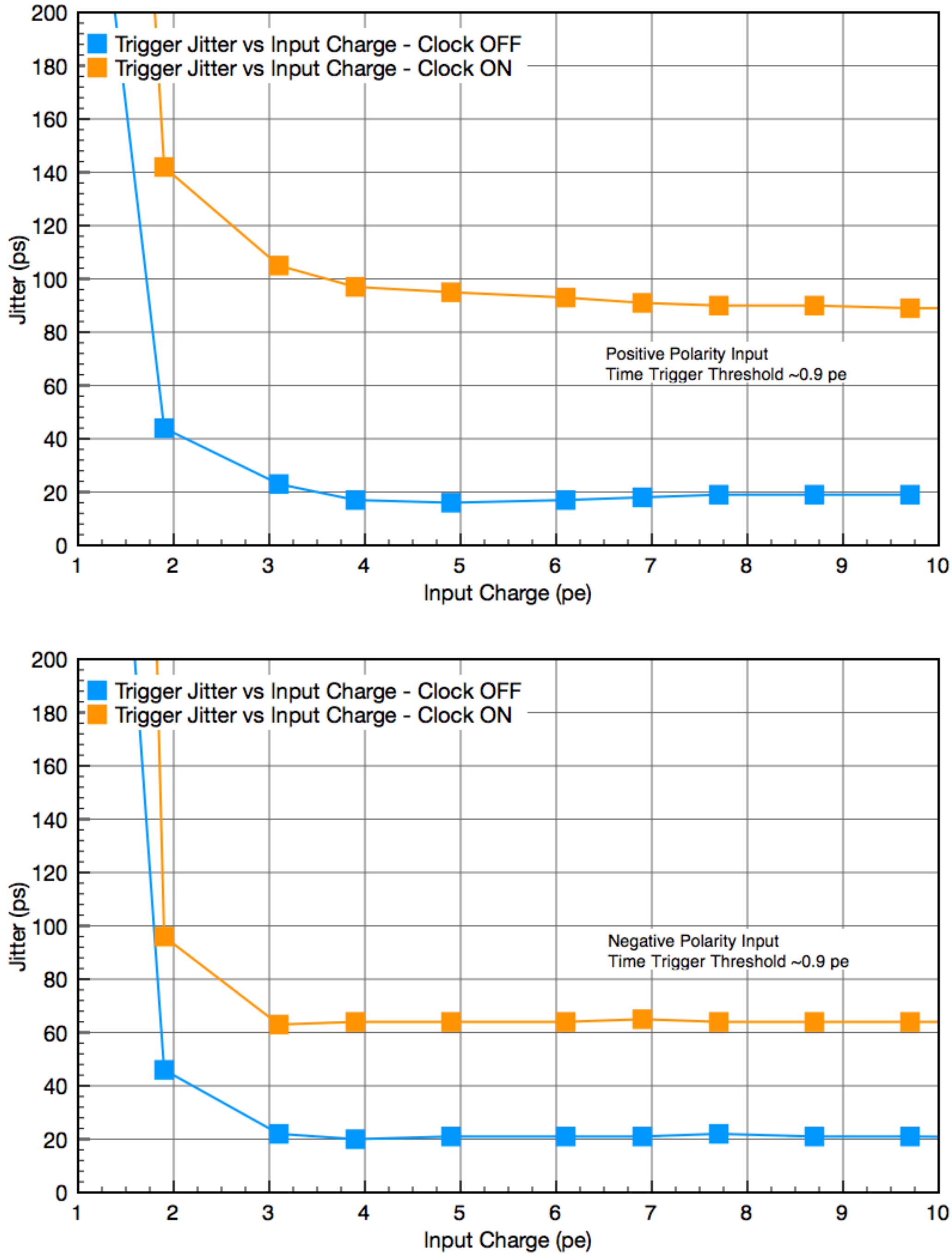
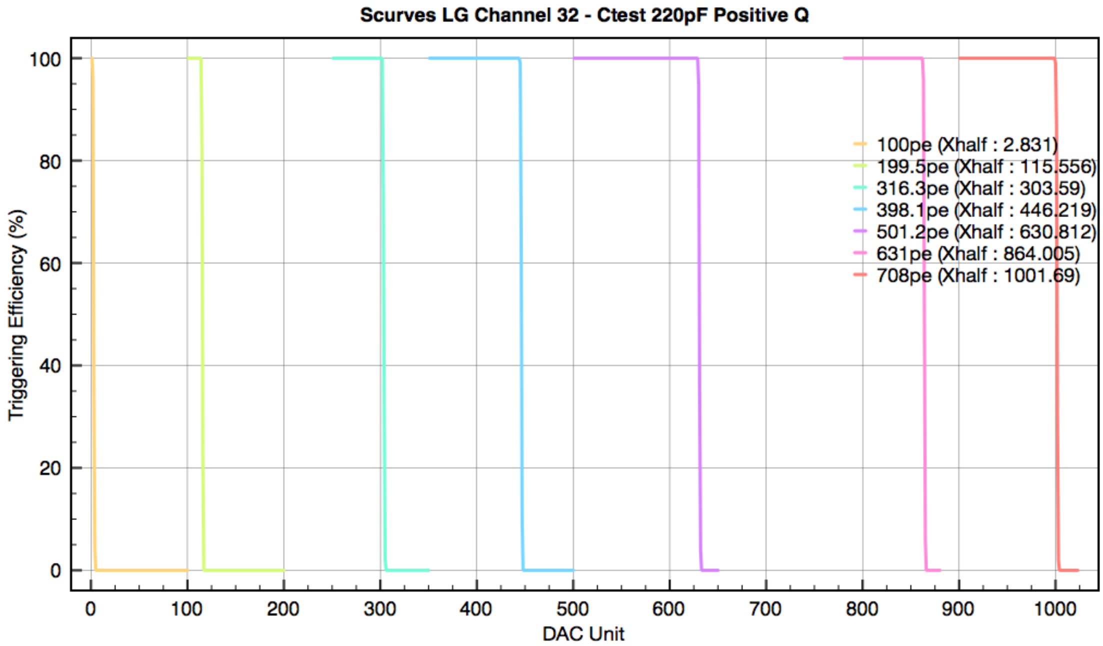


Figure 44 – Time trigger jitter for positive (top figure) and negative (bottom figure) input. Threshold is around 0.9 p.e.

From Figure 44, the jitter for both input configurations increased with clocks enable on the chip. For inputs higher than 4p.e, the jitter with clocks enable is round 90 ps and 65 ps for positive and negative inputs respectively.

7.4 Charge Trigger efficiency

Charge Trigger efficiency has been measured for both input polarity and shown in Figure 45. Minimum input signal required for this trigger would be in the order of ~100 p.e. as shown in the measurement.



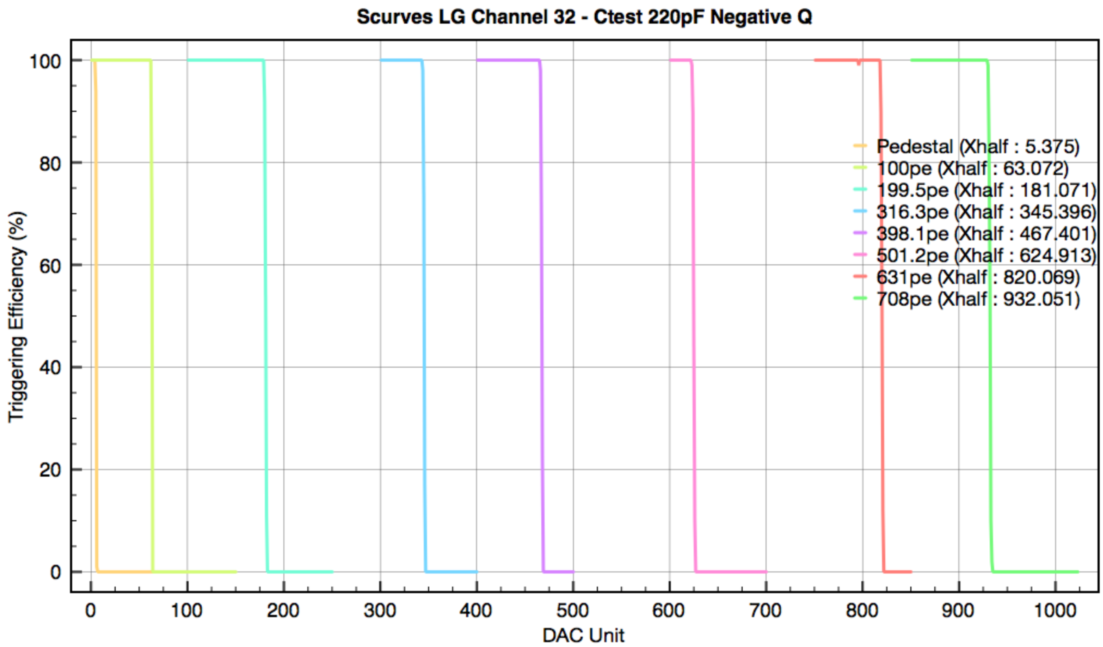


Figure 45 - Charge Trigger S-curves vs input charge (up to ~708p.e) for positive input (top figure) and negative input (bottom figure).

7.5 Coincidence timing resolution

The time difference between 2 channels has been measured by injecting charges directly to the ASIC. Charge injections have been performed synchronously and asynchronously w.r.t to the 40MHz TDC reference clock.

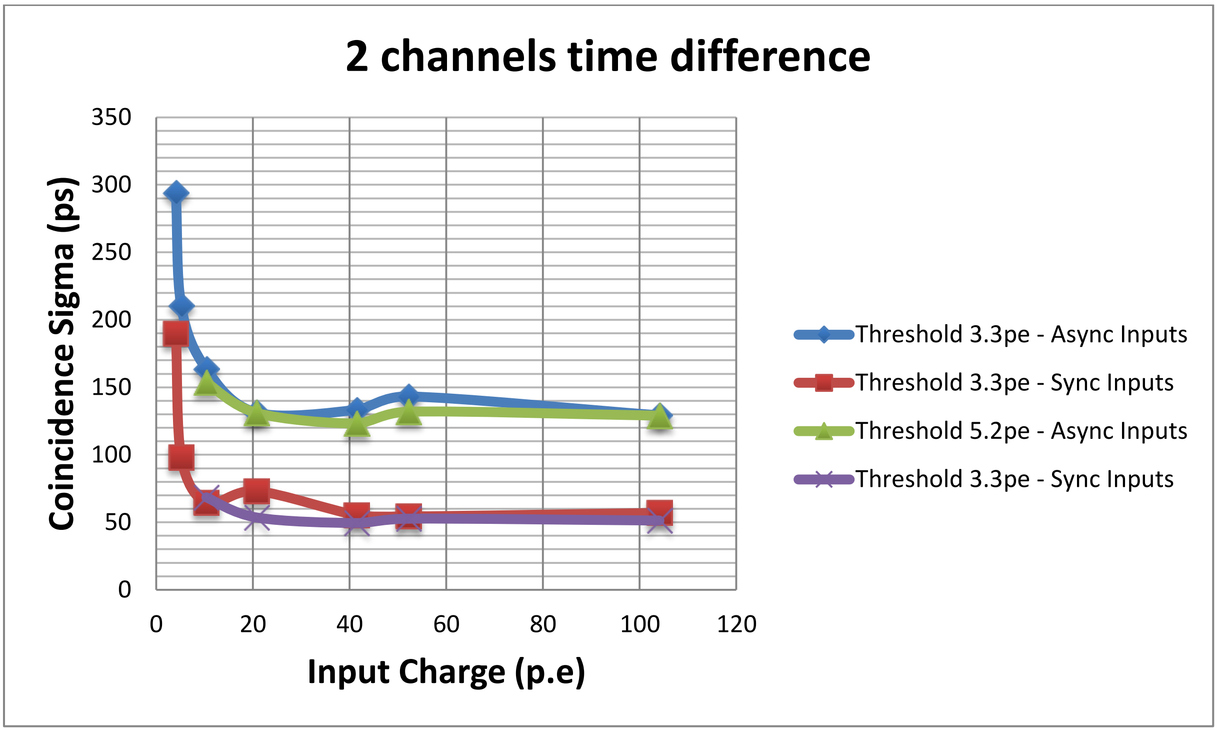


Figure 46 – Time difference for 2 channels. Charge injection via capacitors directly to the ASIC.

Depending on the charge injection method, the timing difference can be up to 150 ps (sigma) or 350 ps (FWHM).

7.6 SiPM readout

Measurements with SiPM array have been carried out with LYSO crystal (1:1 detector coupling) and Germanium isotope.

7.6.1 Energy resolution

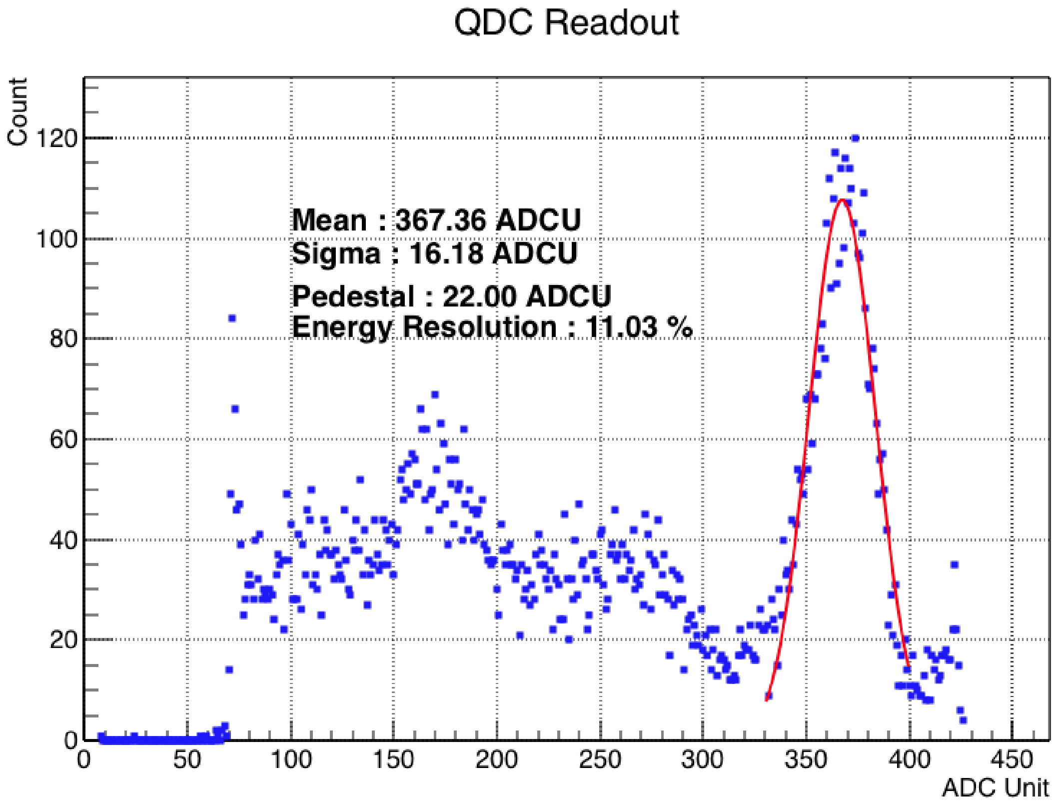


Figure 47 – Charge measurement with Advansid SiPM array and Ge radioactive source. Energy resolution is about 11.03% (without correction).

The measured energy measurement is about 11.03% without any correction. The 511keV peak is clearly identified from the measurement.

7.6.2 Coincidence time resolution

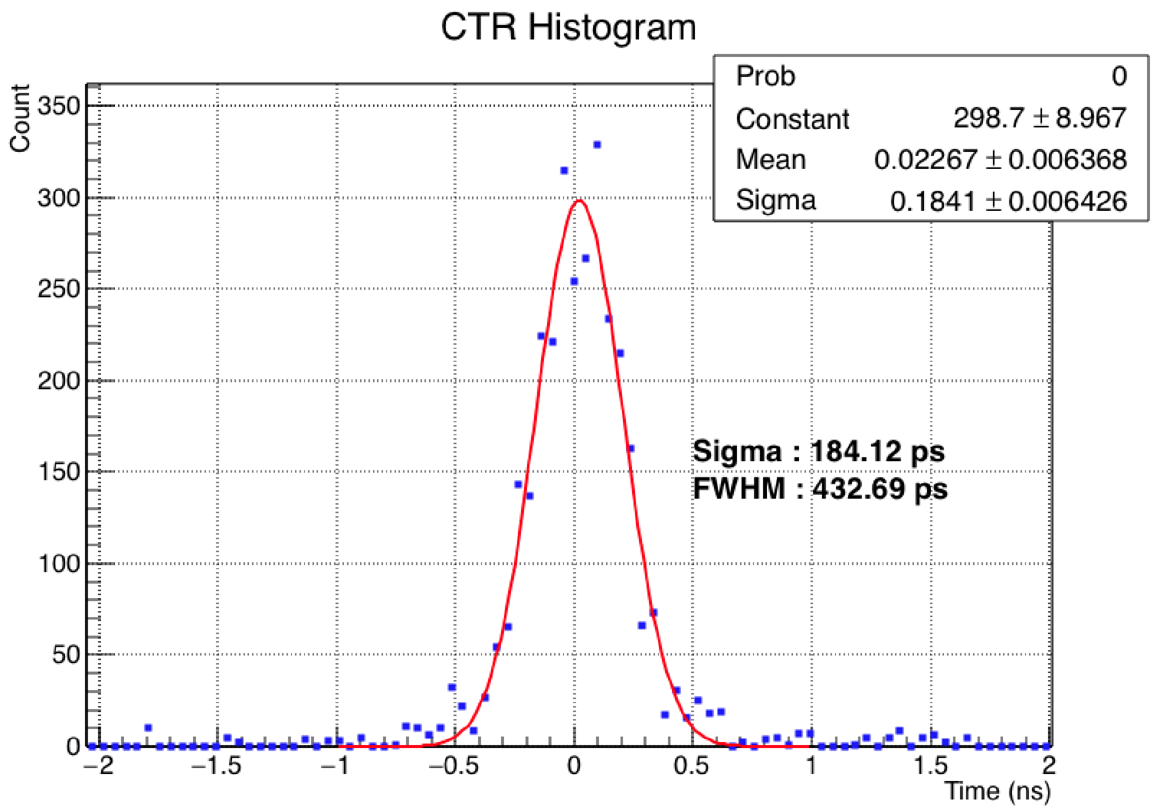


Figure 48– Coincidence time resolution measurement with Advansid SiPM array and Ge radioactive source. Coincidence time resolution is about 432.69 ps (FWHM) or 184.12 ps (sigma).

The measured coincidence time resolution is around 432.69 ps (FWHM) not including any correction strategy.

8 ASIC Pinout

This ASIC is available in 353 balls BGA package and naked dies. All the enumerated pins in this document are based on BGA ball out numbering in Table 13, Figure 49, Figure 50, Figure 51 and Figure 52.

8.1 Pin description

POSITION	BALL OUT	PAD TYPE	PAD NAME	DESCRIPTION	CONNECTION
	vddi	Power	vdd_inpdac	Power Supply 3.3V	vddi with 100nF + 10uF + 470uF decoupling capacitor
	gndi	Power	gndi	Ground	Ground plane
	AB1	Analog Input	in<50>	Channel <50> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB2	Analog Input	in<51>	Channel <51> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC1	Analog Input	in<52>	Channel <52> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC2	Analog Input	in<53>	Channel <53> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB3	Analog Input	in<54>	Channel <54> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC3	Analog Input	in<55>	Channel <55> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB4	Analog Input	in<56>	Channel <56> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
SOUTH	AC4	Analog Input	in<57>	Channel <57> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB5	Analog Input	in<58>	Channel <58> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC5	Analog Input	in<59>	Channel <59> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB6	Analog Input	in<60>	Channel <60> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC6	Analog Input	in<61>	Channel <61> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB7	Analog Input	in<62>	Channel <62> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AC7	Analog Input	in<63>	Channel <63> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AB8	Analog Input	In_ref	Input for reference channel (temperature compensation)	No Connection (N/C)
	gndi	Power	gndi	Ground	Ground plane
	gndm	Power	vssm	Ground	Ground plane

	AC8	Analog Bias	vref_dac_T	Time Trigger threshold DAC reference (1.16V)	Decoupling capacitor 100nF or N/C
	AB9	Analog Output	vth_T	Time Trigger threshold DAC output	Decoupling capacitor 100nF or N/C
	AC9	Analog Bias	vref_dac_Q	Charge Trigger Threshold DAC reference (1.02V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_dac	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	AB10	Analog Bias	iref_dac	Dual 10-bit DAC current reference (2.26V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_dac	Ground	Ground plane
	AC10	Analog Bias	ibo_dac	Dual 10-bit DAC output stage (0.61V)	Decoupling capacitor 100nF or N/C
	AB11	Analog Bias	vcasc1_tdc	TAC ramp 1st cascode reference (1.22V)	Decoupling capacitor 100nF or N/C
	AC11	Analog Bias	ib_otabg	Band Gap ref. OTA bias (0.51V)	Decoupling capacitor 100nF or N/C
	AC12	Analog Bias	vdac_pa	Reference voltage for pre-amp input stage bias (1.56V)	Decoupling capacitor 100nF or N/C
	AB12	Analog Output	vth_delay	Trigger delay DAC output	Decoupling capacitor 100nF or N/C
	W12	Analog Bias	vcasc_discri	Time Trigger discriminator cascode reference (2.32V)	Decoupling capacitor 100nF or N/C
	AC13	Analog Input	inpdac_ext	Input DAC external input	
	W13	Analog Input	in_ctest	Input for internal charge injection	
	AB13	Analog Bias	vcasc2_tdc	TAC ramp 2nd cascode reference (1.7V)	Decoupling capacitor 100nF or N/C
	W14	Analog Input	in_adc	ADC external input	
	gndm	Power	gnd_delay	Ground	Ground plane
	AC14	Analog Bias	ib_delay	Trigger delay DAC current reference bias (0.7V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_delay	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	AB14	Analog Output	vbg	Band Gap ref output (2.52V)	Decoupling capacitor 100nF or N/C
	W15	Analog Bias	vslope_adc_T	Time ADC ramp slope voltage ref (0.27V)	Decoupling capacitor 100nF or N/C
	N/C	N/C	N/C		
	vddm	Power	vdd_adc	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	AC15	Analog Output	ramp_adc_T	Time ADC ramp output	
	gndm	Power	gnd_adc	Ground	Ground plane
	AC16	Analog Output	ramp_adc_Q	Charge ADC ramp output	
	W16	Analog Bias	vref_adc_Q	Charge ADC ramp baseline voltage ref (0.94V)	Decoupling capacitor 100nF or N/C
	AB16	Analog Bias	vslope_adc_Q	Charge ADC ramp slope voltage ref (0.38V)	Decoupling capacitor 100nF or N/C
	AB17	Analog Output	vth_Q	Charge Trigger threshold DAC output	Decoupling capacitor 100nF or N/C
	gndm	Power	vssm	Ground	Ground plane
	gndd	Power	vssd	Ground	Ground plane

	AC17	Analog Bias	ibi_bias_CP	PLL bias	Decoupling capacitor 100nF or N/C
	gndd	Power	gndd	Ground	Ground plane
	AC18	Analog Bias	ibi_comp_CP	PLL bias	Decoupling capacitor 100nF or N/C
	vddd	Power	vddd	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	AB18	Analog Bias	ib_Input_DCshift	PLL bias	Decoupling capacitor 100nF or N/C
	vddd	Power	vdda_pll	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	gndd	Power	gnda_pll	Ground	Ground plane
	gndd	Power	gnd_pll	Ground	Ground plane
	vddd	Power	vdd_pll	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	W17	Analog Bias	vref_CP	PLL bias	Decoupling capacitor 100nF or N/C
	AC19	Analog Bias	ibi_LS	PLL bias	Decoupling capacitor 100nF or N/C
	W18	Analog Bias	ibias_V2I	PLL bias	Decoupling capacitor 100nF or N/C
	AC20	Analog Bias	vcasc_LS	PLL bias	Decoupling capacitor 100nF or N/C
	AB19	Analog Bias	R_V2I	PLL bias	Decoupling capacitor 100nF or N/C
	AB20	Digital Input (LVCMOS)	pwron_dac	Dual 10-bit DACs power on	FPGA/DAQ
	AC21	Digital Input (LVCMOS)	hold	External ADC Hold input	FPGA/DAQ
	AB21	Digital Input (LVCMOS)	ext_trig	External Time Trigger input	FPGA/DAQ
	AC22	Digital Input (LVCMOS)	pwron_a	Analog core power on	FPGA/DAQ
	AB22	Digital Input (LVCMOS)	pwron_adc	ADC power on	FPGA/DAQ
	AC23	Analog Bias	ib_tx	LVDS transmitter bias (0.6V)	Decoupling capacitor 100nF or N/C
	AB23	Analog Bias	vcm_tx	LVDS transmitter common mode (1.2V)	Decoupling capacitor 100nF or N/C
	gndd	Power	vssd	Ground	Ground plane
	Y22	Analog Bias	ibo_rx	LVDS receiver output stage bias (1.2V)	Decoupling capacitor 100nF or N/C
	W22	Analog Bias	ibi_rx	LVDS receiver input stage bias (2V)	Decoupling capacitor 100nF or N/C
	gndd	Power	vssd	Ground	Ground plane
	gndd	Power	gndd2	Ground	Ground plane
EAST	vddd	Power	vddd2	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	AA23	Digital Input (LVDS)	val_evt_n	Time and Charge Trigger fast masking	FPGA/DAQ
	Y23	Digital Input (LVDS)	val_evt_p		FPGA/DAQ
	V22	Digital Output	OvfCptTop	Digital core top manager	FPGA/DAQ

		(LVCMOS)		counter overflow	
	W23	Digital Input (LVDS)	ck_160n	160 MHz clock (Digital Core)	FPGA/DAQ
	V23	Digital Input (LVDS)	ck_160p		FPGA/DAQ
	gndd	Power	vssd	Ground	Ground plane
	U23	Digital Input (LVDS)	ck_40n	40 MHz clock (Time Stamp)	FPGA/DAQ
	T23	Digital Input (LVDS)	ck_40p		FPGA/DAQ
	T22	Digital Input (LVCMOS)	resetb	Digital core reset	FPGA/DAQ
	R23	Digital Output (LVDS)	Dout_48_63n	Data out for channel 48 – 63	FPGA/DAQ
	P23	Digital Output (LVDS)	Dout_48_63p		FPGA/DAQ
	R22	Digital Output (Open-Collector)	Ton_48_63	Transmit On for channel 48 – 63	FPGA/DAQ
	P22	Digital Input (LVCMOS)	ForceConvb	Digital core force conversion external input	FPGA/DAQ
	N23	Digital Output (LVDS)	Dout_32_47n	Data out for channel 32 – 47	FPGA/DAQ
	M23	Digital Output (LVDS)	Dout_32_47p		FPGA/DAQ
	N22	Digital Output (Open-Collector)	Ton_32_47	Transmit On for channel 32 – 47	FPGA/DAQ
	M22	Digital Input (LVCMOS)	RazChn	Digital core channel trigger reset external input	FPGA/DAQ
	L23	Digital Output (LVDS)	Dout_16_31n	Data out for channel 16 – 31	FPGA/DAQ
	K23	Digital Output (LVDS)	Dout_16_31p		FPGA/DAQ
	L22	Digital Output (Open-Collector)	Ton_16_31	Transmit On for channel 16 – 31	FPGA/DAQ
	K22	Power	VL	Low level for digital buffer (Ground)	Ground plane
	J23	Digital Output (LVDS)	Dout_0_15n	Data out for channel 0 – 15	FPGA/DAQ
	H23	Digital Output (LVDS)	Dout_0_15p		FPGA/DAQ
	J22	Digital Output (Open-Collector)	Ton_0_15	Transmit On for channel 0 – 15	FPGA/DAQ
	H22	Digital Input (LVCMOS)	StartSyst	Digital core start conversion external input	FPGA/DAQ
	G23	Digital Output (LVDS)	Dout_Topn	Data out for Top Manager: Global Time Stamp	FPGA/DAQ
	F23	Digital Output (LVDS)	Dout_Topp		FPGA/DAQ
	G22	Digital Output (Open-Collector)	Ton_Top	Transmit On for Top Manager	FPGA/DAQ
	gndd	Power	vssd	Ground	Ground plane
	gndd	Power	gndd	Ground	Ground plane
	vddd	Power	vddd	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor

	F22	Digital Output (Open-Collector)	NOR64_time	Time trigger 64-channel NOR	FPGA/DAQ
	E23	Digital Output (Open-Collector)	NOR64_charge	Charge trigger 64-channel NOR	FPGA/DAQ
	D23	Power	VH	High level for digital buffer (3.3/2.5/1.8V)	VH with 100nF decoupling capacitor
	E22	Power	VL	Low level for digital buffer (Ground)	Ground plane
	D22	Digital Output (LVCMOS)	D_probe	Digital signals probe(monitoring)	FPGA/DAQ
	C23	Digital Output (LVCMOS)	Trig_MUX	Time Trigger multiplexed output	FPGA/DAQ
	vddd	Power	vddd2	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	gndd	Power	gndd2	Ground	Ground plane
	gndd	Power	vssd	Ground	Ground plane
	gndd	Power	gndd	Ground	Ground plane
	gndd	Power	vssd	Ground	Ground plane
	C22	Digital Input (LVCMOS)	pwron_d	Digital part (LVDS transmitter) power on	FPGA/DAQ
NORTH	B23	Digital Output (LVCMOS)	sr_out	Shift Output for Slow Control registers (select='1') or Probe registers (select='0')	FPGA/DAQ
	gndd	Power	vssd	Ground	Ground plane
	A23	Digital Input (LVCMOS)	sr_in	Shift Input for Slow Control registers (select='1') or Probe registers (select='0')	FPGA/DAQ
	B22	Digital Input (LVCMOS)	load_sc	Slow Control load signal for input DACs	FPGA/DAQ
	A22	Digital Input (LVCMOS)	rstb_sr	Reset for Slow Control registers (select='1') or Probe registers (select='0')	FPGA/DAQ
	B21	Digital Input (LVCMOS)	ck_sr	Clk for Slow Control registers (select='1') or Probe registers (select='0')	FPGA/DAQ
	A21	Digital Input (LVCMOS)	select	Select signal for ck_read, ck_sr, rstb_sr,,sr_in and sr_out	FPGA/DAQ
	E19	Digital Input (LVCMOS)	ck_read	Clk for bias (select='1') or Read (select='0') registers	FPGA/DAQ
	E18	Digital Input (LVCMOS)	sel_monitoring	Select leakage current/temperature monitoring	FPGA/DAQ
	E17	Analog Output	A_probe	Analog signal output monitoring	
	gndd	Power	vssd	Ground	Ground plane
	B20	Analog Bias	ib_otaq	Bias out analog output OTA (0.83V)	Decoupling capacitor 100nF or N/C
	E16	Analog Output	out_time	Time ADC multiplexed output	
	B19	Analog Bias	ibi_discri_adc	ADC discriminator input stage bias (0.65V)	Decoupling capacitor 100nF or N/C
	gndd	Power	gnd_sc	Ground	Ground plane

	A20	Analog Bias	ibo_discri_adc	ADC discriminator output stage bias (2.14V)	Decoupling capacitor 100nF or N/C
	E15	Analog Bias	out_bias	Bias register multiplexed output	Decoupling capacitor 100nF or N/C
	B17	Analog Bias	ibo_peak_lg	LG Shaper peak detector output stage bias (2.06V)	Decoupling capacitor 100nF or N/C
	E14	Analog Output	out_charge	Charge ADC multiplexed output	
	A19	Analog Bias	ib_1NA_peak_lg	LG Shaper peak detector reset stage bias (2.42V)	Decoupling capacitor 100nF or N/C
	vddd	Power	vdd_sc	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	B17	Analog Bias	ibi_peak_lg	LG Shaper peak detector input stage bias (0.7V)	Decoupling capacitor 100nF or N/C
	vddd	Power	vddd	Power Supply 3.3V	vddd with 100nF + 10uF + 470uF decoupling capacitor
	A18	Analog Bias	ibo_inv_lg	LG Shaper signal inverter output stage bias (0.68V)	Decoupling capacitor 100nF or N/C
	gndd	Power	gndd	Ground	Ground plane
	B16	Analog Bias	ibi_inv_lg	LG Shaper signal inverter input stage bias (0.68V)	Decoupling capacitor 100nF or N/C
	gndd	Power	vssd	Ground	Ground plane
	gndm	Power	vssm	Ground	Ground plane
	A17	Analog Bias	ibo_discri_charge	Charge Trigger discriminator output stage (2.15V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_discri_adc	Ground	Ground plane
	B15	Analog Bias	ib_sca_lg	LG Shaper SCA output OTA bias (1.27V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_discri_adc	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	A16	Analog Bias	ibo_peak_hg	HG Shaper peak detector output stage bias (2.04V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_discri_charge	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	B14	Analog Bias	ib_1NA_peak_hg	HG Shaper peak detector reset stage bias (2.4V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_discri_charge	Ground	Ground plane
	A15	Analog Bias	ibi_peak_hg	HG Shaper peak detector input stage bias (0.69V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_capa_lg	Ground	Ground plane
	A14	Analog Bias	ibi_inv_hg	HG Shaper signal inverter input stage bias (0.67V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_lg	Ground	Ground plane
	B13	Analog Bias	ibo_inv_hg	HG Shaper signal inverter output stage bias (0.67V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_lg	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	E13	Analog Bias	vref_charge_lg	LG Shaper baseline reference (1.02V, Negative polarity | 2.07V, Postive polarity)	Decoupling capacitor 100nF or N/C
	A13	Analog Bias	ibo_charge_lg	LG Shaper output stage (0.82V, Negative polarity | 0.94V, Postive polarity)	Decoupling capacitor 100nF or N/C

	E12	Analog Bias	vref_charge_hg	HG Shaper baseline reference (1.02V, Negative polarity | 2.06V, Postive polarity)	Decoupling capacitor 100nF or N/C
	B12	Analog Bias	ib_sca_hg	HG Shaper SCA output OTA bias (1.27V)	Decoupling capacitor 100nF or N/C
	E11	Analog Bias	vref_tdc	TAC ramp baseline reference (0.9V)	Decoupling capacitor 100nF or N/C
	A12	Analog Bias	vslope_tdc	TAC ramp slope reference (0.36V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_hg	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	A11	Analog Bias	ibi_tdc	TAC ramp input stage bias (2.23V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_hg	Ground	Ground plane
	B11	Analog Bias	ibo_tdc	TAC ramp output stage bias (0.8V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_capa_hg	Ground	Ground plane
	A10	Analog Bias	ib_6bit_dac	Time Trigger threshold trimming stage bias (0.6V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_tdc	Ground	Ground plane
	A9	Analog Bias	ibo_discri	Time Trigger discriminator output stage (1.37V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_tdc	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	B10	Analog Bias	ibi_discri	Time Trigger discriminator input stage (0.8V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_discri	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	A8	Analog Bias	ibi_pa	Pre-amplifier bias (0.74V)	Decoupling capacitor 100nF or N/C
	gndm	Power	gnd_discri	Ground	Ground plane
	B9	Analog Bias	vref_ota_inpda c	Input DAC OTA reference (0.29V)	Decoupling capacitor 100nF or N/C
	vddm	Power	vdd_pa	Power Supply 3.3V	vddm with 100nF + 10uF + 470uF decoupling capacitor
	B8	Analog Bias	vref_isource	Input DAC current source reference (1.01V)	Decoupling capacitor 100nF or N/C
	gndm	Power	vssm	Ground	Ground plane
	gndi	Power	vssi	Ground	Ground plane
	vddi	Power	vdda_pa	Power Supply 3.3V	vddi with 100nF + 10uF + 470uF decoupling capacitor
	gndi	Power	gndi	Ground	Ground plane
	A7	Analog Input	in<0>	Channel <0> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B7	Analog Input	in<1>	Channel <1> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	A6	Analog Input	in<2>	Channel <2> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B6	Analog Input	in<3>	Channel <3> input	SiPM
	gndi	Power	gndi	Ground	Ground plane

	A5	Analog Input	in<4>	Channel <4> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B5	Analog Input	in<5>	Channel <5> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	A4	Analog Input	in<6>	Channel <6> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B4	Analog Input	in<7>	Channel <7> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	A3	Analog Input	in<8>	Channel <8> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B3	Analog Input	in<9>	Channel <9> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	A2	Analog Input	in<10>	Channel <10> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	A1	Analog Input	in<11>	Channel <11> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B2	Analog Input	in<12>	Channel <12> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	B1	Analog Input	in<13>	Channel <13> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	vddi	Power	vdda_Inpdac	Power Supply 3.3V	vddi with 100nF + 10uF + 470uF decoupling capacitor
WEST	gndi	Power	vssi	Ground	Ground plane
	gndi	Power	gnd_pa	Ground	Ground plane
	C2	Analog Input	in<14>	Channel <14> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	C1	Analog Input	in<15>	Channel <15> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	D2	Analog Input	in<16>	Channel <16> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	D1	Analog Input	in<17>	Channel <17> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	E2	Analog Input	in<18>	Channel <18> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	E1	Analog Input	in<19>	Channel <19> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	F2	Analog Input	in<20>	Channel <20> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	F1	Analog Input	in<21>	Channel <21> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	G2	Analog Input	in<22>	Channel <22> input	SiPM
	gndi	Power	gndi	Ground	Ground plane

	G1	Analog Input	in<23>	Channel <23> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	H2	Analog Input	in<24>	Channel <24> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	H1	Analog Input	in<25>	Channel <25> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	J2	Analog Input	in<26>	Channel <26> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	J1	Analog Input	in<27>	Channel <27> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	K2	Analog Input	in<28>	Channel <28> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	K1	Analog Input	in<29>	Channel <29> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	L2	Analog Input	in<30>	Channel <30> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	L1	Analog Input	in<31>	Channel <31> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	N1	Analog Input	in<32>	Channel <32> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	N2	Analog Input	in<33>	Channel <33> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	P1	Analog Input	in<34>	Channel <34> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	P2	Analog Input	in<35>	Channel <35> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	R1	Analog Input	in<36>	Channel <36> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	R2	Analog Input	in<37>	Channel <37> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	T1	Analog Input	in<38>	Channel <38> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	T2	Analog Input	in<39>	Channel <39> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	U1	Analog Input	in<40>	Channel <40> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	U2	Analog Input	in<41>	Channel <41> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	V1	Analog Input	in<42>	Channel <42> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	V2	Analog Input	in<43>	Channel <43> input	SiPM
	gndi	Power	gndi	Ground	Ground plane

	W1	Analog Input	in<44>	Channel <44> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	W2	Analog Input	in<45>	Channel <45> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	Y1	Analog Input	in<46>	Channel <46> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	Y2	Analog Input	in<47>	Channel <47> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AA1	Analog Input	in<48>	Channel <48> input	SiPM
	gndi	Power	gndi	Ground	Ground plane
	AA2	Analog Input	in<49>	Channel <49> input	SiPM
	gndi	Power	gnd_pa	Ground	Ground plane
	gndi	Power	vssi	Ground	Ground plane

Table 13 - Triroc1A pin descriptions

8.2 BGA 12x12 353 Ball Map

	1	2	3	4	5	6	7	8	9	10	11
A	in<11>	in<10>	in<8>	in<6>	in<4>	in<2>	in<0>	ibi_pa	ibo_discri	ib_64bit_ dac	ibi_tdc
B	in<13>	in<12>	in<9>	in<7>	in<5>	in<3>	in<1>	vref_Isource	vref_ota_Inp dac	ibi_discri	ibo_tdc
C	in<15>	in<14>									
D	in<17>	in<16>									
E	in<19>	in<18>			vddi	gndi	gndi	gndi	gndi	vddm	vref_tdc
F	in<21>	in<20>			vddi	gndi	gndi	gndi	gndi	vddm	vddm
G	in<23>	in<22>			vddi	gndi					
H	in<25>	in<24>			vddi	gndi		gndd	gndd	gndm	gndm
J	in<27>	in<26>			vddi	gndi		gndd	gndd	gndd	gndd
K	in<29>	in<28>			vddi	gndi		gndd	gndd	gndd	gndd
L	in<31>	in<30>			vddi	gndi		gndd	gndd	gndd	gndd
M	gndi	gndi			gndi	gndi		gndd	gndd	gndd	gndd

Figure 49 - North-East side

N	in<32>	in<33>			vddi	gndi		gndd	gndd	gndd	gndd
P	in<34>	in<35>			vddi	gndi		gndd	gndd	gndd	gndd
R	in<36>	in<37>			vddi	gndi		gndd	gndd	gndd	gndd
T	in<38>	in<39>			vddi	gndi		gndd	gndd	gndm	gndm
U	in<40>	in<41>			vddi	gndi					
V	in<42>	in<43>			vddi	gndi	gndi	gndi	gndi	vddm	vddm
W	in<44>	in<45>			vddi	gndi	gndi	gndi	gndi	vddm	vddm
Y	in<46>	in<47>									
AA	in<48>	in<49>									
AB	in<50>	in<51>	in<54>	in<56>	in<58>	in<60>	in<62>	in_ref	vth_T	iref_dac	vcasc1_tdc
AC	in<52>	in<53>	in<55>	in<57>	in<59>	in<61>	in<63>	vref_dac_T	vref_dac_Q	ibo_dac	ib_otag
	1	2	3	4	5	6	7	8	9	10	11

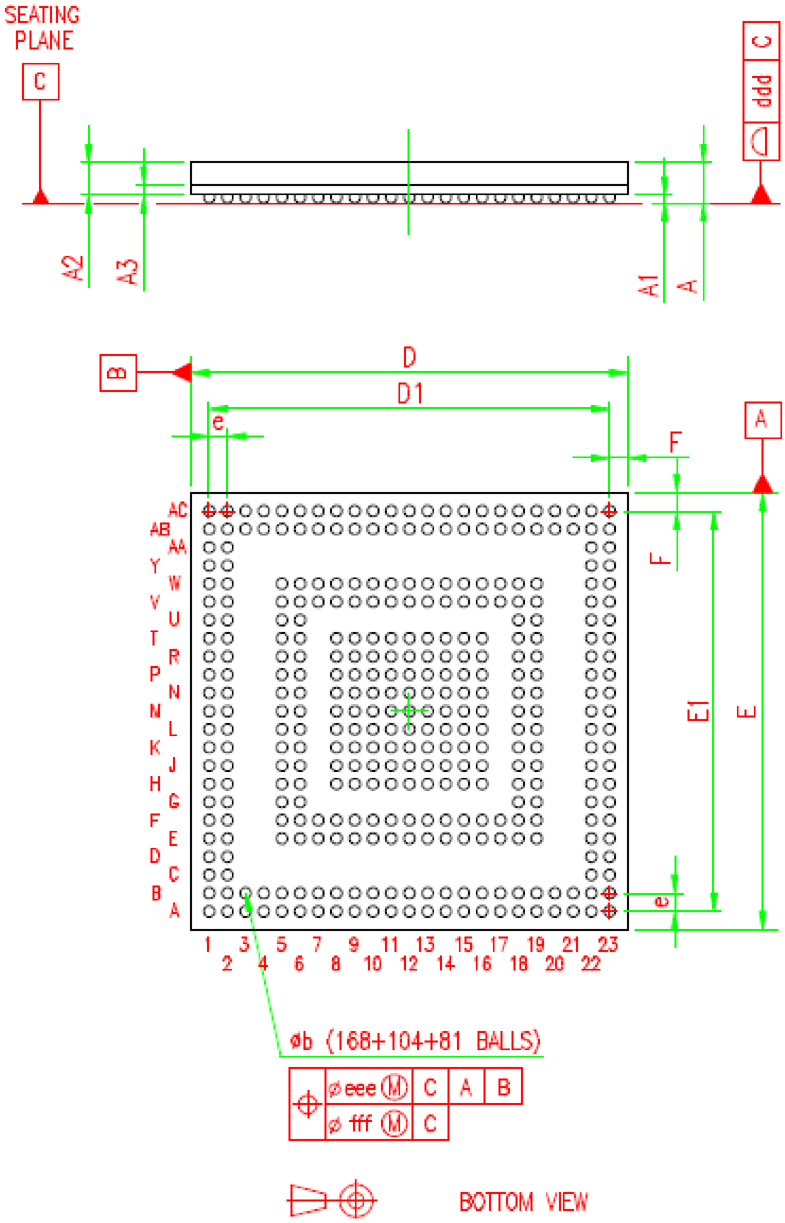
Figure 50 - South-East side

12	13	14	15	16	17	18	19	20	21	22	23	
vslope_tdc	ibo_charge_lg	ibi_Inv_hg	ibi_peak_hg	ibo_peak_hg	ibo_discri_charge	ibo_Inv_lg	ib_1nA_peak_lg	ibo_discri_adc	select	rstb_sr	sr_in	A
ib_sca_hg	ibo_Inv_hg	ib_1nA_peak_hg	ib_sca_lg	ibi_Inv_lg	ibi_peak_lg	ibo_peak_lg	ibi_discri_adc	ib_otaq	ck_sr	load_sc	sr_out	B
										pwron_d	Trig_MUX	C
										D_probe	VH	D
vref_charge_hg	vref_charge_lg	out_charge	out_bias	out_time	A_probe	sel_monitoring	ck_read			VL	NOR64_charge	E
vddm	vddm	vddm	vddd	vddd	vddd	vddd	vddd			NOR64_time	Dout_Topp	F
						vddd	vddd			Ton_Top	Dout_Topn	G
gndm	gndm	gndm	gndd	gndd		vddd	vddd			StartSyst	Dout_0_15p	H
gndd	gndd	gndd	gndd	gndd		vddd	vddd			Ton_0_15	Dout_0_15n	J
gndd	gndd	gndd	gndd	gndd		vddd	vddd			VL	Dout_16_31p	K
gndd	gndd	gndd	gndd	gndd		vddd	vddd			Ton_16_31	Dout_16_31n	L
gndd	gndd	gndd	gndd	gndd		vddd	vddd			RazChn	Dout_32_47p	M

Figure 51 - North-West side

gndd	gndd	gndd	gndd	gndd		vddd	vddd			Ton_32_47	Dout_32_47n	N
gndd	gndd	gndd	gndd	gndd		vddd	vddd			ForceConvb	Dout_48_63p	P
gndd	gndd	gndd	gndd	gndd		vddd	vddd			Ton_48_63	Dout_48_63n	R
gndm	gndm	gndm	gndd	gndd		vddd	vddd			resetb	ck_40p	T
						vddd	vddd			N/C	ck_40n	U
vddm	vddm	vddm	vddd	vddd	vddd	vddd	vddd			OvfCptTop	ck_160p	V
vcasc_discri	in_ctest	in_adc	vslope_adc_T	vref_adc_Q	vref_CP	ibias_V2I	vddd			ibi_rx	ck_160n	W
										ibo_rx	val_evt_p	Y
										N/C	val_evt_n	AA
vth_delay	vcasc2_tdc	vbg	vref_adc_T	vslope_adc_Q	vth_Q	ib_input_Dcshift	R_V2I	pwron_dac	ext_trig	pwron_adc	vcm_tx	AB
vdac_pa	Inpadac_ext	ib_delay	ramp_adc_T	ramp_adc_Q	ibi_bias_CP	ibi_comp_CP	test_VCO	PLL_Out	hold	pwron_a	ib_tx	AC
12	13	14	15	16	17	18	19	20	21	22	23	

Figure 52 - South-East side



DIMENSIONS

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A			1.20
A1	0.15		
A2		0.88	
A3		0.28	
b	0.25	0.30	0.35
D	11.85	12.00	12.15
D1		11.00	
e		0.50	
E	11.85	12.00	12.15
E1		11.00	
F		0.50	
ddd			0.08
eee			0.15
fff			0.05

Figure 53 - TF-BGA 353 mechanical drawing

9 Bug list & hotfix log

- Non recorded

10 Document version

Version	Date	Pages	Changelog
1.0	21/10/2016	38	Initial Release
1.1	19/07/2017	45	Updated info
1.2	01/12/2017	74	Updated info
1.3	08/03/2019	74	Update in Table 9 Probe

			register
1.4	28/09/2023	75	ReadOut Clock + minor updates