weeroc

High-end Microelectronics Design

Triroc1a Evaluation Board Software User Guide

Table of content

1 Introduction 4
2 Installation & Test of the evaluation board 4
2.1 Pre requisites 4
2.2 Installation guide 5
3 Evaluation board presentation 6
3.1 Setup for power supply 7
4 Software interface 8
4.1 Setup tab 8
4.2 Slow Control, Probe and Read tabs 9
4.2.1 Slow Control 1 – Main settings: Analog front end and digital settings 10
4.2.2 Slow Control 2 – Input DACs 13
4.2.3 Slow Control 3 – Enable tab 14
4.2.4 Slow Control 4 – Internal charge injection, Time Trigger threshold tuning and Discriminator outputs mask 15
4.2.5 Analog and Digital probes & SCA Read tab 16
4.3 Firmware option configuration 17
4.4 S-curve tests 18
4.5 Hold Scan 19
4.6 Data Acquisition 20
4.7 PCB information, FPGA Test Pins and ASIC ball-out 22
4.8 Injection Test Signal 25
4.9 Help Button, Save Image and WEEROC website link 26
5 Known bugs and issues 27
6 Document revision 27

List of figure and table

Figure 1 – Evaluation board switches, I/Os and power supply connectors 6
Figure 2 – Triroc1A software connect tab 8
Figure 3 – Slow Control "Main settings" tab 10
Figure 4 – Slow control Threshold Value 10
Figure 5 – Slow control main page settings for trigger latch and input signal polarity 10
Figure 6 – Slow control trigger mask and charge injection matrix 11
Figure 7 – Slow control pre amp impedance and LVDS transmitter 11
Figure 8 – Slow control Shaper parameters 11
Figure 9 – Slow control Track/Hold settings 12
Figure 10 – Slow control ADC settings 12
Figure 11 – Slow control noise rejection settings 12
Figure 12 – Slow Control 2 tab – Input DACs 13
Figure 13 – Slow Control 3 tab – Enable and disable tab 14
Figure 14 – Slow Control 4 tab – Internal charge injection, Time Trigger threshold tuning and Discriminator outputs mask 15
Figure 15 – Probe & Read Registers tab 16
Figure 16 – Firmware Options tab 17
Figure 17 – S-curves test 18
Figure 18 - Hold Scan data per channel 19
Figure 19 – Data decoded tab 20
Figure 20 – Data Acquisition 21
Figure 21 - Charge injection scheme 25
Figure 22 – Pulser injection signal 26

Table 1 – Saved data Acquisition example file 21
Table 2 – PCB I/Os information 22
Table 3 – ASIC ball-out information and corresponding DC value 24

1 Introduction

TRIROC1A is a 64-channel **front-end ASIC** designed to readout silicon photomultipliers (**SiPM**) with both polarities for particle time-of-flight measurement applications. Targeted applications will be PET scan (medical imaging) and gamma ray detection.

This guide explains how to install and use the test board for TRIROC1A and how to operate with its associated software.

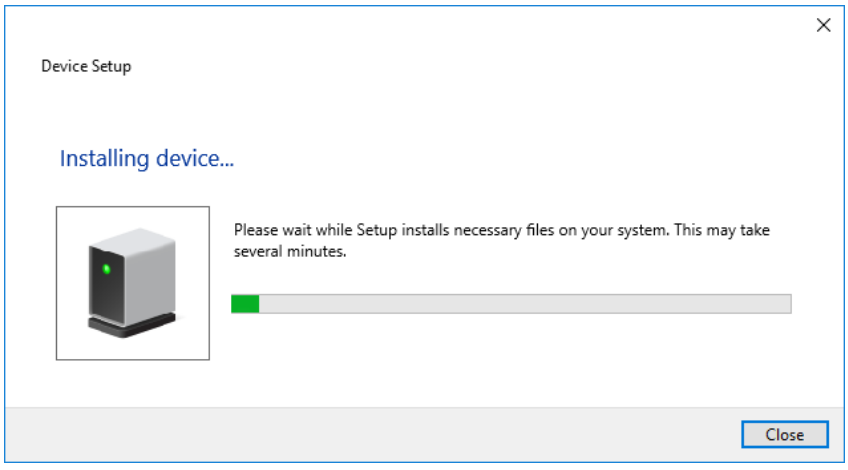
2 Installation & Test of the evaluation board

2.1 Pre requisites

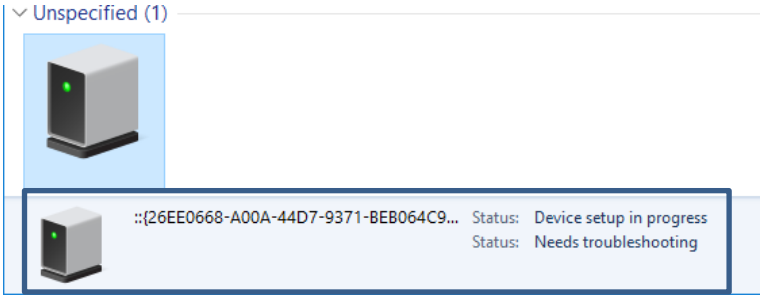
The use of this PCB requires:

- A computer (windows OS) with USB connection
- The FTDI driver that you can find on their website: https://www.ftdichip.com/Drivers/D2XX.htm
- A USB-A to mini-USB cable
- Optional : A positive output power supply (delivering 500mA)

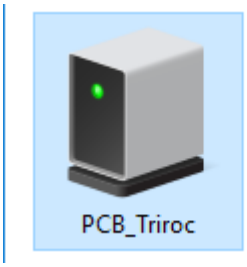
The first time a Weeroc testboard is plugged, the following message should prompt.



In order to verify that the drivers are correctly installed, go in the control panel under the "Devices and Printers" window. PCB_Triroc1A device should have gone from



to



2.2 Installation guide

Before running the software for the first time, please verify that the testboard is correctly identified in the "Devices and Printers" window under the control panel. The release of the TRIROC1A user interface can be found in the Weeroc download center on the website http://www.weeroc.com .

3 Evaluation board presentation

This evaluation board is mainly developed to allow characterization and debug of the ASIC. Some features were added on the board or in the firmware/software in order to allow its use with real detector or within an experiment. Schematics of this board, firmware and software code sources are provided so that users can modify this evaluation system to fit their requirements.

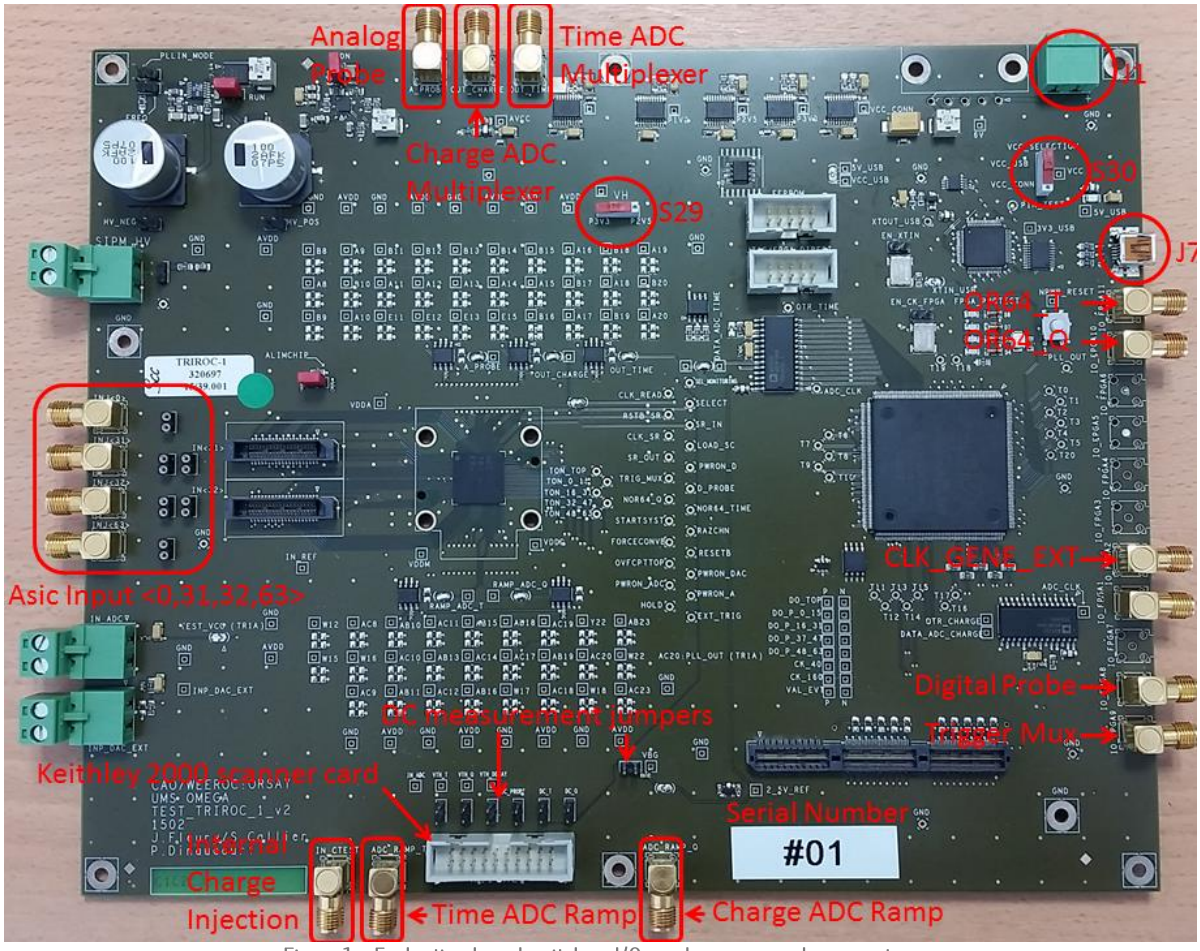


Figure 1 – Evaluation board switches, I/Os and power supply connectors

3.1 Setup for power supply

This board can be powered either by a test bench DC power supply or USB bus. On-board switch S30 can be used in order to select the power source (external or USB).

J1 connector is used to connect the board to an external DC power supply. Only positive 6V power supply delivering at least 500mA is required for powering this board.

On the other hand, J7 connecter (mini USB type) can be also used to power the board. Just connect the USB cable to a PC and select the S30 switch to correct position for powering the board.

As described in the datasheet, the high-level voltage swing of the digital outputs (Trig_Mux and Digital Probe) can be lowered from the nominal value of 3.3V. An on-board switch (S29) is used in order to select the voltage of VH of these digital outputs. Users can either select 3.3 V or 2.5 V for the high-level voltage of the digital outputs. The low-level swing, VL, is connected to the ground of the evaluation board.

4 Software interface

4.1 Setup tab

The software has been written in the C# language and has been developed with visual studio. The source code is available to help comprehend the functionality of this software. This is especially useful if users aim to develop their own DAQ system.

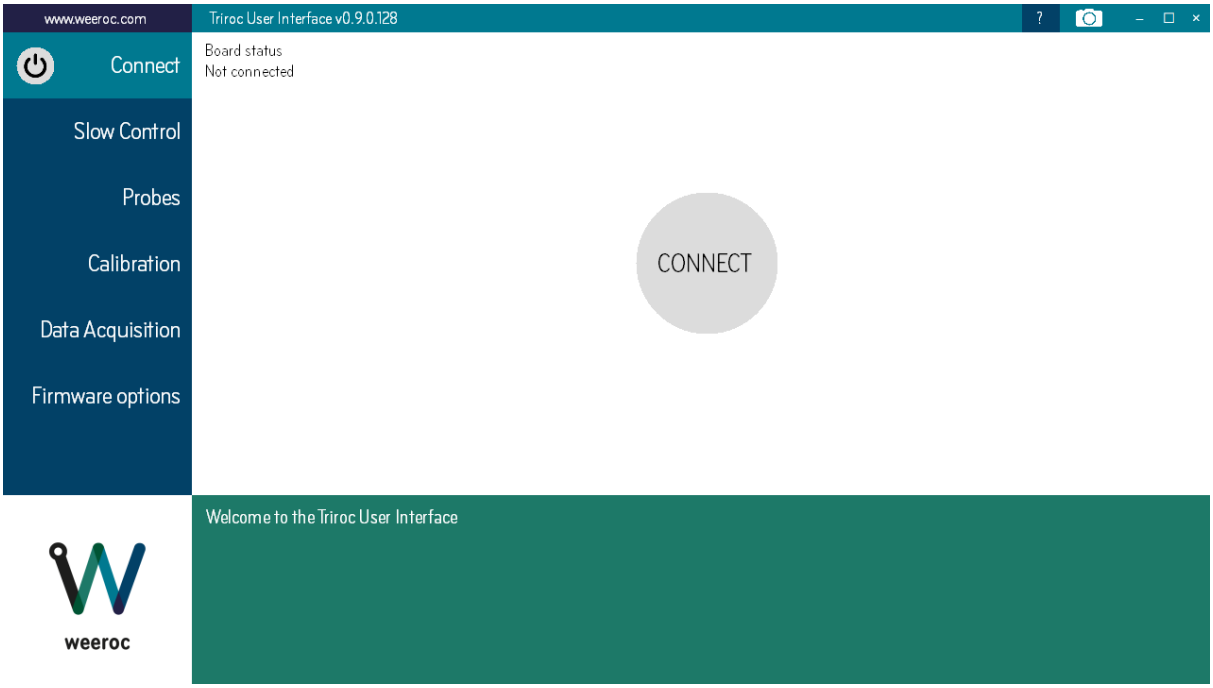


Figure 2 – Triroc1A software connect tab.

To start the evaluation board, the following steps are required:

1. Connect the USB cable from the PCB to your computer.
2. Provide power supply to the PCB if not provided by the USB (the power supply can be switched between external and USB with the jumper on the top right of the evaluation board).
3. Start the software and click on the "Connect" round button.

When connecting the evaluation board, drivers for the USB device should install automatically. If it is not the case, the drivers can be found on the FTDI website (http://www.ftdichip.com/Drivers/D2XX.htm).

When this software is launched and the "Connect" button clicked, no error should occur, meaning that the installation has been done successfully and all the drivers and dll have been found. If a crash occurs or if you need assistance for any other issue with the software, contact the Weeroc support by opening a new support ticket at the address http://www.weeroc.com/my-weeroc/support.

While this guide will help users to use this software and evaluation board, it should be noted that there is an embedded help in the software. By hovering controls with the mouse, the green bottom part will be filled with information on the object being hovered.

4.2 Slow Control, Probe and Read tabs

All the slow control parameters (referred as SC afterwards) of the TRIROC1A are displayed on 4 tabs, allowing tuning & tests of different settings.

To program the TRIROC1A, just click once on the "Send SC" button available on any tab. In each SC related tabs, there is an indicator displaying the status of this SC register and should be green after a "Send SC" command.

The Slow Control settings tab can be saved in a text format file through "Save SC" button, and reloaded from this file by the "Load SC" button. Note that the path & name for this file has to be provided in the saving pop up page.

To load old Triroc1A software slow controls from LabVIEW press the "Import LV file" button.

4.2.1 Slow Control 1 – Main settings: Analog front end and digital settings

The "Main settings" tab allows users to access various parameters of the analog and the digital part of this ASIC. The parameters here will affect the behaviour of the whole ASIC.

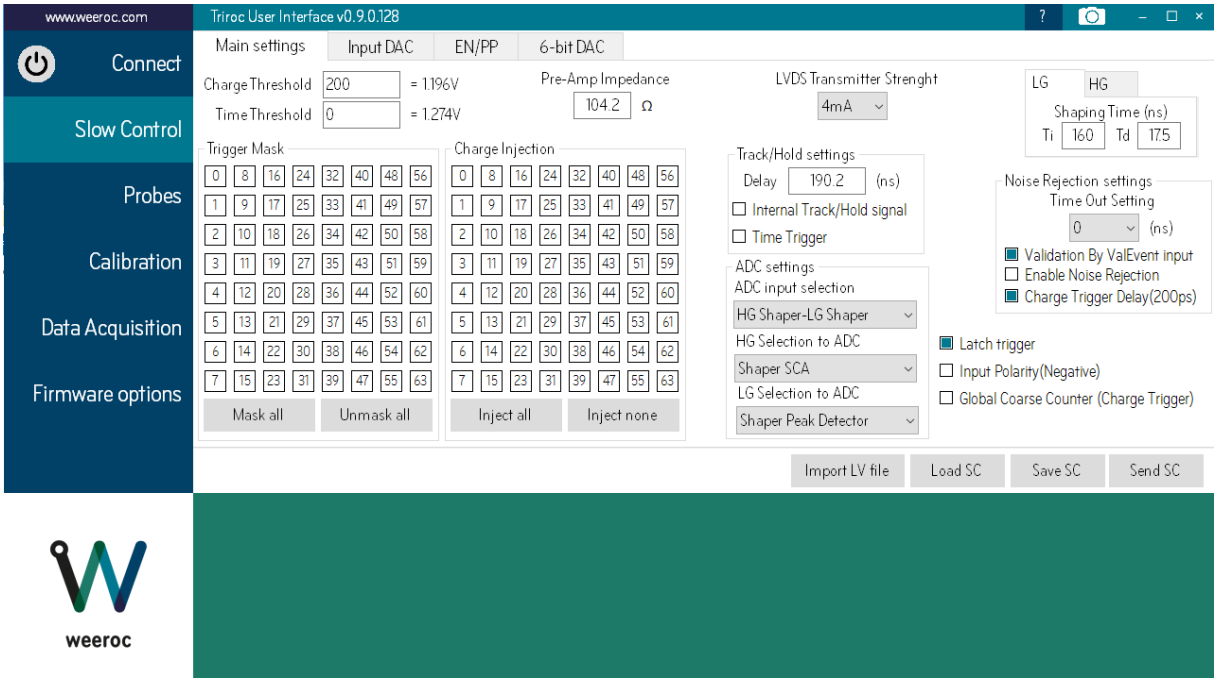


Figure 3 – Slow Control "Main settings" tab

In this section, it is possible to set up some important ASIC parameters such as Charge and Time Threshold where users need to put a code value between 0 and 1023 to see the threshold voltage change (refer to Figure 4).

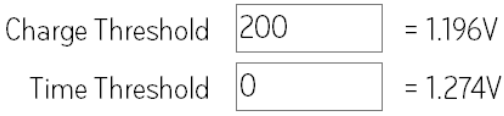


Figure 4 – Slow control Threshold Value

It is also possible to latch the trigger outputs with the latch trigger checkbox as shown in Figure 5.
Additionally users will need to set "Input polarity" checkbox (refer to Figure 5) according to the input signal polarity (negative or positive).

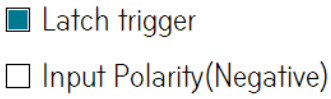


Figure 5 – Slow control main page settings for trigger latch and input signal polarity

With the Trigger Mask matrix (Figure 6) setting, it is possible for users to mask channels in order to avoid cross talk, reduce noise or disable unusable channel for example.

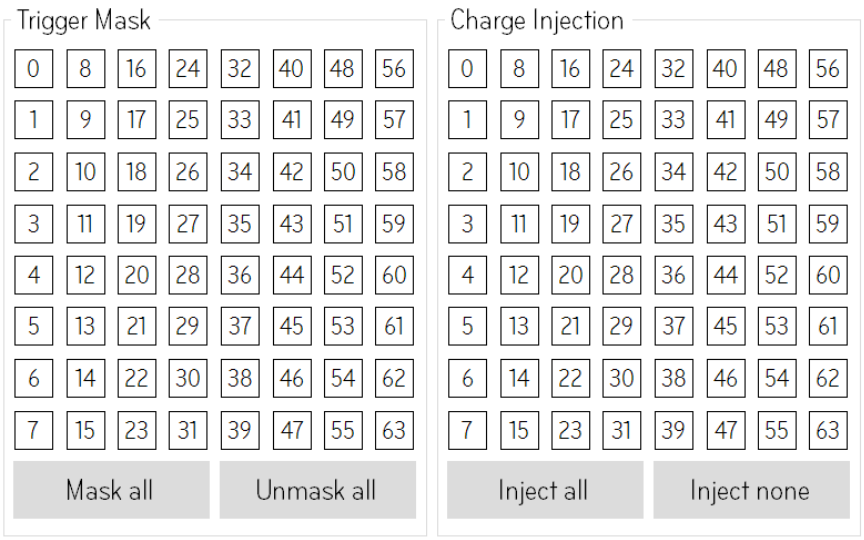


Figure 6 – Slow control trigger mask and charge injection matrix

With the Charge injection matrix (Figure 6) setting, it is possible for users to select the channels which will receive charge injection stimuli.

The Pre-Amplifier Impedance can be modified with the associated textbox by giving a value in ohms as indicated in Figure 7.

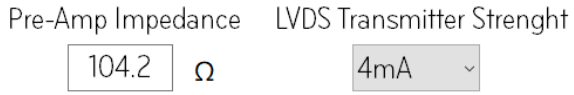


Figure 7 – Slow control pre amp impedance and LVDS transmitter

It is also possible to change LVDS transmitter current level with the associated combo box as shown in Figure 7.

Users can also set shaping time (defined by integration time constant, Ti and derivation time constant, Td) for High Gain (HG) and Low Gain (LG) shapers in order to modify each shaper gain or response time (Find more information in section 3.2 of datasheet). Refer to Figure 8.

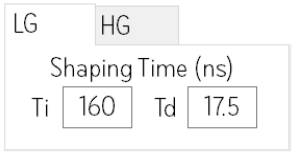


Figure 8 – Slow control Shaper parameters

In the Track and Hold section there is a textbox were it is possible to set up the track and hold delay (Figure 8). This value can also be found automatically with the hold scan calibration test (refer to section 4.5).
It is possible to select if the track and hold signal is internal or external with the associated checkbox.
Users can select either Charge or Time trigger for internal Track and Hold with the last checkbox of this section.

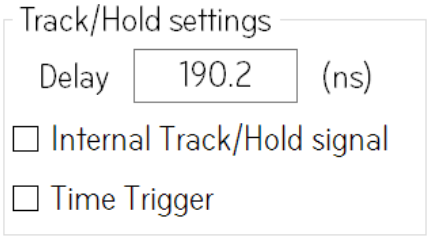


Figure 9 – Slow control Track/Hold settings

In next section of this tab (Figure 10), there are the settings for internal ADCs where for example the ADC input can be changed between TDC-LG Shaper, HG Shaper-LG Shaper, TDC-HG Shaper or External Input. In this tab page, it is also possible to select HG and LG shaper outputs to be converted by ADC. For the HG selection, there is a choice between Shaper Peak Detector, Pre-Amp SCA or Shaper SCA and for LG, the choices are between Shaper Peak Detector and Shaper SCA.

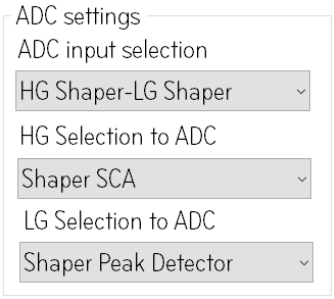


Figure 10 – Slow control ADC settings

Next section deals with the noise rejection as shown in Figure 11. It is possible to modify the time out for noise rejection module (validation by Charge Trigger) in order to improve the noise rejection by adding an extra delay (25ns, 50ns or 75ns). The delay can be increased further by adding 200ps to Charge Trigger.

It is also possible to activate the validation by Charge_Trigger or ValEvent with the associated checkbox. With ValEvent checked, event will be only validated by Val Event input and Charge trigger.
Users can also choose to enable or disable the noise rejection module within the associated checkbox. By disabling this module, analog signal conversion and data transmission will be initiated solely by Time trigger. On the other hand, enabling noise rejection module will initiate signal conversion once Charge and Time triggers occur within the selected time window.

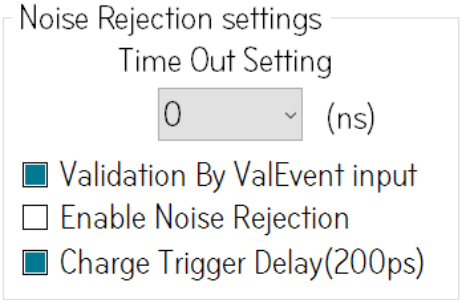


Figure 11 – Slow control noise rejection settings

4.2.2 Slow Control 2 – Input DACs

Slow Control 2 tab is related to the input DAC for each channel. Users can change input DAC value for each channel by entering voltage value between 0.2V and 2.2V. All the channel values can be changed at the same time with the set all option and the associated text box and button. There is also an array of buttons identified by channel number for enabling or disabling the input DAC individually.

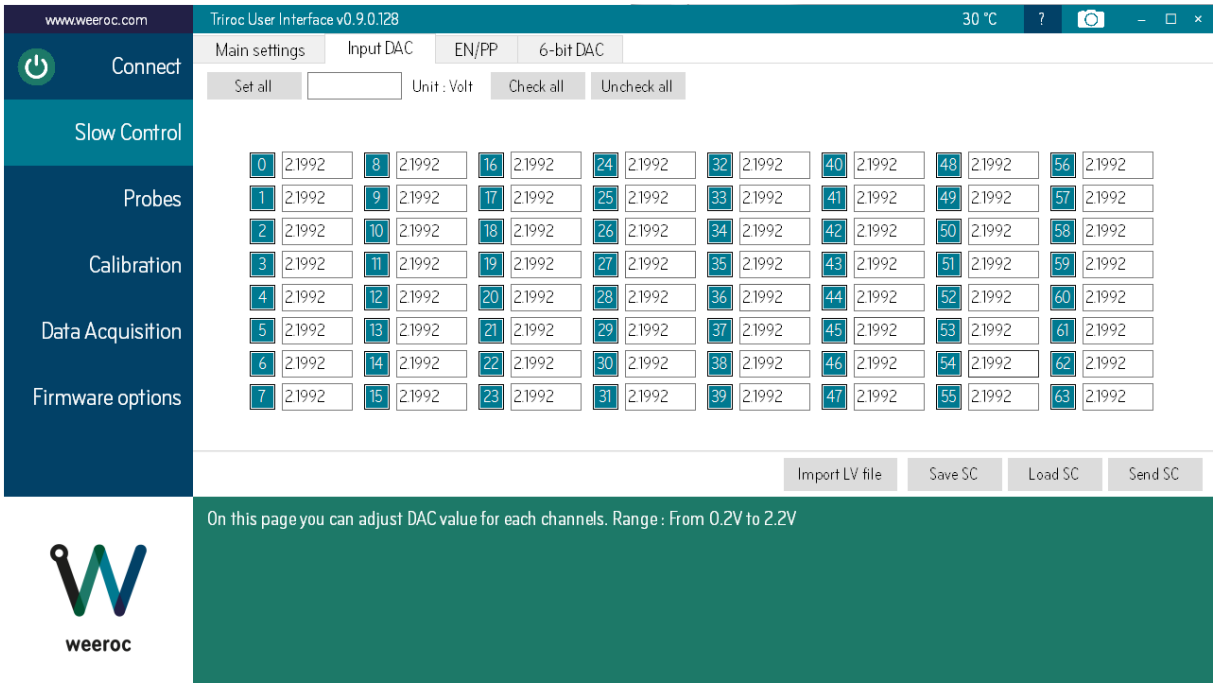


Figure 12 – Slow Control 2 tab – Input DACs

4.2.3 Slow Control 3 – Enable tab

Slow Control 3 has been created to allow users to enable or disable some ASIC part and also put some part on Power Pulsing (PP) mode (Please find information on the options of this tab page in the slow control part of the datasheet).

Figure 13 – Slow Control 3 tab – Enable and disable tab

4.2.4 Slow Control 4 – Internal charge injection, Time Trigger threshold tuning and Discriminator outputs mask

Slow Control 4 tab is for fine tuning Time Trigger threshold. Time Trigger threshold can be tuned individually for each channel via a 6-bit DAC. Users can choose to adjust the threshold value for each channel, use a common value for all channels or apply a value to a specific channel and another value for other channels. All the channel values can be changed at the same time with the set all option and the associated text box and button.

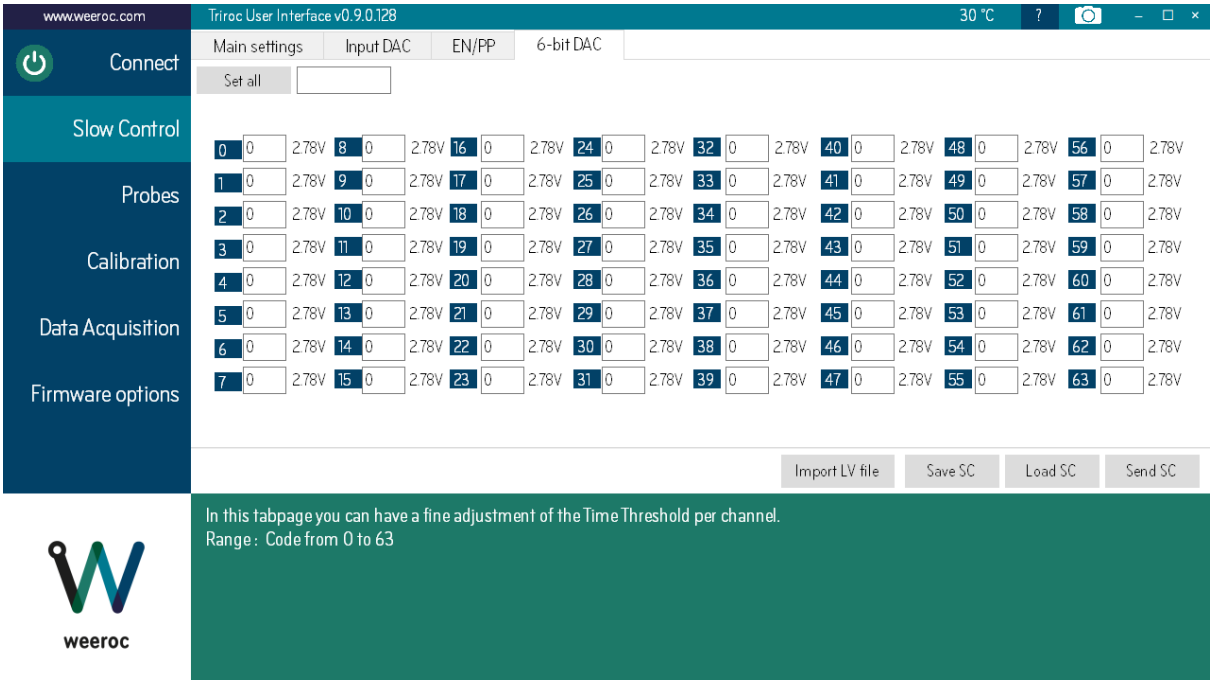


Figure 14 – Slow Control 4 tab – Internal charge injection, Time Trigger threshold tuning and Discriminator outputs mask

4.2.5 Analog and Digital probes & SCA Read tab

An internal ASIC shift register allows to probe or monitor analog and digital outputs for a given channel. Users can select an analog and a digital probe to be monitored on the evaluation board by selecting the appropriate probes and click on the Send Probe button.

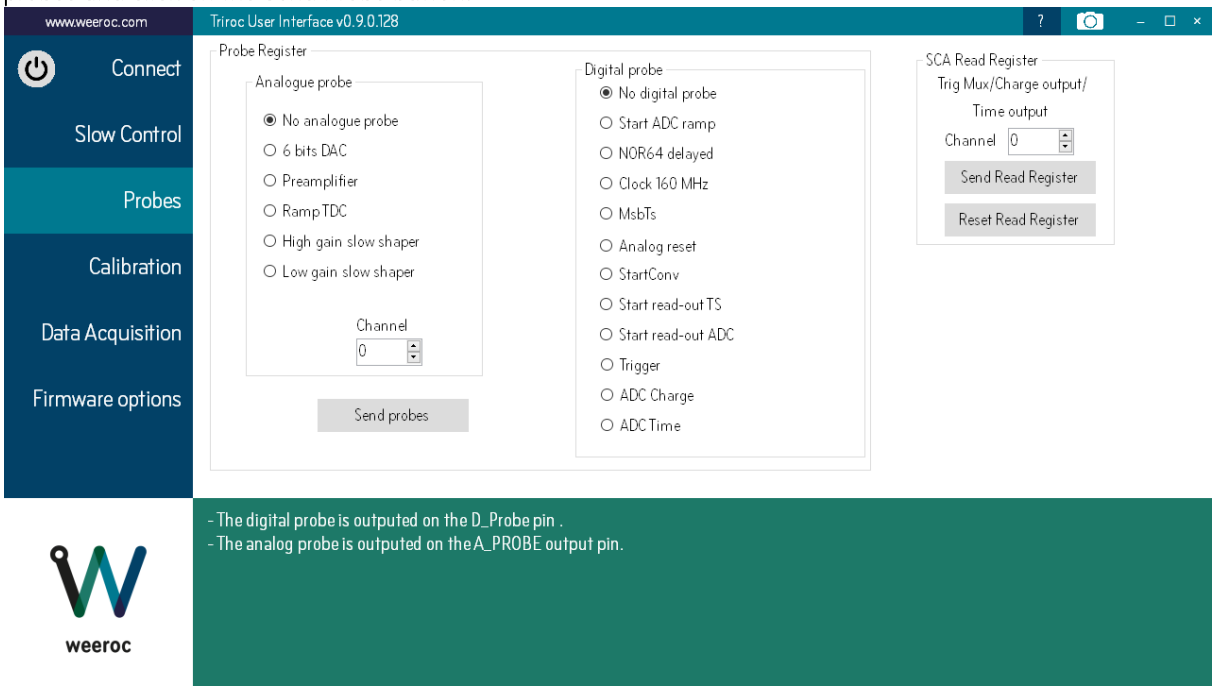


Figure 15 – Probe & Read Registers tab

The SCA Read Register is an analog memory register of the shaper outputs and this signal is available through multiplexed outputs (Charge and Time outputs) on the evaluation board. Additionally same register is used to send Time triggers through a multiplexed output (Trig Mux). Select a channel and click on send read register in order to modify the Charge output, Time output and Trig Mux output signal.

4.3 Firmware option configuration

This tab is essentially used for the configuration of the FPGA on board.

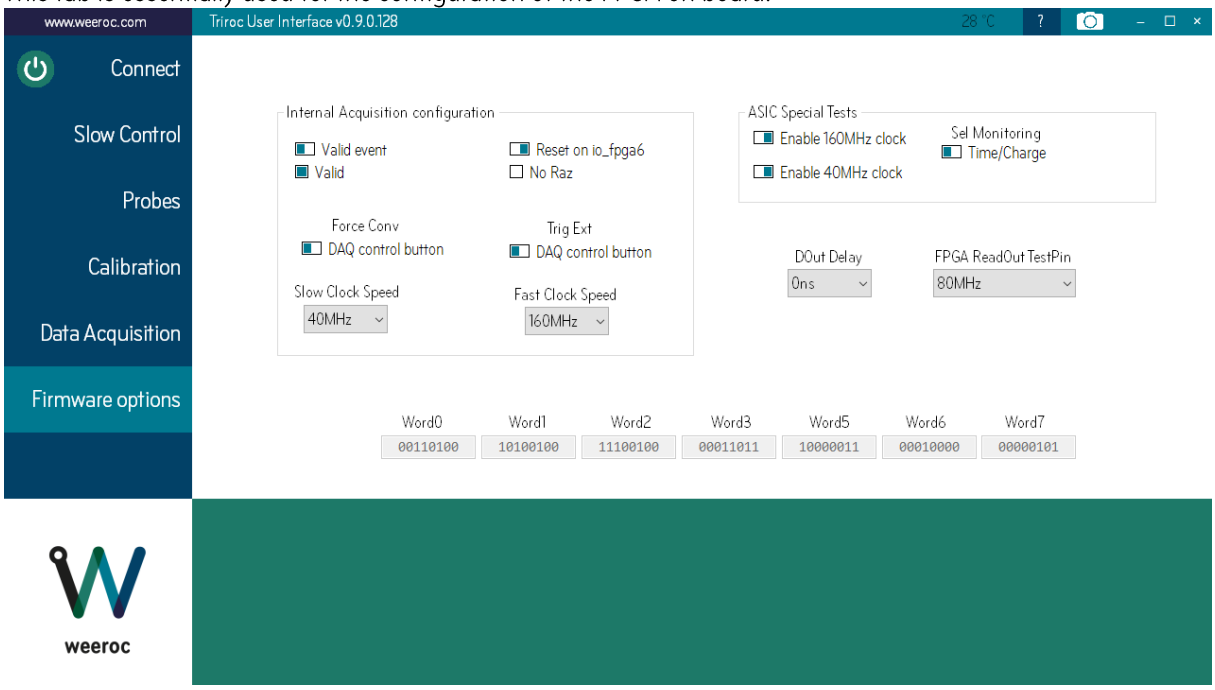


Figure 16 – Firmware Options tab

On this tab, several signals for ASIC, which are mostly related to the digital part, can be modified. The settings for some signal are displayed by a toggle switch-button. A right switch on the front page corresponding to logic value "1" or ON (example: "Valid Event" or "Reset on io_fpga6") and vice versa. Additionally, the frequency of the clocks ("Fast Clock Speed" and "Slow Clock Speed") required by the ASIC can be modified from the drop-down lists.

Users can visualize the FPGA configuration word sent to evaluation board on the bottom of the page.

4.4 S-curve tests

Trigger efficiency or S-curve measurement can be accessed from the tab shown in Figure 17. This tab is used for testing the different channels trigger efficiency in function of the threshold value. This calibration test can be performed either in digital or analog mode.

In order to perform the measurements, the following setup to the evaluation board is required:

- Reference Synchronisation(IO_FPGA7) for Digital S-curves
- Reference Synchronisation(IO_FPGA2) for Analog S-curves
- Input signal: on-board connectors (ASIC INPUT <0,31,32,63>), Internal Charge injection. For the injection signal to be applied please refer to section 4.8 .
- Users can select the injection frequency with the synchronisation signal sent by FPGA to the pulser (refer to Figure 21 in section 4.8). To modify this value, users have to select clock value in the clock drop-down list. Available values: 1 kHz, 10 kHz, 50 kHz and 100 kHz.

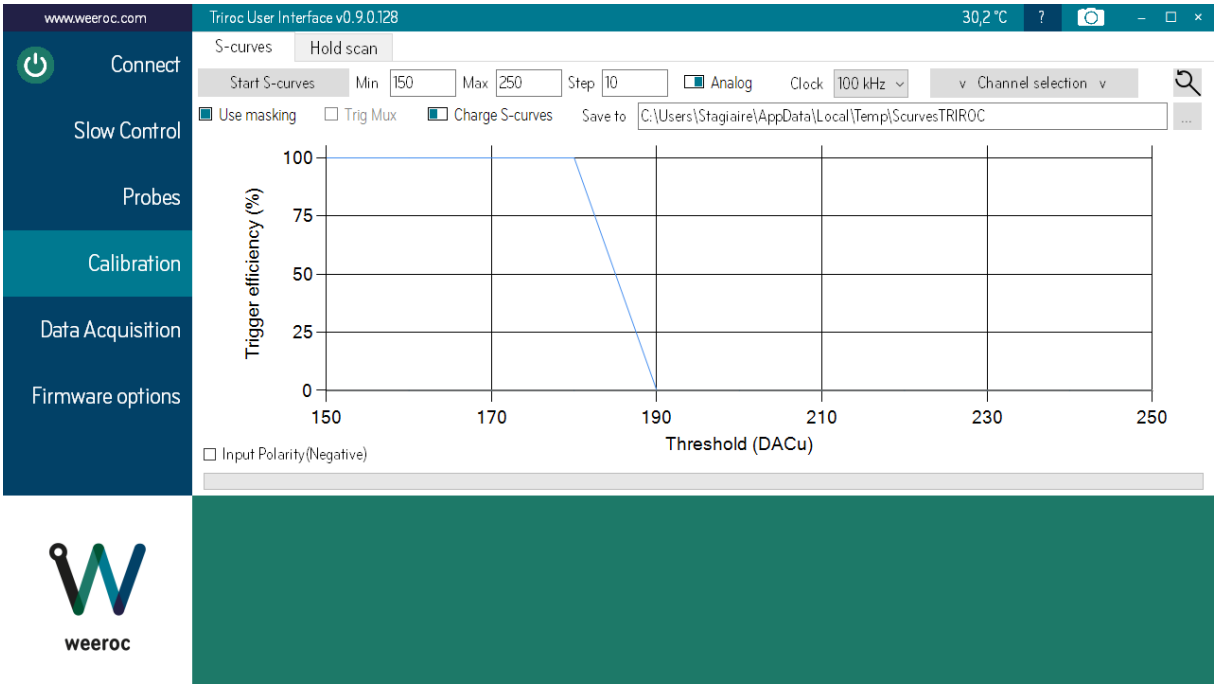


Figure 17 – S-curves test

Lastly, this tab will modify ASIC Slow Control parameter in order to make sure to perform S-Curves correctly.

The remaining fields of this tab, "Min", "Max" and "Step" should be filled accordingly. Both DACs (DAC Q & DAC T) are 10-bits, thus giving maximum DAC code of 1023.

In this tab it is possible to modify directly some parameters in order to have different test results:

- "Mask channel": If activated (Green on selected channels), only the currently measured channel will be unmasked if the "Use Masking" checkbox is check.
- "Analog/Digital S-Curves" with this switch box you can select if you want to have a digital S-Curve based on the data acquisition system or an analog S-Curves.

4.5 Hold Scan

The second tab under the calibration page is the "Hold scan". It will trace shaper outputs signal by varying the "hold" delay value on a single channel. Users will have to select channel to be observed in "Channel" field. In order to have it working properly a signal should be injected in the measured channel and a trigger must start the data acquisition (For the injection signal setup, refer to section 4.8). A fit on the result of the scan is performed and the x-axis value corresponding to the maximum of the fit is automatically extracted. The delay parameter (in Main settings tab – section 4.2.1) is updated with the extracted value. The fit is meant to be used with the SCA. Users can select either the Time trigger or the Charge Trigger for the hold scan calibration test with the associated checkbox.

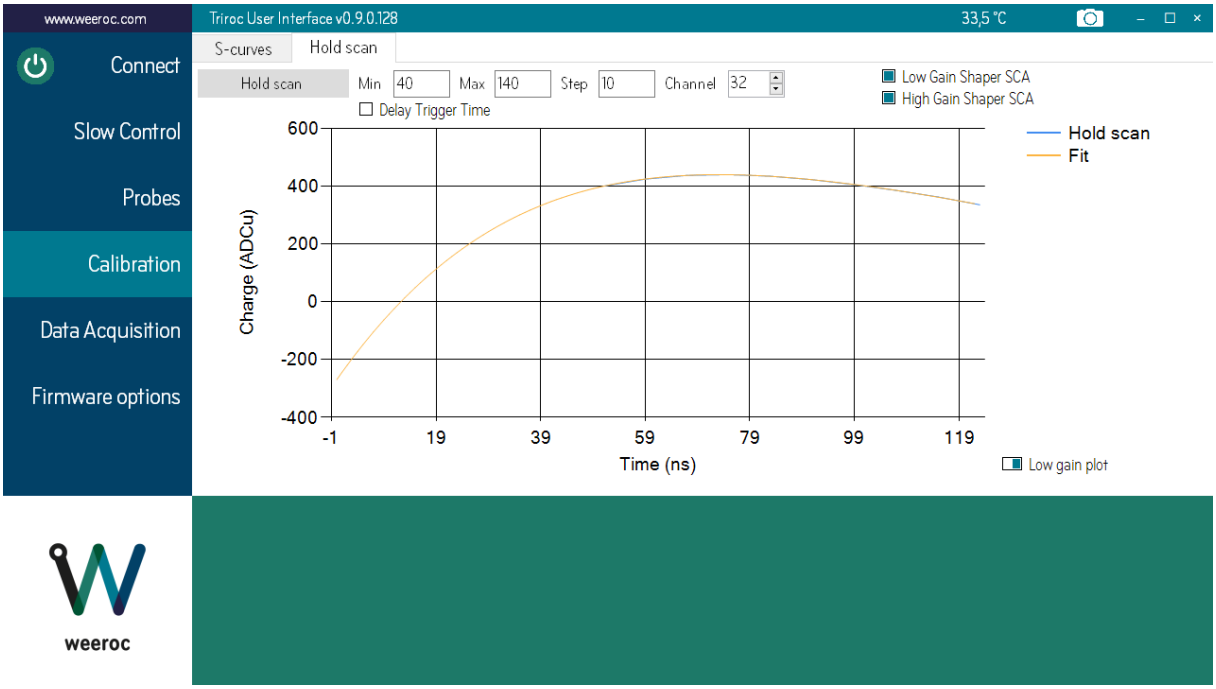


Figure 18 - Hold Scan data per channel

Users can select to plot the hold scan for the high gain or the low with the associated switchbox and choose between plot the hold scan in peak detector mode or in SCA.

4.6 Data Acquisition

A simple DAQ interface is also available as shown in Figure 19 and Figure 20. The tab in Figure 19 is used mainly for debugging the DAQ system, as it will display decoded data from the ASIC.

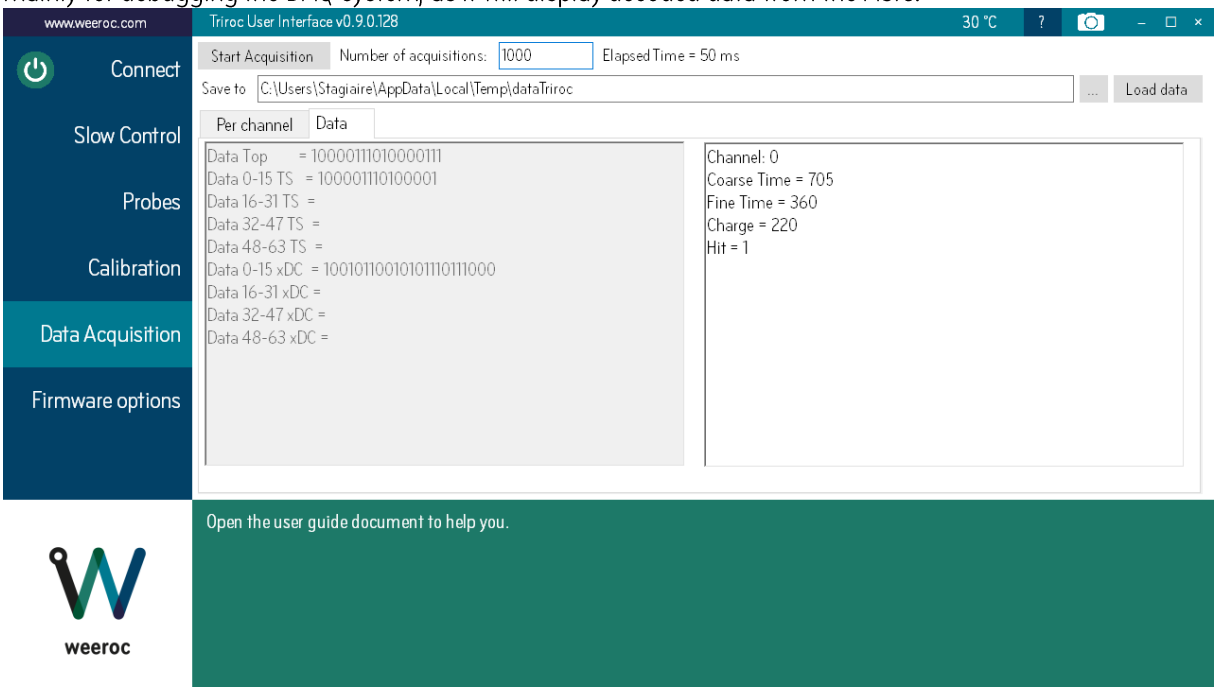


Figure 19 – Data decoded tab

The data acquisition will be started when "Start Acquisition"" is clicked and the number in "Number of Acquisition" field will indicate how many times the ASIC will be readout. The data will be displayed in the Data tabs of the interface. The histograms of the displays will show only the selected channel number in "Channel" field which has to be filled prior to run the data acquisition. The histograms that users will visualize, depend of the ADC settings selected in the first Slow control tab page.

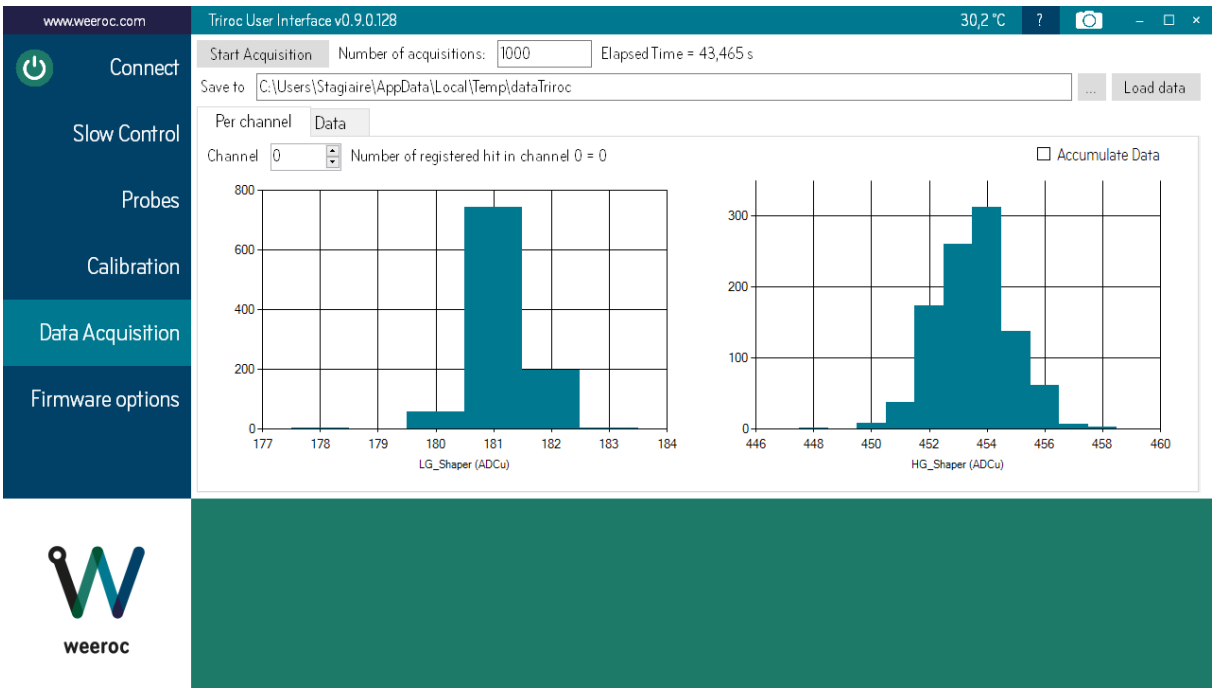


Figure 20 – Data Acquisition

Lastly, this tab will modify ASIC Slow Control parameter in order to make sure to perform Data acquisition correctly. Users have to connect the pulser synchronisation input on io_fpga7 in order to synchronise the pulser to the pulser injection signal (an injection signal example is available in section 4.8 of this user guide).
At the end of the acquisitions the data are automatically saved as a text document at the path that users have choosen on the "Save to" textbox. Users have to select a path and the name of the file in order to save it where he wants.

Channel	CoarseTime	FineTime	Charge	Hit
63	400	243	130	1
63	400	242	130	1

Table 1 – Saved data Acquisition example file

In this document format the data are separated by a single space character. With this document (as shown in Table 1) users will have the channel number of the trigged channel, the coarse time value, the fine time value, the charge value and the channel hit. Please note that FineTime data and Charge data are assignable ADC input and the data here will correspond to the selection done in Figure 10. Please refer to Section 4.1 of the datasheet for more information about the assignable ADC inputs.

4.7 PCB information, FPGA Test Pins and ASIC ball-out

The items in Table 2 can be used by users in order to identify the I/Os of the ASIC.

INPUTS / OUTPUTS
IO_FPGA1 : IN: Val Evt
IO_FPGA2 : OUT: CLK_GENE_EXT (Scurve) / Ck40M (AutoDAQ)
IO_FPGA3 : IN: Power Pulsing
IO_FPGA4 : IN: Trig_Ext / Coincidence
IO_FPGA5 : IN: Hold
IO_FPGA6 : IN: Raz Chn
IO_FPGA7 : OUT: coincidence / strt_DAQ (AutoDAQ)
IO_FPGA8 : OUT: Digital Probe
IO_FPGA9 : OUT: Trigger MUX
IO_FPGA10 : OUT : OR32_Q
IO_FPGA11 : OUT : OR32_T

Table 2 – PCB I/Os information

The information shown in Table 3 is for the identifying ball-out of the ASIC. All the ball-out listed here is available on the evaluation board and can be identified by the corresponding silkscreen label. These points can be probed directly and measured for example with a multi-meter.

Bias	Type (Ballout)	Simulated value	Measured value
vref_dac_T	Direct pad (AC8)	1.185V	1.16V
vref_dac_Q	Direct pad (AC9)	0.996V	1.02V
iref_dac	Direct pad (AB10)	2.24V	2.26V
ibo_dac	Direct pad (AC10)	0.629V	0.61V
vcasc1_tdc	Direct pad (AB11)	1.2V	1.22V
ib_otabg	Direct pad (AC11)	0.53V	0.51V
vdac_pa	Direct pad (AC12)	1.54V	1.56V
vcasc_discri	Direct pad (W12)	2.29V	2.32V
vcasc2_tdc	Direct pad (AB13)	1.7V	1.72V
ib_delay	Direct pad (AC14)	0.65V	0.7V
vbg	Direct pad (AB14)	2.494V	2.527V
vslope_adc_T	Direct pad (W15)	0.267V	0.27V
vref_adc_T	Direct pad (AB15)	1.054V	1.073V
vref_adc_Q	Direct pad (W16)	0.937V	0.9V
vslope_adc_Q	Direct pad (AB16)	0.384V	0.38V
ibi_bias_CP	Direct pad (AC17)	2.36V	2.26V
ibi_comp_CP	Direct pad (AC18)	0.71V	0.71V
ib_input_Dcshift	Direct pad (AB18)	2.34V	2.34V
vref_CP	Direct pad (W17)	0.5V	2.34V
ibias_V2I	Direct pad (W18)	2.48V	2.395V
ib_tx	Direct pad (AC23)	0.6V	0.63V
vcm_tx	Direct pad (AB23)	1.2V	1.13V
ibo_rx	Direct pad (Y22)	1.18V	1.23V
ibi_rx	Direct pad (W22)	2.11V	1.99V
vref_charge_lg	Direct pad (E13)	0.99V(cmd_polarity='0') 2.04V(cmd_polarity='1')	1.02V 2.07V
vref_charge_hg	Direct pad (E12)	0.99V(cmd_polarity='0') 2.04V(cmd_polarity='1')	1.02V 2.06V
vref_tdc	Direct pad (E11)	0.91V	0.9V
ib_otaq	Direct pad (B20)	0.82V	0.83V
ibi_discri_adc	Direct pad (B19)	0.66V	0.65V
ibo_discri_adc	Direct pad (A20)	2.27V	2.14V
ibo_peak_lg	Direct pad (B18)	2.24V	2.06V
ib_1nA_peak_lg	Direct pad (A19)	2.56V	2.42V
ibi_peak_lg	Direct pad (B17)	0.68V	0.71V
ibo_inv_lg	Direct pad (A18)	0.66V	0.68V
ibi_inv_lg	Direct pad (B16)	0.66V	0.68V
ibo_discri_charge	Direct pad (A17)	2.27V	2.15V
ib_sca_lg	Direct pad (B15)	1.27V	1.2V

ibo_peak_hg	Direct pad (A16)	2.24V	2.04V
ib_1nA_peak_hg	Direct pad (B14)	2.56V	2.5V
ibi_peak_hg	Direct pad (A15)	0.68V	0.69V
ibi_inv_hg	Direct pad (A14)	0.66V	0.67V
ibo_inv_hg	Direct pad (B13)	0.66V	0.67V
ibo_charge_lg	Direct pad (A13)	0.8V(cmd_polarity='0') 0.92V(cmd_polarity='1')	0.82V 0.94V
ib_sca_hg	Direct pad (B12)	1.27V	1.27V
vslope_tdc	Direct pad (A12)	0.345V	0.36V
ibi_tdc	Direct pad (A11)	2.37V	2.23V
ibo_tdc	Direct pad (B11)	0.8V	0.81V
ib_6bit_dac	Direct pad (A10)	0.6V	0.59V
ibo_discri	Direct pad (A9)	1.42V	1.37V
ibi_discri	Direct pad (B10)	0.79V	0.8V
ibi_pa	Direct pad (A8)	0.76V	0.74V
vref_ota_inpdac	Direct pad (B9)	0.29V	0.29V
vref_isource	Direct pad (B8)	0.99V	1.01V

Table 3 – ASIC ball-out information and corresponding DC value

4.8 Injection Test Signal

In order to perform Data acquisition, S-Curves and Hold Scan, a pulser injection signal can be used to simulate input signal for the ASIC.

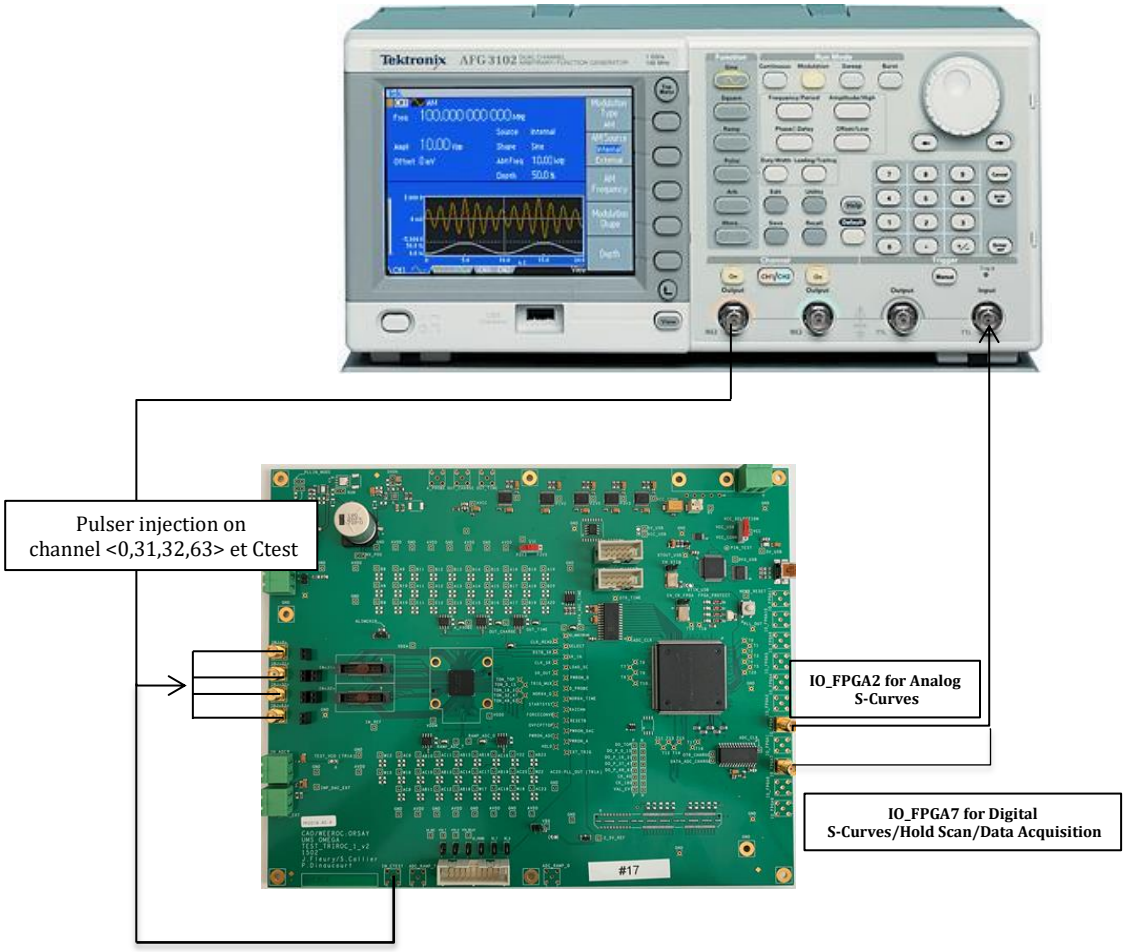


Figure 21 - Charge injection scheme

Signal produced by a Tektronix waveform generator as shown in Figure 22 can be used for this application in order to get an input signal similar provided by detector.

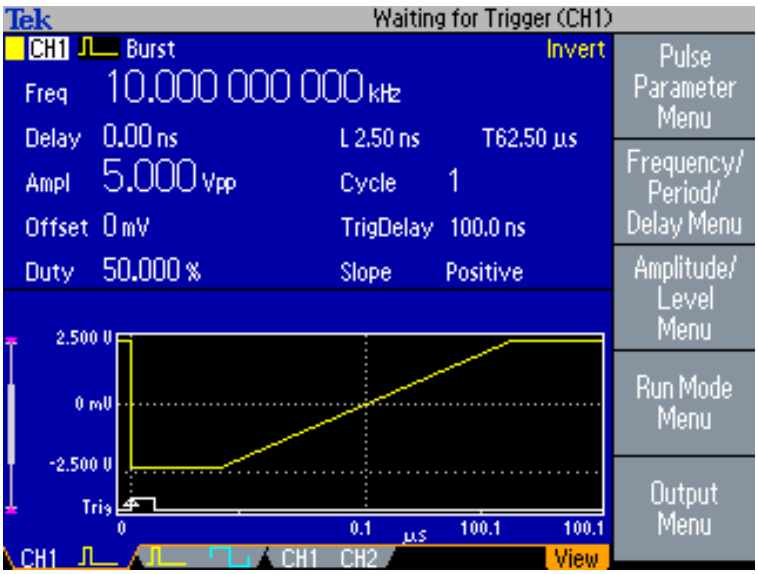


Figure 22 – Pulser injection signal

Signal Setup :

- Function : Pulse -> Burst -> 1-Cycle -> More-> Source External
- Output menu : Invert -> On
- Ampl : 5 Vpp
- Frequency : 10 kHz
- Trailing Edge : 62.5 us

To make the signal compatible with the ASIC input polarity, users need to verify the input polarity selection in the slow control parameter (Figure 5).

4.9 Help Button, Save Image and WEEROC website link

Users have the possibility of saving screenshot of the software at any moment with the capture button . A dialogue window will be opened and users will have to choose the saving path of the screenshot.

With this version of the software it is possible to access directly to the WEEROC's website with the link button www.weeroc.com.

5 Known bugs and issues

The Analog Time S-Curves can be long to plot (Around 8 minutes for 50 points and all the channel).

6 Document revision

Version	Date	Pages	Changelog
1.0	13/08/2019	27	Initial release for C# software. This document version related to Triroc1A 1.0 software version and the Triroc1A V128 firmware version